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DIPLOMARBEIT

Scanning Probe Capacitance Measurements on GaAs and Si with Schottky and MOS Junctions

Ausgeführt am Institut für

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der Technischen Universität Wien

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durch

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Contents

Abstract

This Work consists of Scanning Probe Capacitance measurements made with an Atomic Force Microscope (AFM) tip as an electrode in contact with two different materials. In the first part we used a Gallium Arsenide wafer as sample composed with layers of different doping concentrations previously defined by simulating capacitance curves. These capacitance measurements were performed with Schottky and MOS junctions. The second part consists of measurements performed on a Silicon based solar cell.

We have also measured the capacitance of the same GaAs wafer in the same conditions on a large scale set up (device) which is well understood and easier to describe from the point of view of the Poisson's equation solution and these measurements were used for a comparison with the AFM measurements. Except by the surface impurities (such as oxides and water films) that can influence the capacitance curve behavior in the AFM, in the Schottky case, no significant differences between the AFM and the device measurements were found. On the other hand, in the MOS case, the capacitance curve behavior is completely different in both set ups (AFM and device). In the large scale set up, at 1kHz, no low frequency behavior is presented. On the other way around, the capacitance curve measured with the AFM tip presents a low frequency characteristic for measurements performed with frequencies up to 20kHz. The believed reason for

this unexpected behavior is the spherical symmetry of the electrical field produced by the AFM tip, the high density of minorities right below the oxide/wafer interface due to the surface states of GaAs and the charges contained in the oxide that help attracting the minorities carriers to the surface. The cutoff frequency for this low frequency behavior of the capacitance has been estimated to be 3,85 kHz and the results of these measurements in the GaAs-MOS capacitor in the AFM will be submitted for publication in specialized scientific journals.

In the second part of this work, in chapter 5, we performed capacitance measurements along a Si p-n junction and, observing the change of behavior of the capacitance curves that go from high (while the tip was set in the p-type neutral bulk) to low frequency (as the tip approaches the space charge region of the junction), we were able to determine that the electrons diffused from the n-type approximately 288nm inside of the p-type Si (space charge region). From those measurements, we could also estimate the doping profiles of each Si type.

Acknowledgement

I would like to thank all my loved ones for the support I have had during this period of work. I know I was never alone.

I would also like to thank Prof. Eisenmenger and all who were involved in this project. Specially, Prof. Juergen Smoliner and Dr. Wolfgang Brezna for the time they always made their vast experience in Semiconductor Physics available during the long discussions we have had since the beginning of the project still with the design of the crystal wafer.

Chapter 1

Introduction

Richard Feynman, on his famous speech on December 29th 1959 at the annual meeting of the American Physical Society at the California Institute of Technology (Caltech)-*There's Plenty of Room at the Bottom An Invitation to Enter a New Field of Physics*-, did more than just throwing creation seeds to the minds of the new generation. He, indeed, proposed a whole new field of science. A new direction to go.

> "I would like to describe a field, in which little has been done, but in which an enormous amount can be done in principle. This field is not quite the same as the others in that it will not tell us much of fundamental physics (in the sense of, "What are the strange particles?") but it is more like solid-state physics in the sense that it might tell us much of great interest about the strange phenomena that occur in complex situations. Furthermore, a point that is most important is that it would have an enormous number of technical applications. What I want to talk about is the problem of manipulating and controlling things on a small scale.
>
> As soon as I mention this, people tell me about minia-

> turization, and how far it has progressed today. They tell me about electric motors that are the size of the nail on your small finger. And there is a device on the market, they tell me, by which you can write the Lord's Prayer on the head of a pin. But that's nothing; that's the most primitive, halting step in the direction I intend to discuss. It is a staggeringly small world that is below. In the year 2000, when they look back at this age, they will wonder why it was not until the year 1960 that anybody began seriously to move in this direction.
>
> **Why cannot we write the entire 24 volumes of the Encyclopedia Brittanica on the head of a pin?"**

It took about another 21 years until mankind was presented to the so called "nanoworld" through the invention of the Scanning Tunneling Microscope (STM) by Gerd Binning and Heinrinch Rohrer at the IBM Labs in Zurich. For the first time in History, we were allowed to see surfaces features smaller than an atom. An example of how the STM is powerful and precise are the works of art made of single atoms on a surface such as the famous IBM logo made with Xenon atoms on a Nickel surface and the Quantum Corral where "they have positioned 48 iron atoms into a circular ring in order to "corral" some surface state electrons and force them into "quantum" states of the circular structure. The ripples in the ring of atoms are the density distribution of a particular set of quantum states of the corral. The artists were delighted to discover that they could predict what goes on in the corral by solving the classic eigenvalue problem in quantum mechanics – a particle in a hard-wall box"[3]. More example of this "artistical" use of the STM can be found in the same reference.

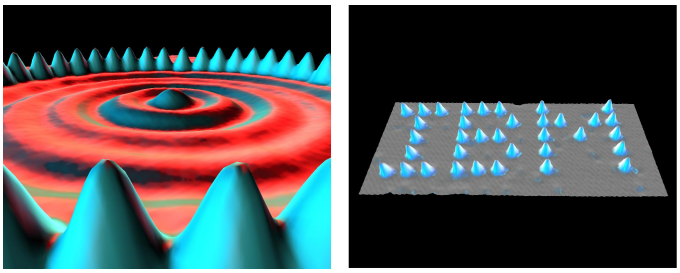

Figure 1.1: The famous Quantum Corral and the IBM logo constructed with the STM. Extracted from the IBM web site [3].

Unfortunately, the STM methodology cannot be used in all materials. The disadvantage of this method is that the scanned surface must be conductive once the readings are based on the electrons that tunnel from the sample to the metal tip. It would not be possible, for example, to scan the surface of an oxide. It took another five years in order to have that difficulty overcome.

Just after receiving the Nobel Prize for the STM invention, Binning came up with the Atomic Force Microscope (AFM) which is able to map the surface of a material via mechanical contact by recording -via a laser circuit system- the vertical displacement necessary to maintain constant force on the cantilevered probe tip -by means of a piezo crystal which can change its dimensions under certain applied voltages- as the tip scans the sample's surface [16].

Almost every surface material can be investigated by the many variations created from the original AFM. Not only the morphology but many other features of interest such as: mechanical, electric, optical, magnetic, thermal and chemical properties. The set of all the methods based on the original AFM is known as Scanning Probe Microscopy (SPM). Examples of some of those applications can be found in the work of Hansma [12], Ludwig [13], Yuanhong [18] and Wadas [17].

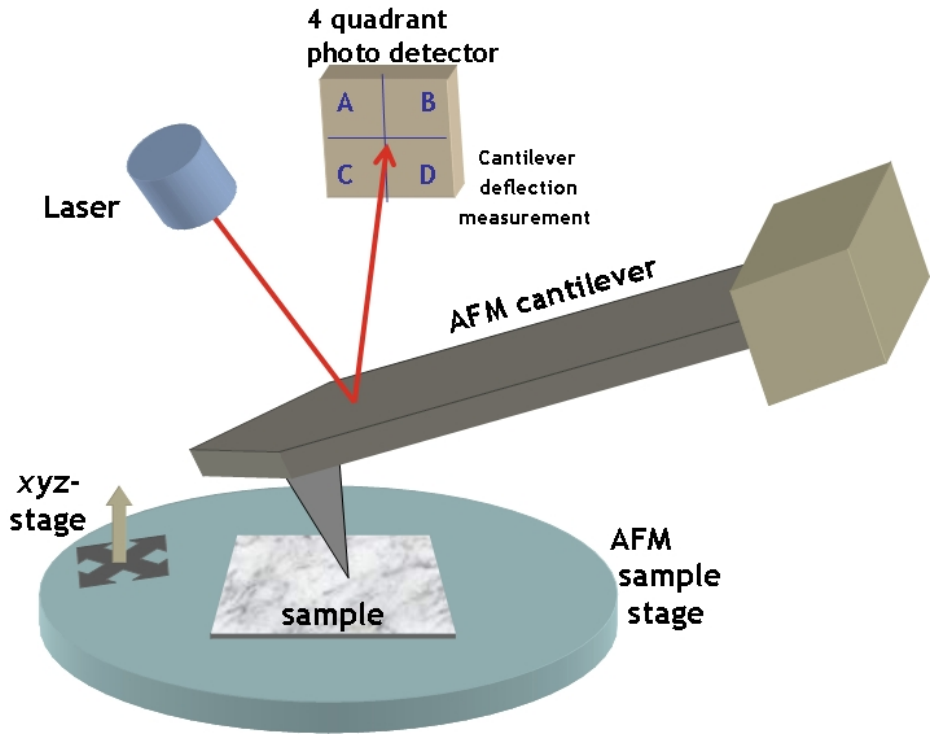

Figure 1.2: AFM basic working scheme. Extracted from Wikipedia [4].

Two special branches that have been created as variation of the AFM are the Scanning Capacitance Spectroscopy(SCS) and Microscopy(SCM). These are the most promising tools for failure analysis and quality control in the semiconductor fabrication[32]. The high resolution due to the small area of the probing tip allows the acquisition of maps (SCM) or capacitance spectra by varying the voltage applied (SCS) of a specific region on the sample.

Scanning Capacitance Microscopy

In 1984, one year before the advent of the AFM, Matey and Blanc -at the RCA labs in Princeton- presented to the world the concept scanning capacitance microscopy (SCM) which was based on a commercial product made for information encoding. The idea was probing the topography of the sample as well as the point to point variation in its dielectric constant. They produced surface images with topographic features of hight 0.3 nm and a lateral resolution of 100 nm. In its original design, the probe consisted of an electrode supported by a diamond stylus which is at mechanical contact with the sample. The capacitance is measured between the probe and the sample below it[10].

The introduction of the AFM in the SCM methodology and the development of sharper and electrically conductive tips allowed a severe increase in the resolution of the capacitance measurements. In the later nineties, the highly coated diamond tips were introduced to solve problems such as abrasion and depletion effects that the first developed tips made with silicon and metal coated material, respectively, suffered. These effects were effectively responsible for many discrepancies on the measurements data.

The diamond coated tip is extremely doped ($10^{20} cm^{-3}$) with

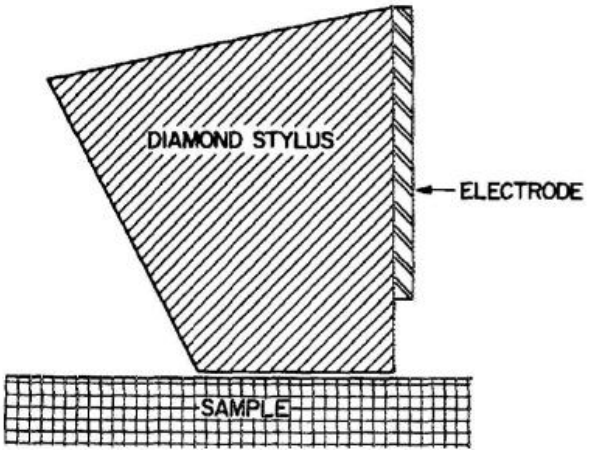

Figure 1.3: Scheme of the capacitance probe where the diamond stylus is used as a carrier for the electrode. The capacitance is measured between the electrode and the sample. Extracted from the work of Matey and Blanc[10].

boron and its area is below the 100x100 nm^2[6]. With this high doping no depletion effect is observed and its diamond coating is tough enough to stand the aggressive pressure up to 100Kbars[11] without being abraded.

The analysis of the capacitance-voltage (CV) characteristics and apparent concentration profile is an attractive non-destructive method for evaluating doping profiles[22]. Even tough, macroscopic capacitance techniques have been developed since the 60s and much of the knowledge acquired along the decades of experience can be used in the new methodology, there are still enormous difficulties in the relatively new SCM/SCS methods. The current state of the art of SCS and SCM can be found in the review articles such as the references [28, 27, 26] and other developments such as measurements at low frequencies, either by electric force based methods detecting higher harmonics in the AFM signal or special sensor circuits can be found in the

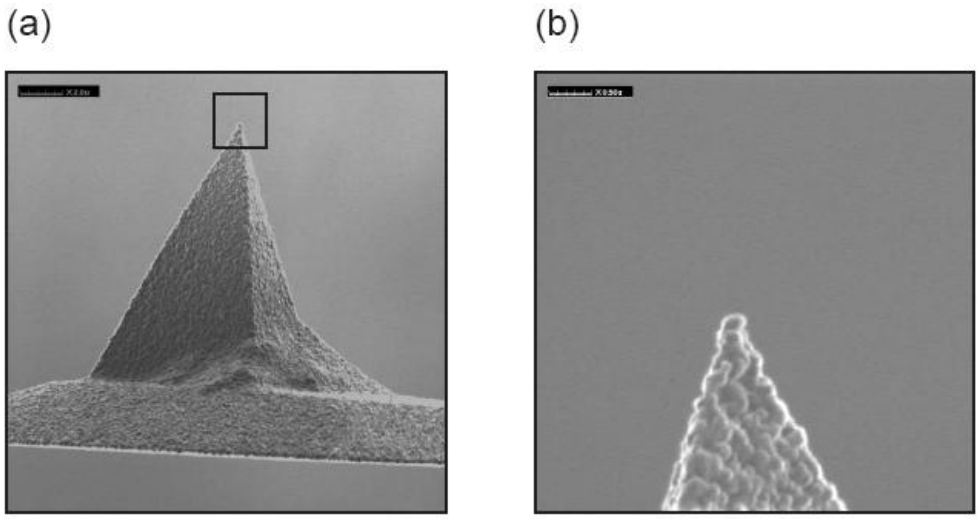

Figure 1.4: (a) Scanning Electron Microscope (SEM) image of a conductive diamond coated force modulation AFM tip (CDT-FMR) commonly used in SCM. (b) A magnification of the tip.

references[23, 24].

Quantitative applications of SCM/SCS still face many technical difficulties such as the change of signal due to tip wear, the magnitude of the measured capacitances -which is in the aF regime ($10^{-18}F$)- and the selection of an appropriate bias to acquire meaningful SCM images. When one proposes himself to execute measurements in this scale, the scanning capacitance microscope does not deliver absolute values for the local capacitance due to the small magnitudes and, hence, calibration curves are needed for a quantitative evaluation. Quantitative and reproducible measurements on SCM/SCS are still barriers to be transposed. An example of quantitative measurements with SCM can be found on reference [27] where Brezna et al. performed capacitance measurements on GaAs based material using a spherical capacitor model because of the tip geometry. Other real challenges for these techniques are on the sample preparation and

on all the physical processes that lead to the contrast on the SCM images which are not yet fully understood.

Despite all the technical difficulties, SCM/SPM have emerged as promising techniques for many applications in the semiconductors industry and for many other scientific areas and is already a reality in the mapping of electrical properties in the nanoscale. It has been already successfully used, for example, to sense doping variations, to deliver high resolution p-n junction delineation and to do investigations on the mobility degradation of carriers[31, 21].

In his famous speech, Feynman thought about having the whole Britannica[1]in the head of a pin. Curiously, we have been figuring out the entry doors of this new world he predicted back in 1960 with the other end of the pin (the AFM tip). The STM and AFM inventor, Binning is now up to the project *Millipede* at the IBM labs, where thousands of AFM probes are put together in arrays to create a new kind of data storage device. The unit will have an astounding density of 155 gigabits/cm^2 ($\approx 19.4 GB/cm^2$) which is enough to store 50 DVDs on something the size of a credit card. Ones and zeros are stored by making microscopic depressions on a polymer film[16]. Considering that the latest *Enciclopaedia Brittanica* has 3.5GB data voluma and that the head of a pin has the surface of $0.095 cm^2$, this new technology would be able to fit fairly half of the volume of data of the *Britannica* on it's head.

Despite all the efforts in the last 40 years of research and if the idea of this project turns into reality, Feynman's "prophecy" would still not be fulfilled. That gives us the exact idea of the enormous proportions of the challenge of going into small scale Physics.

[1]Who is older than the Internet will remember all those heavy books...

Chapter 2

Equipment

2.1 Contact Mode AFM based SCM/SCS

The Atomic Force Microscope (AFM) used in this work is the Dimension 3100 manufactured by DI. The AFM is usually concerned on the sample-probe interaction by measuring the resulting contact forces (eg.: van der Waals and hydrophilic forces caused by films of water on the sample).

The AFM can operate in three different modes as depicted on the figure 2.1: contact, tapping and non-contact. In the contact mode the probe remains static in the permanent contact with the sample surface; in tapping mode, the probe is oscillating and not in permanent contact with the probe and in the non-contact mode, the probe is set to oscillate and the assertions about the surface are made from the attenuation of the oscillating frequency. This mode is not used in the construction of images but it is useful for the study of the forces acting on the surface of the sample.

As it is demonstrated on figure 2.2, the AFM constructs the “picture” of the surface by scanning it with the tip. At the end of the cantilever, right on top of the tip, a laser is shone. This

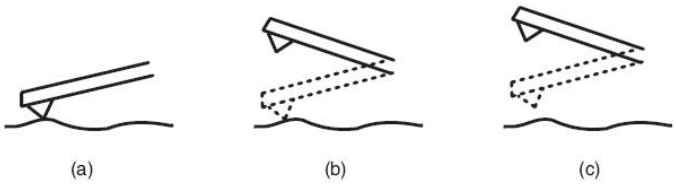

Figure 2.1: Illustration of the AFMs operating modes: (a) contact, (b) tapping and (c) non-contact.

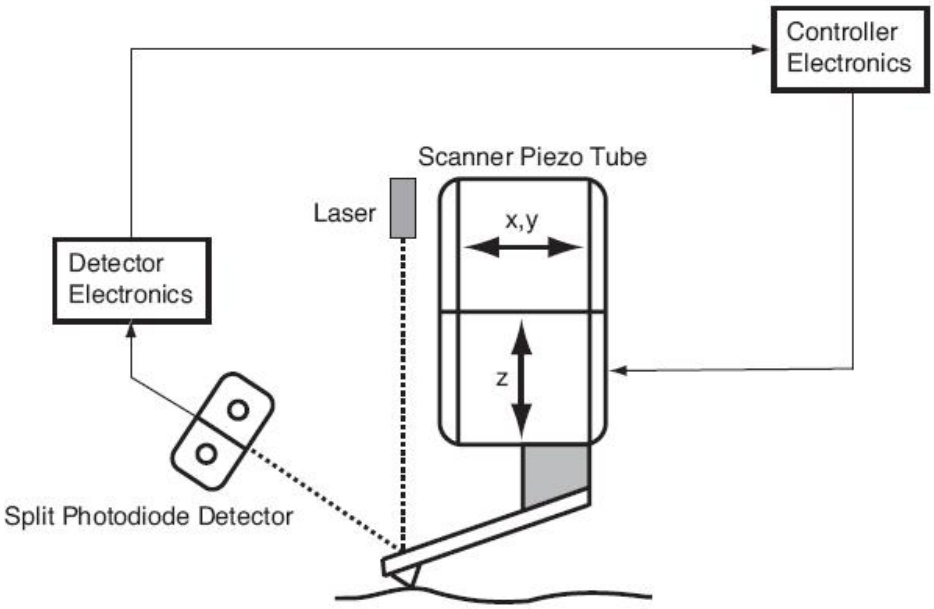

Figure 2.2: Contact AFM principle of operation

laser is reflected from the cantilever to a detector which is able to measure its deflection. This deflection will vary the position of the reflected laser that hits the detector and such variation will describe the saliences of the scanned surface.

For the SCM/SCS measurements, there is the need to establish a contact with the sample in order to apply an electrical potential and, thus, see capacitance effects. The tips used here must be somehow hard once the pressures applied in the contact mode are of the order of 50 kbars and, therefore, the ones we have used are coated with highly doped diamond. Due to this high doping, we can consider the tip a conductor and, in direct contact with the semiconductor, the whole set up can be considered a Schottky Diode or a MOS capacitor depending on the configuration of the sample[1].

In the contact mode the tip remains still on the sample and the cantilever deflection is maintained constant. The deflection stability of the cantilever will be assured by the detection and feedback circuit as it's shown on figure 2.2. As one can see, the reflected beam is detected by the photo-diode detector. Any small change on the deflection of the cantilever[2] will result on a shift of the reflected spot on the detector. With that information, the computer will be able to increase or decrease the voltage on the piezo and, consequently, keep the stability.

The temperature fluctuation is one of the most common influences on the AFM capacitance measurements. The thermal expansion of the whole AFM varies the distance between the tip holder and the sample. As consequence, the stray (background) capacitance, which must be absolutely stable during the measurements, will vary and influence the acquired data. In order to

[1] This will be discussed in details later on.

[2] These changes are of the order of Angstroms.

keep the control over the temperature, the whole AFM machine is set into an insulating hatch. There, the temperature must be controlled within a 10 mK variation. In our case, the waiting time was of at least 6 hours until the system could come to thermal balance and, therefore, the fluctuations on the stray capacitance were small enough to start acceptable measurements.

2.2 The Measurement Set Up

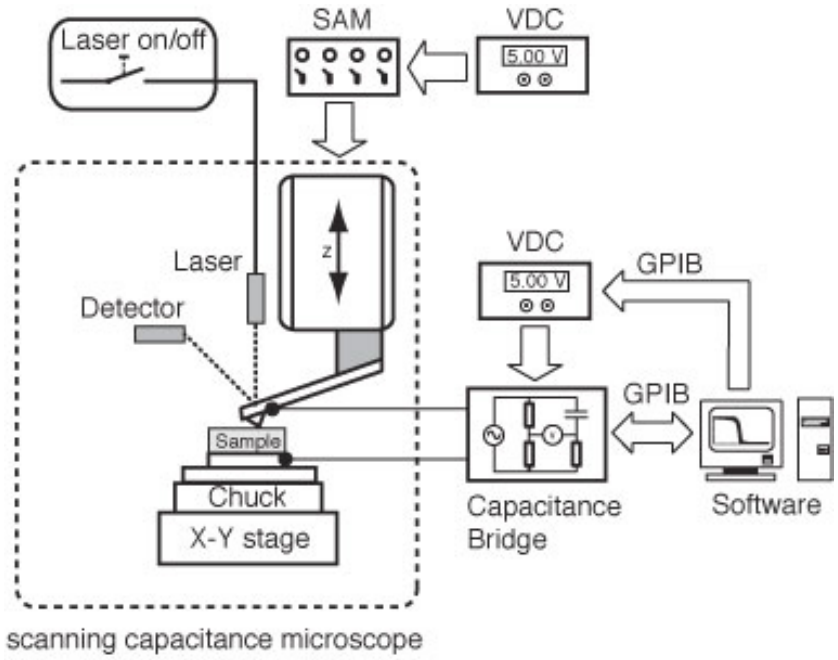

Figure 2.3: The Experimental setup of the SPM - Courtesy of Mathias Schramboeck.

The complete measurement set up can be seen on figure 2.3. The capacitance bridge is directly connected to the tip-sample set. The contact of the sample is made via a cable which is plugged into the sample holder constructed by Smoliner et al. The sample must be stable and, therefore, it is fixed on the vac-

uum chuck as its described on the figure above. In order to establish a good back contact, the sample is binded with silver glue onto a metallic coin which is previously covered with a thin gold layer. A not well made back contact will result in different consequences in the measurement such as: poor quality in the images contrast and difficulty in acquiring quantitative values in the measurement[32]. The external voltage source is connected to the set up through the capacitance bridge and both are controlled by the specific software that runs in the computer attached to the system by a GPIB connection.

Even though the temperature inside the Clean Room where the AFM is located is fairly stable, the temperature variation inside the hood is a drastic point for the successful stabilization of the tip on the sample's surface. Drift would cause undesirable change on the acquired data and, hence, their reproduction turns out to be impossible. The temperature must be set[3] and its variation must be minimized down to the neighborhood of $10\mu K$. To achieve this balance the temperature must be regulated by a duo thermometer-heater.

One specific detail in this AFM configuration is the external control of the piezo voltage and the laser on/off mechanism which are in direct connection with the AFM controller.

The Laser ON/OFF Machanism

One remarkable change made in the AFM used in this work by past researchers who contributed to the development of these measurement techniques is the automatic switch off and turn on of the laser during data acquisition. They have realized that problems on trustable numbers in their very first capacitance readings

[3] In out case it was 36°C

were caused by the incidence of the laser on the sample during the measurements and, therefore, causing unexpected effects that compromised the quality of the data they were reading.

It is believed that the laser was influencing the creation of the minority carriers in the sample which caused these undesired change on the capacitance readings (optical pumping)([33] and also review articles can be found in references[14, 15]). An example of the laser influence can be seen on figure 2.4.

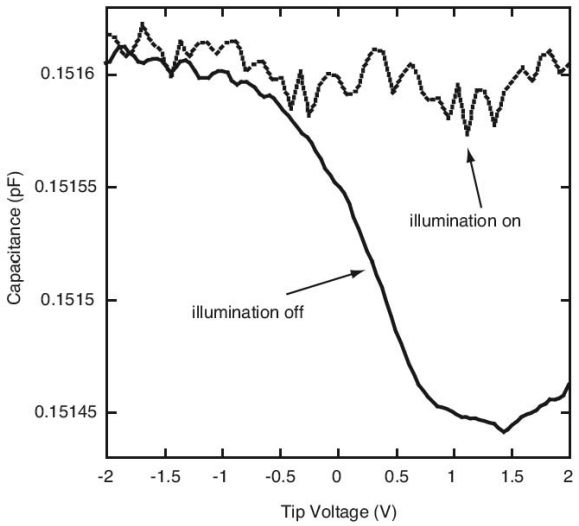

Figure 2.4: Laser influence on the SCS. Coutesy of Mathias Schramboeck[33].

However, the laser is the responsible element for the cantilever deflection once the voltage that controls the piezo is influenced by the correct reading of the signal reflected on the top of the cantilever by the internal controller electronics. The interruption of this feedback circuit by turning the laser off will make the system “think” that the cantilever is strongly bent because the reflection of the laser is not illuminating the detector and, consequently, in order to react to the cantilever deflection and detect the reflected signal again, the piezo controller will apply its max-

imum/minimum voltage(±200V). This situation could cause unwanted damage to the sample and the solution for this obstacle turned out to be an external voltage applied to the piezo via the Signal Access Module (SAM) developed by the Smoliner Group (figure 2.3) which bypasses the internal circuitry of the AFM while the laser is turned off.

2.3 The Capacitance Bridge

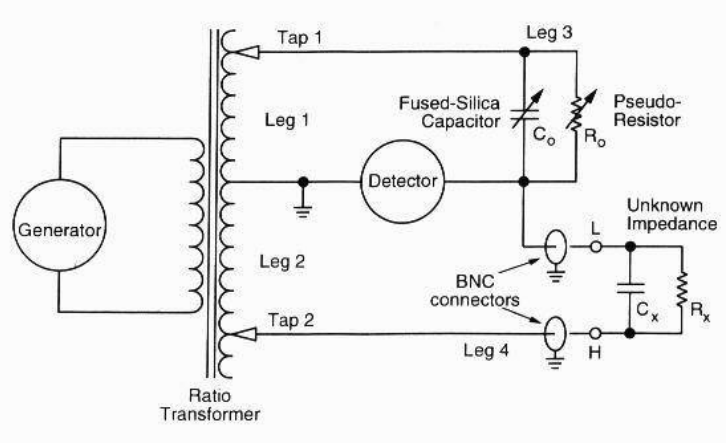

Figure 2.5: Bridge Circuit - Extracted from the user's manual [2]

We ran the experiments using two different capacitance bridges manufactured by Andeen Hagerling: the AH2550A and the AH-2700A. Their functionality is basically the same and the only significant difference between them is that the latter works in various frequencies.

These bridges "incorporate a *true bridge* in the conventional sense of the word"([2], pp.4-1). The extreme high accuracy and precision are provided by the specially-wound ratio transformers and a temperature-controlled fused silica capacitor in the basic bridge circuit.

The sine wave generator excites the ratio transformer that forms legs 1 and 2 of the basic bridge . Both legs have many transformer taps that allow the precise selection of the voltages to drive the third and fourth legs of the equipment. The construction of the third leg is based on several fused-silica capacitors and some other circuitry that simulates a stable resistor. On the other side, the leg number 4 is the unknown impedance. The bridge's internal computer is responsible for balancing taps 1 and 2 of the transformer and selecting the best values for C_0 and R_0 so that the voltage in the detector is at its minimum. It is able to detect both in-phase and quadrature voltages in relation to the generator voltage. This makes it possible for both resistive and capacitive components of the unknown impedance to be balanced separately. As long as the internal computer of the bridge is able to determine the minimum voltage, the unknown capacitance will be determined, since the ratio of the unknown capacitance (C_x) to C_0 is the same as the ratio for the voltage on tap 1 to the voltage on tap 2.

The Averaging Time

The Averaging time is the parameter that controls the reduction of the effects of random noise by internally averaging the noise over a period of time. Any high gain amplifier (such as the one connected in the LOW terminal of the bridge) generates random noise at its input. This noise produced by the amplifier is unavoidable and is the reason for providing control over the averaging time. Another reason is that the externally generated noise can be extremely reduced by averaging if it has random nature[2].

Noise will cause the measurements taken with short averaging time to fluctuate more than the ones taken over a longer period.

When the noise's nature is purely random, the variation in the measurements will be inversely proportional to the square root of the time period in which measurements were done.

Nevertheless, this is only true for small changes in the unknowns value. Larger changes will require the selection of a different ratio transformer tap which may cause the measurement to be restarted or aborted.

2.4 GaAs: The object of the study

GaAs is a III-V[4] compound semiconductor that was created by Goldschmidt in the 1920s but the first publications about this material appeared just in the 1950s. Years of intensive research have evolved into a low volume prototype production in the past decades. Nowadays, due to the establishment of reliability and the relative low production cost, the manufacturing of GaAs devices and monolitic integrated circuits has been consolidated. It is now firmly entrenched as a production technology and its reducing costs meet the exponentially growing demand for GaAs based devices[8]. An extensive source of GaAs facts can be found on reference [34]. On the other hand, GaAs does not have a native oxide that "passivates" the wafer and this makes the production of MOS devices with GaAs to be not so direct as it is with silicon.

GaAs presents some technical advantages when compared to silicon ([8] pgs. 17-20 and [5]):

- Its higher electron mobility and saturated drift electron velocity allow the electrons to move faster in the GaAs than

[4]Ga and As are elements from the III and V columns of the periodic chart, respectively.

in Silicon. Which means that transistors made with GaAs can operate in higher frequencies than the ones made with silicon(up to 250 GHz).

- The devices based on GaAs also generate less noise as silicon devices when operating at high frequencies.
- GaAs presents higher resistivity than silicon which makes the device isolation an easier task. It makes GaAs an ideal substrate for the construction of monolithic integrated circuits.
- GaAs devices are also tougher against radiation.
- Differently from silicon it has a direct band gap which means that the probability of photon emission or absorption during an electron transition from valence to conducting band is increased.

These properties qualify GaAs as a good option for optical, aerospace and telecommunication applications.

Chapter 3

One Dimensional Schottky and MOS

In this work we performed systematic measurements with the AFM tip in direct contact with the GaAs crystal or with a layer of oxide insulator on top of it. Once the AFM tip is highly doped, it can be considered as a conductor and, therefore, the sets AFM tip-semiconductor and AFM tip-oxide-semiconductor can be treated with the theoretical background of the Schottky Diode and the MOS Capacitor respectively.

Even though for the complete AFM capacitance measurements understanding, one needs at least a 2 dimensional analysis, in the following sections we will develop the most important concepts used in our work for the Schottky and MOS cases in one dimension which are still analytically treatable.

Nevertheless, we have also developed measurements in large devices in which the following conclusions are totally valid once the differential equations of the electrostatics can be reduced to a one dimensional problem with great success in their cases.

The content of this chapter is standard semiconductor theory and it can be seen in richer details in references [20] and [19].

For the complete analysis for the MOS capacitor, the reference [25] is recommended. For Solid State Physics, reference [1] is the standard literature.

3.1 Metal Semiconductor Contact

When a metal is brought in contact with a semiconductor, in order to achieve the thermodynamical balance, a transfer of charge carriers takes place. In the n-type semiconductor case (which is the case treated in our experimental montage), electrons at a higher energy level flow towards the metal until the balance is achieved, i.e., their chemical potentials (Fermi levels) are equalized. The drained electrons leave behind a layer of positive ionized donors and this particular extension is known as the depletion layer. The net positive charge of the ionized donor atoms create a negative field that bends upwards the band edges of the semiconductor. This bending gives rise to the so called built in potential (fig.3.1).

If a positive voltage (forward bias) is applied in the metal-semiconductor junction, the Fermi level of the metal is lowered with respect to the Fermi level in the semiconductor. As consequence, the built in potential barrier will be lowered; more electrons will be able to overcome it and, therefore, diffuse directly to the metal forming a current. If a negative voltage is applied (reverse bias), the Fermi level of the metal will be raised in relation with the Fermi level of the semiconductor. Consequently, the built in potential and the depletion zone become larger and almost no current will flow. These are the characteristics of the metal-semiconductor junction diode (Schottky Diode).

The electrostatic analysis of the electric field formed in the depletion zone due to the charge separation will provide more input

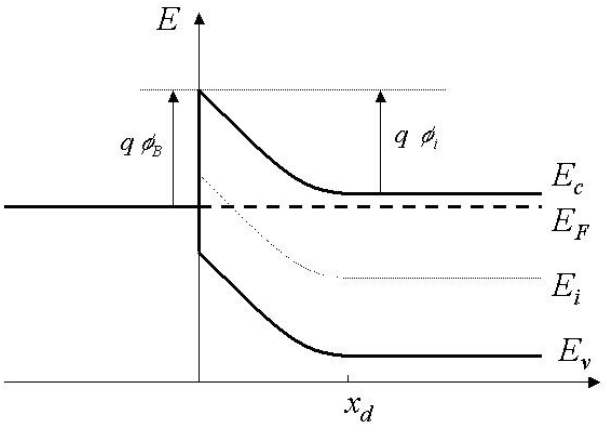

Figure 3.1: Energy band Diagram for the n-type semiconductor where ϕ_t is the built in pontential, ϕ_b is the barrier height, x_d is the depletion zone length and E_c, E_F, E_i and E_v are the energy levels of the conduction band, Fermi level, intrinsic level and valence band of the semiconductor, respectively. Figure extracted from [19].

about the characteristics of the diode such as charge concentration and doping level. These features can be determined by the capacitance-voltage characteristics of the diode.

3.1.1 Capacitance of the Schottky Diode in One Dimension

We calculated the depletion zone width for the one dimensional case considering the full depletion approximation, i.e, $\rho \approx qN_d^+$ for $x \leq W$, $\rho \approx 0$ and V constant for $x \geq W$, where W is the depletion zone width, ρ is the charge density and N_d^+ is the ionized donor impurities density. After solving the Poisson equation for the charge distribution in the semiconductor

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_s},$$

we can express the depletion layer width as:

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V - \frac{kT}{q})}{qN_{\mathrm{d}}}} \tag{3.1}$$

where V_{bi} is the built in voltage, V is the applied potential and $\frac{kT}{q}$ is the thermal energy per unit of charge of the majority carriers.

We acquire the expression of the capacitance per area using its definition ($C = \frac{dQ}{dV}$) and the expression 3.1. Once $dQ = qN_d^+ dW$, then

$$C = qN_d^+ \frac{dW}{dV}$$
$$C = \frac{\varepsilon_s}{W} \tag{3.2}$$

which is exactly the capacitance expression for the simple case of the classical parallel plates capacitor.

3.2 The MOS Capacitor

The Metal-Oxide(insulator)-Semiconductor system has been described as a voltage dependent capacitor in 1959 by John Moll, who, at Stanford, proposed it for the first time as a circuit element. The first MOS capacitors were very simple but, still, they were a very powerful structure. They consisted of a piece of silicon which had a layer of SiO2 (insulator) grown on its top and, finally, a thin metal layer topping everything[7] (please see figure **??**). Due to its various applications, the MOS systems have played a fundamental role in the modern electronics industry. They are applied mainly as MOSFET (MOS Field Effect Transistors) or flash memory devices and in CCD (Charge Coupled Devices)[32].

In our measurements with the Scanning Capacitance Microscope, we consider the system composed by the highly doped tip, the oxide layer and the GaAs sample as a MOS capacitor. Even though this system can no longer be an approximated one dimensional case, our digression in the simplest case will be helpful to interpret our results.

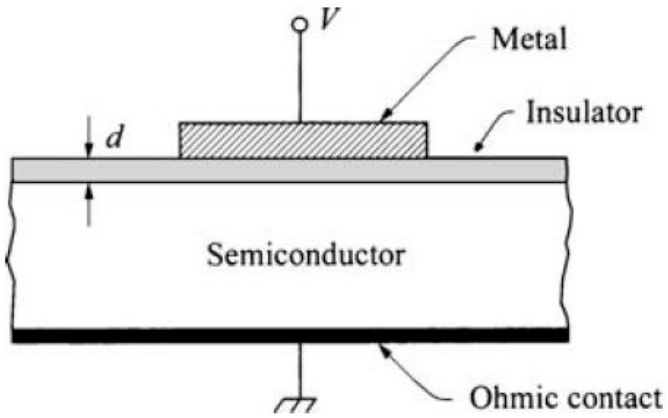

Figure 3.2: Metal Insulator Semiconductor Capacitor

The MOS system is described as 2 capacitors in series: the oxide and the semiconductor itself. Once the system as a whole is neutral, the concentration of charges in the metal gate (AFM tip) must be equal in modulus to the net charge deposited below the insulator. It follows that

$$Q_m = Q_s \tag{3.3}$$

where Q_m and Q_s are the charge density in the gate[1] and in the semiconductor, respectively.

The conservation of energy urges that the total voltage applied on the MOS capacitor will be composed by the voltage applied on the insulator (V_i) and the voltage applied on the semi-

[1]Gate is the technical term for the metal contact on top of the MOS capacitor.

conductor (V_s). Thus

$$V = V_i + V_s \tag{3.4}$$

The field inside the (ideal) insulator is related to V_i by

$$V_i = E_i d = \left(\frac{Q_s}{\varepsilon_i}\right) d \equiv \frac{Q_s}{C_i}. \tag{3.5}$$

Clearly, the capacitance of the insulator is constant and is given by

$$C_i = \frac{\varepsilon_i}{d} \tag{3.6}$$

for a given insulator width "d". The capacitance "C_s"of the semiconductor is the interesting one and will vary with the applied voltage on the Metal contact (AFM tip).

Finally, after these considerations, we can use the classical expression for the addition of capacitors in series to describe the total capacitance of the MOS system

$$C_{MOS} = \left(\frac{1}{C_s} + \frac{1}{C_i}\right)^{-1} \tag{3.7}$$

where C_s is the semiconductor capacitance and will be given by $C_s = \frac{dQ(V_s)}{dV}$.[2]

During Operation, the MOS capacitor will present 3 modes: ACCUMULATION, DEPLETION and INVERSION[3]:

- **Accumulation** occurs when the voltage ($V_g > V_{fb}$) applied on the gate attracts the major carriers in the direction of the oxide layer.

[2] However, this differential definition for capacitance will be a good approximation only if the AC excitation voltage used to determine the capacitance (please see section 3.2.2) is small compared to the applied DC voltage which is the actual gate voltage.

[3] When no voltage is applied, once we are here treating the ideal case where there is no leakage of current through the insulator and the work function difference between the gate and the semiconductor is disregarded, the energy bands of the semiconductor are left flat (*flat band voltage* (V_{fb}))

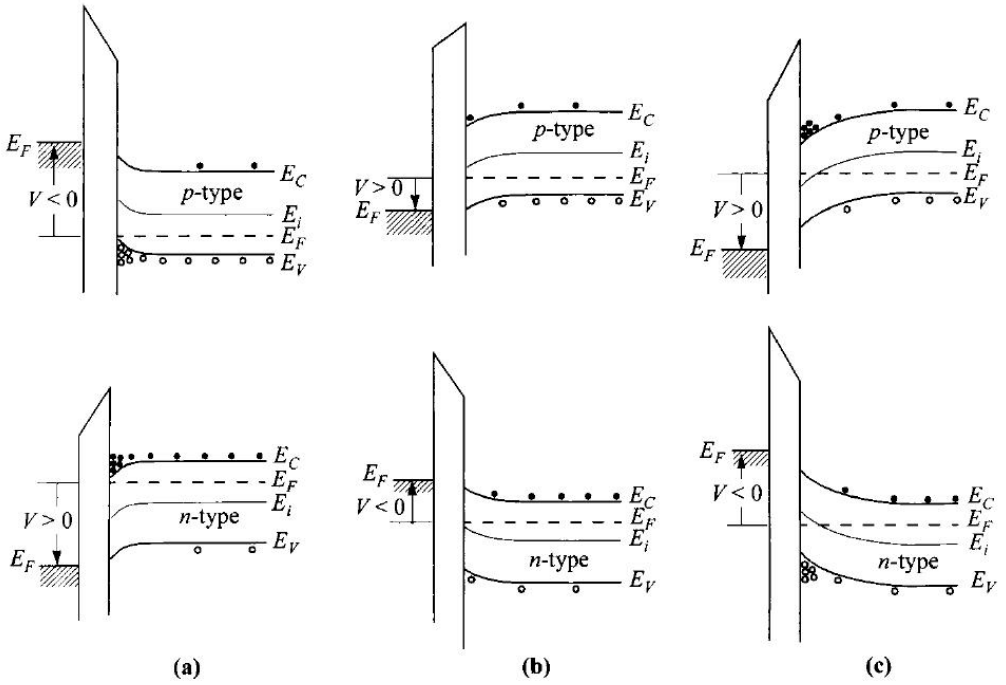

Figure 3.3: Energy Band Diagrams for Ideal MOS Diodes for a non zero voltage in the following cases: (a) accumulation; (b) depletion; (c) inversion. Here V is the applied voltage and E_c, E_F, E_i and E_v are the energy levels of the conduction band, Fermi level, intrinsic level and valence band of the semiconductor, respectively. Figure extracted from reference [20].

- **Depletion** will occur when a reverse bias ($V_g < V_{fb}$) is applied and, therefore, the majority carriers are repelled to the opposite direction.
- **Inversion** will be observed after a *Threshold Voltage* is reached in the depletion regime where the minority charge carriers will be attracted to the interface by the gate bias. At this point, the band is bent in such a way that the intrinsic level crosses over the Fermi level.

3.2.1 Solution of the Poisson Equation

In order to develop a theoretical model for the MOS case, we will consider that the system has a quasi-static development and, therefore, we will be able to apply classical electrostatic theory.

The electron and hole concentrations as a function of the applied voltage are:

$$n = n_0 \exp(qV_s/kT) \tag{3.8}$$

$$p = p_0 \exp(-qV_s/kT) \tag{3.9}$$

Where n_0 and p_0 are the equilibrium densities of electrons and holes, respectively. The potential V_s as function of the position in the semiconductor can be calculated after solving the one-dimensional Poisson equation

$$\frac{d^2V_s}{dx^2} = -\frac{\rho}{\varepsilon_s} \tag{3.10}$$

where $\rho = q(N_d^+ - N_a^- - n + p)$ and N_d^+ and N_a^- are the doping concentrations for donors and acceptors, respectively. In our case, once we deal only with a n-type semiconductor, we set $N_a^- = 0$.

If we claim that deep in the bulk there is charge neutrality, hence, no potential is felt and $\rho = 0 \rightarrow N_d^+ = n_0 - p_0$. Finally, we will have:

$$\rho = q(N_d^+ - n + p) \tag{3.11}$$

$$= q[n_0(1 - e^{\frac{qV_s}{kT}}) - p_0(1 - e^{\frac{-qV_s}{kT}})] \tag{3.12}$$

After these considerations, the Poisson equation to be solved will be:

$$\frac{d^2V_s}{dx^2} = \frac{q}{\varepsilon_s}[p_0(1 - e^{\frac{-qV_s}{kT}}) - n_0(1 - e^{\frac{qV_s}{kT}})]. \tag{3.13}$$

If we multiply both sides by $\frac{dV_s}{dx}$ and use the chain rule from calculus, we will be able to express the electrical field E_s as function of the potential after integrating the Poisson equation from the bulk to the surface of the crystal:

$$E\left(V_s, \frac{n_0}{p_0}\right) = \pm\frac{\sqrt{2}kT}{qL_d}F\left(\frac{qV}{kT}, \frac{n_0}{p_0}\right) \tag{3.14}$$

Where the L_d is the Debye length for the holes:

$$L_d = \sqrt{\frac{kT\varepsilon_s}{q^2 p_0}} \tag{3.15}$$

and

$$F(\frac{qV_s}{kT}, \frac{n_0}{p_0}) = \sqrt{(e^{(-\frac{qV}{kT})} + \frac{qV_s}{kT} - 1) + \frac{n_0}{p_0}(e^{(\frac{qV_s}{kT})} - \frac{qV_s}{kT} + -1)}$$

(3.16)

Now, using again the Poisson equation and the fact that the electric field is given by $E = -\frac{Q}{\varepsilon_s}$, where Q is the total charge, we will deduce the areal capacitance density. Applying the operator $\frac{d}{dV_s}$ on the electric field expression leads to

$$\frac{dE}{dV_s} = \frac{\frac{dQ}{dV_s}}{\varepsilon_s} \tag{3.17}$$

$$= \frac{C_s}{\varepsilon_s} \tag{3.18}$$

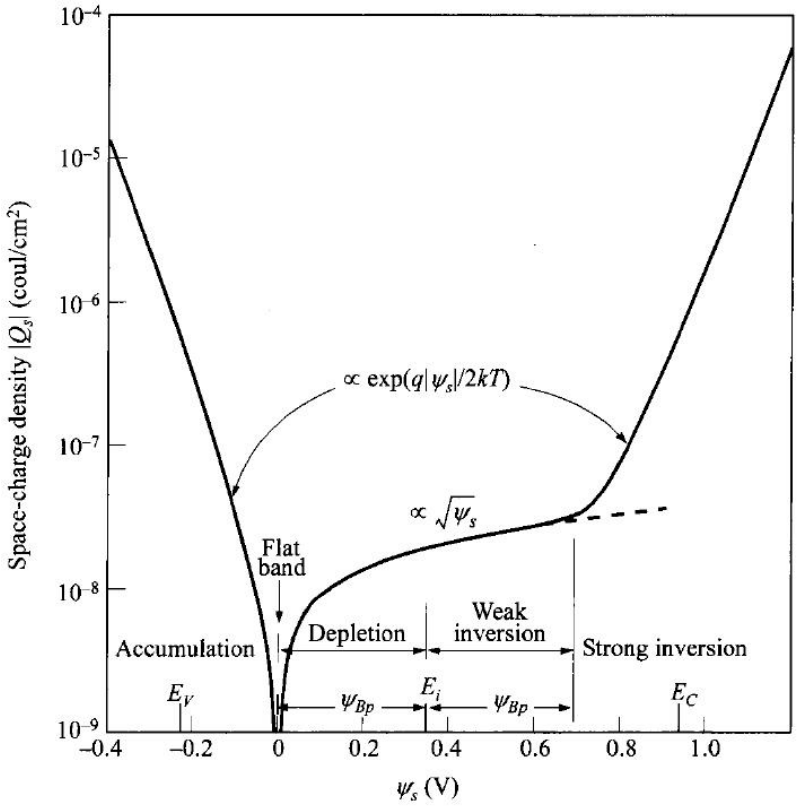

Figure 3.4: Variation of the space-charge density ($Q_s = E\varepsilon_s$) in the semiconductor as a function of the potential for a p-type silicon at room temperature. $\psi_s(V)$ corresponds to the voltage in the semiconductor $V_s(V)$. Figure extracted from reference [20]

.

Back to the Poisson equation:

$$\frac{d^2V_s}{dx^2} = \frac{dE}{dx} \tag{3.19}$$

$$= \frac{dE}{dV_s}\frac{dV_s}{dx} \tag{3.20}$$

$$= \frac{C_s}{\varepsilon_s}E \tag{3.21}$$

$$= \frac{\rho}{\varepsilon_s} \tag{3.22}$$

$$\tag{3.23}$$

Then, finally, we have the capacitance density as function of the applied potential:

$$C_s(V_s) = \frac{\rho(V_s)}{E(V_s)}. \tag{3.24}$$

The combination of equations (3.4), (3.6), (3.7) and (3.24) will describe the ideal (normalized by C_i) MOS capacitance curve as shown in the figure 3.5.

3.2.2 High and Low Frequency influence on the CV curve

If we take a closer look on the C(V) curve of figure 3.5, we can easily identify the operational modes of the MOS capacitor.

At the negative voltages, there is the accumulation of majority carriers under the oxide surface and the capacitance is at its maximum (C_i). Then the capacitance starts to decrease as the voltage becomes larger. In this regime, the end of the semiconductor covered by the oxide is depleted of the majority carriers until the minimum of capacitance is reached. And, finally, in the inversion regime, the last part of the curve will show us an interesting feature of the MOS capacitor: depending on the frequency of the small ac voltage used in the capacitance measurement, the curve will stay at its minimum or go up again.

The reason for this effect can be credited to the generation-recombination rate of the minority carriers, i.e. the total net charge density given by the minorities, and also by their generation response time to the applied ac signal (voltage perturbation). If the frequency is low enough, the creation rate of the minorities will be able to “follow” the signal and the density of minority carriers is increased. As consequence of charge neutrality, the cloud of minorities next to the insulator will screen completely the depleted majority carriers and be “felt” in the capacitance measure-

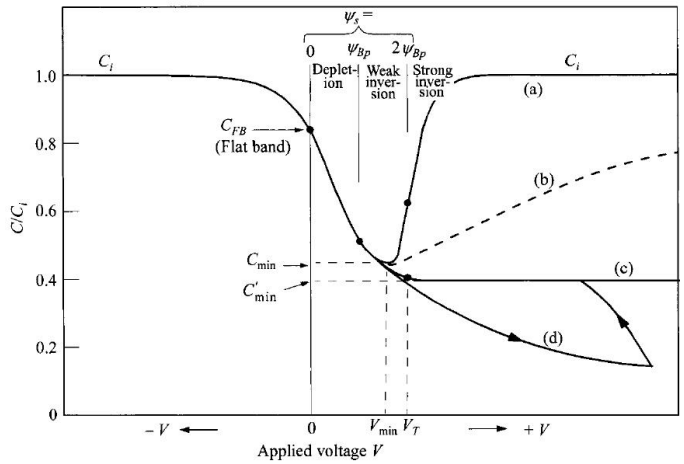

Figure 3.5: MOS capacitance-voltage curves. (a) Low Frequency. (b) High Frequency. (c) Deep Depletion. Extracted from reference [20]

ment. On the other way around, if the frequency is too fast to the point that the minorities creation rate cannot respond to the small perturbation, charge neutrality will not be maintained anymore. There will be no screening (or at least not total screening of the field) and the fast depleted majority carriers will quickly respond going further down away from the insulator inside the crystal. As result, the depletion zone will grow and the depleted majority carriers will be felt in the capacitance measurements.

Another way to see the same picture is: if the frequency is high or low for a measurement will be determined by how large the minority carriers density is in order to keep charge neutrality with the gate and, consequently, screen (hide) the electric field from the majority carriers. This density can be altered by the temperature of the environment, the illumination or even the geometry in which the problem is treated[4]. As an example, we can cite the work of Yang *et al* [30] where capacitance measurements

[4]This will be discussed more in details in the chapter 4.

with a MOS GaAs based device were performed in different illumination conditions at a constant frequency of 1 kHz and both low and high frequencies curves could be observed.

The high frequency curve can be obtained using an approach where the Fermi Level E_f is replaced by the minorities *quasi-Fermi Level* E_{fn}[5] which takes into account the level of occupancy on the conduction band so the net minorities density is kept constant, independent of the AC voltage applied.

We present here a short summary of the solution of the Poisson Equation which can be looked in details in reference [25]. For the case of a p-type semiconductor at not so low temperatures, the electron density will be given by

$$n = n_i e^{v(x,t)+u_{Fn}(t)} \tag{3.25}$$

where $v_s(x,t) = (kT/q)V_s$, $u_{Fn} = (E_{Fn} - E_i)/kT$ and the charge density is given by $\rho = q(p - N_a - n)$.

Now, solving the Poisson equation

$$\frac{d^2 v_s}{dx^2} = \frac{1 - e^{-v} + e^{v+u_{Fn}+u_B}}{{L_d}^2} \tag{3.26}$$

with the assumptions above, where the electrons redistribution response to the AC voltage in the vicinity of the semiconductor surface ($x = 0$) has been taken into account, we will be able to express the electric field ($E_{x=0} = \frac{dv}{dx})_{x=0}$ by integrating once. Using $C_s = \varepsilon_s \frac{dE_{x=0}}{dv}$, we come to an expression for the capacitance:

$$C_s = \frac{\varepsilon_s}{L_d} \frac{1 - e^{-v_s} + (\frac{n_i}{N_a})^2 [(e^{v_s} - 1)(1 - \frac{\delta u_{Fn}}{\delta v_s} + 1)]}{\sqrt{2[(e^{v_s} - 1)e^{u_B - u_{Fn}} + v_s + e^{-v_s} - 1]}} \tag{3.27}$$

[5] As the total number of minority carriers is fixed, the level to which the inversion layer is filled is described by the quasi-Fermi Level.

where $\frac{\delta u_{Fn}}{\delta v_s} = \frac{1}{1+\Delta}$. The derivation of the expression for Δ is beyond the scope of this discussion. Nevertheless it can be found in the Appendix V of reference [25].

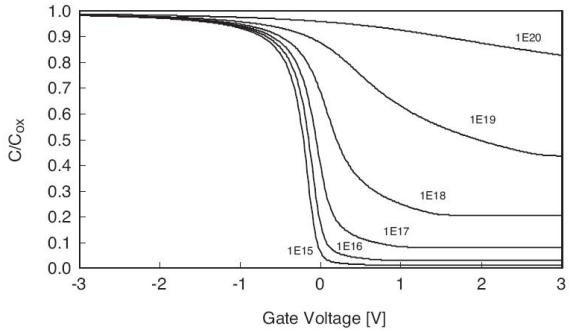

Figure 3.6: Normalized high frequency capacitance for different dopping concentrations. Extracted from reference [33].

As one can see on the figure 3.6 where the capacitance is displayed for varied doping concentrations, the main differences can be seen in the inversion regime. Another important characteristic that can be observed is that in the depletion regime, for higher doping levels, a higher gate bias is needed in order to reach to the minimum of the curve. This can be understood in the same fashion as in the Schottky contact case[6], if one takes a closer look on equation 3.2 where the capacitance is directly proportional to the square root of the doping concentration.

[6]Where the minority carriers are not active in the capacitance curve once they flow to the metal contact and are felt as leakage current.

Chapter 4

Experimental Data and Discussion

In this experimental work a multilayered Gallium Arsenide structure has been investigated as a Schottky diode and as a MOS capacitor in the AFM and also as a regular macroscopic device. For the many measurements we have performed, we have used a MBE grown multilayered n-type GaAs structure as sample. Each layer's Si doping level and thickness has been decided based on a Schottky contact simulation[1] for the one dimensional case disregarding minorities and the diffusion of electrons in the junctions between layers. As result, we decided that the following configuration would be worth it investigating and analyzing the results a layered structure could show when the capacitance is measured with the AFM. The following table presents the layers structure, thickness and doping level of GaAs crystal we have researched.

[1] See equation 3.2.

Layer (Substrate → *Surface*)	Thickness (nm)	Doping (Si)(cm^3)
Substrate n+	350μm	10^{18}
Si: GaAs	200	10^{15}
GaAs	200	–
Si: GaAs	200	10^{16}
GaAs	200	–
Si: GaAs	100	10^{17}

Table 4.1: Wafer Doping Configuration

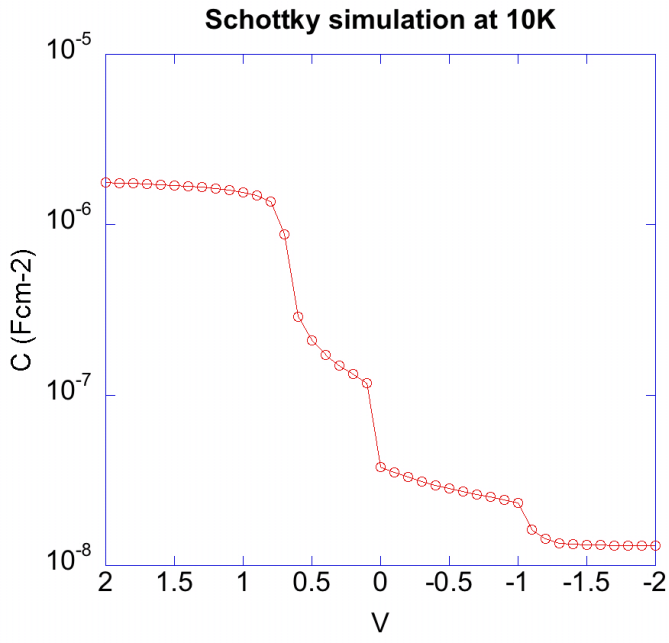

Figure 4.1: Simulation of the C(V) curve expected for our GaAs sample - The simulator is a courtesy from Greg Snider [35].

The device production is standard. For the Schottky case, we have evaporated a thin aluminum strip along its surface inside of a vacuum chamber using a shadow mask. In the MOS case, the insulator aluminum oxide (Al_2O_3) has been grown via *Atomic Layer Deposition* on top of the wafer and, afterwards, we evaporated -in the same fashion as for the Schottky diode- the aluminum contact (gate). The device contact is much larger than the AFM tip on the wafer and, hence, more current is able to flow. For that reason, we applied a thicker insulator for the minimization of the current leakage. The oxide thickness used in the device was 10nm and in the AFM set up it was 3nm.

Once the doping profile techniques and the MOS capacitor theories for the device are well understood, it was used as a comparison for the results of the AFM set ups. For both devices, we ran capacitance measurements with varied temperature regimes in order to establish the temperature dependence of the capacitance. In all the AFM measurements, the temperature was kept constant at (36 ± 10^{-2})°C. For the MOS measurements made in the AFM, the frequency dependence has been tested[2].

[2]All the other measurements were executed with the capacitance bridge frequency at 1kHz.

4.1 The Schottky Diode

4.1.1 Device Measurements

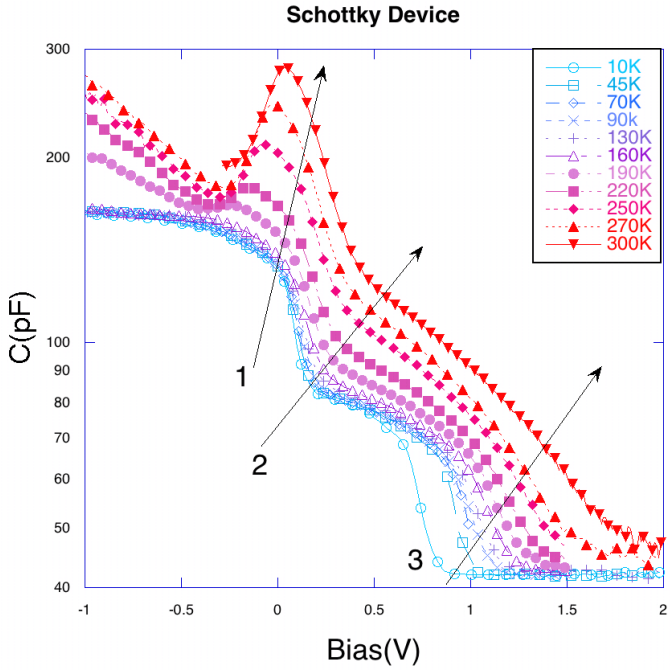

Figure 4.2: Temperature dependence of the capacitance curve of the device.

Figure 4.2 displays the results from the capacitance measurements we have performed on the GaAs device for different temperatures. Each arrow indicates the effects the doping regions inside the crystal and temperature change cause in the capacitance curve and they also point in the increasing temperature direction.

As it can be seen on the capacitance curves, the shoulders (arrows 2 and 3) demonstrate the different doping levels of the GaAs structure. They are very well pronounced for the lowest temperatures and smear out along with the temperature increase. Arrows

number 2 and 3 indicate how the first[3] and the second[4] steps vary with the heat. As one can see, at room temperature, the effects of the different doping layers of the GaAs wafer are still present but not so pronounced anymore.

I would like to propose a closer look at what is happening at the junction between two of these layers in order to explain this dependence on the sharpness on the layers effects on the capacitance curve. When the layers are brought together in the manufacturing process dopant atoms can diffuse from one layer to another. This means, in reality, that the border between two layers is not necessarily a sharp line. But the effects from this diffusion will be neglected in this discussion once it is small compared to the diffusion of carriers and it is the same for all temperatures.

A more important fact is that electrons from a doped region can diffuse to a non doped one. This process generates an electric current until the Fermi levels of the two layers are equal, i.e., thermal equilibrium is achieved. What happens here is basically the same as what happens in the Schottky contact case where a metal is brought in intimacy with a semiconductor. The only difference here is that the metal can be considered a thermodynamical *reservoir* or, in other words, it is an inexhaustible source/receiver of electrons and, hence, its Fermi level is unchangeable in such processes.

We can use the *drift diffusion* equation at thermal equilibrium, where there are no net currents, to generate an expression for the electric potential between the layers:

$$\vec{J} = \left(nq\mu \left(-\frac{dV_j}{dx} \right) - \mu kT \frac{dn}{dx} \right) \hat{x} = 0$$

[3]Caused by the abrupt doping level change between the first layer ($N_d^+ = 10^{17} cm^{-3}$) to the second doping layer (intrinsic).

[4]Caused by the abrupt doping level change between the third layer ($N_d^+ = 10^{16} cm^{-3}$) and the fourth layer (intrinsic)

$$\Rightarrow nq\mu\left(\frac{dV_j}{dx}\right) = \mu kT\frac{dn}{dx}. \tag{4.1}$$

Applying the chain rule from calculus and integrating between the two layers we reach an expression for the built in potential created by carriers diffusion from the doped to the non doped layer:

$$V_j = \frac{kTln\left(\frac{N_d}{n_i}\right)}{q}. \tag{4.2}$$

Once the terms N_d and n_i[5] are constant in this perimeter of the wafer, the height of this natural built in barrier for carriers will depend linearly on the temperature variation.

In order to establish a relation of the temperature of the device with the extension of this barrier inside the wafer, we can use the expression 3.1 where

$$W = \sqrt{\frac{2\varepsilon_s V_j}{qN_d}}.$$

Then,

$$W = \sqrt{\frac{2\varepsilon_s kTln\left(\frac{N_d}{n_i}\right)}{N_d}}. \tag{4.3}$$

Using the expressions developed above, we can deduce, at room temperature, an approximated width of 95nm which is about the length of the whole first layer. This means that the doping concentration for the first layer has been decreased along almost its whole extension due to diffusion. We must also remember that each intrinsic layer is between two doped ones and, therefore, it receives electrons from both sides. Finally, at 10K, the diffusion width is $\sqrt{\frac{300K}{10K}} \approx 5,5$ times shorter for each junction ($\approx 17nm$).

[5]This value in GaAs is in the order of $10^6 cm^{-3}$.

This means that the doping profile of the first layer is affected by the diffusion of carriers only locally in the vicinity of the junction.

According to the argumentation above, we are able to interpret the smearing out of the capacitance steps with the increase of temperature as the diffusion of free carriers into the intrinsic layers of the wafer. The intrinsic layers are being, indeed, *passively doped* from both sides, by diffusion, when they accept the electrons from the Si doped GaAs layers. In other words: the increase of thermal energy in the system mixes both layers (doped and intrinsic) and the border between them, that was so clear at low temperatures, at high temperatures is blurred.

4.1.2 AFM Measurements

The plots below are the Schottky diode capacitance curves taken from the AFM measurements. Each plot is the result of the average of 16 measurements with the tip stabilized. Both tip position and cantilever deflection are fixed and the temperature is at (36 ± 10^{-2})°C. As it will be soon noticeable, reproducibility in these measurements is not an easy task due to many difficulties that such measurements present. This section will point out the reasons for it and also establish a parallel between the AFM and the macroscopic device set ups as a Schottky junction.

We will start with figure 4.3 which is the closest to the device curve at room temperature. This capacitance curve was measured with the highest deflection[6] (3V) on the tip cantilever. As it is discussed by Smoliner et al. on reference [29], the Schottky barrier height depends on the tip force which means a larger built in potential. Here, in the same manner as in the device measurements at high temperatures, the steps corresponding to the

[6]Deflection is a synonym for pressure on the tip in this case.

different doped layers are not pronounced and we can also notice the local minimum pointed by the arrow 2.

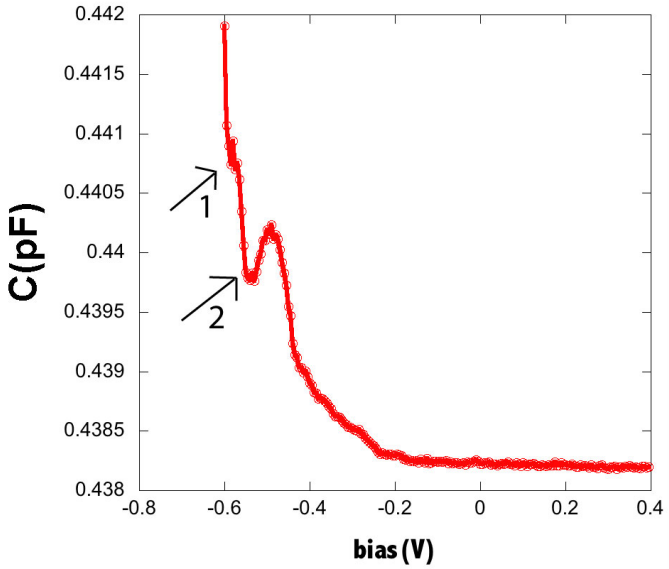

Figure 4.3: Capacitance measurement taken with deflection of 3V at (36 ± 10^{-2})°C.

The main difference between figures 4.3 and 4.4 is that the capacitance curve is shifted back on the voltage axis when compared the the similar curve on the device. This can be explained by the difference of the the work functions between the aluminum on the device and the diamond doped tip. Once the bands of the wafer are bent until the Fermi levels of the crystal and the metal are equal, the height of the barrier can be calculated by the difference of their work functions. Comparing figures 4.2 (at high temperatures) and 4.3, we can estimate that the shift on the voltage axis is of the order of 0.5 eV to the left in the AFM case. Now, adding this value to the aluminum's work function 4.08 eV [39], we can roughly estimate the tips work function to be 4.58 eV.

Figure 4.4 is the same capacitance spectrum as in the figure

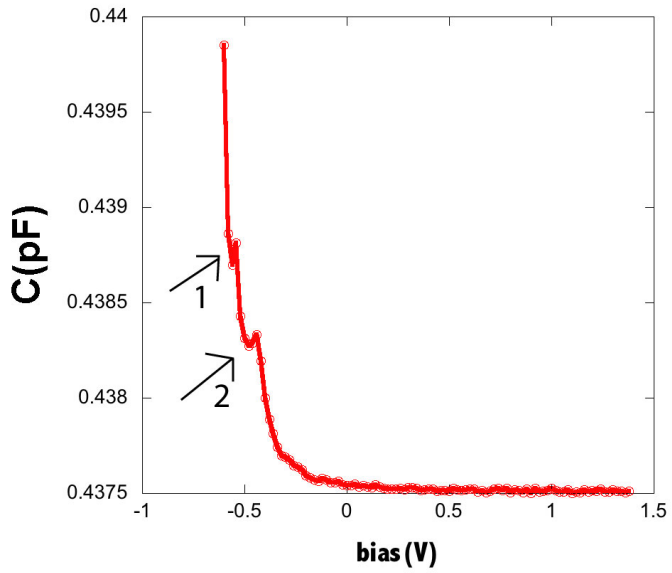

Figure 4.4: Capacitance measurement taken with deflection of 2V at (36 ± 10^{-2})°C.

4.3. This measurement was taken in a different zone on the top of the crystal and the deflection (pressure) of the cantilever was at 2V. As it is explicit on the figure, the features pointed by the arrows on the curve obtained from the device can still be observed. Nevertheless, they are not so prominent as for the case where the deflection is set to its highest value.

The difference between both curves due to the respective pressures applied on the tip give room to some speculations. In first place, its obvious that the high pressure causes a better contact between tip and semiconductor. Like that, the influence of any oxides, water films or any other dirt that could be on top of the wafer is reduced once the tip would simply break though them. It is also believed that the high pressures on the crystal are able to deform its lattice structure locally and, consequently, cause significant changes on the band structure. This is not what seems to happen in our curves because they are very similar to the ones

obtained in the device. Nevertheless, the very first small step indicated by arrow 1 in both AFM curves points to a feature that is not evident in the device set up and it could be caused by the tip's influences in the measurement.

After the previous discussion, there are some points about the capacitance spectroscopy in the AFM with a Schottky contact that can be exposed:

1. **The Results**: The difference of the results for the Schottky case between the AFM measurements and the device is not conclusive. The curves, are essentially the same for both measurements and, therefore, in terms of charge distribution and dopant analysis nothing new is brought by the AFM. On the other hand, the influence of insulators locally in the capacitance was evident in the AFM measurements.

2. **The reproducibility of the Measurements**: The curves we have showed the same structure and, basically, the same information could be read from them. The difference in the settings between them is just the deflection of the cantilever. Nevertheless, in the nanoscale the crystal's surface cannot be considered isotropic anymore due to agglomerations of oxides and other agents on its surface. This might lead the less experienced users to unreproducible results for different zones on the surface.

3. **The time of each measurement**: Adding the time spent on the measurement, in the preparation of the sample and also the wait of 12 hours until the AFM hatch got a stable temperature in the 10 mK magnitude goes up to 3 days. Moving the tip for another measurement on the crystals surface causes another wait of several hours until the piezo is stabilized and the measurement is trustable again. This is

another sign of how the measurements in this scale can be delicate.

4.2 The MOS Capacitor

4.2.1 MOS - Device Measurements

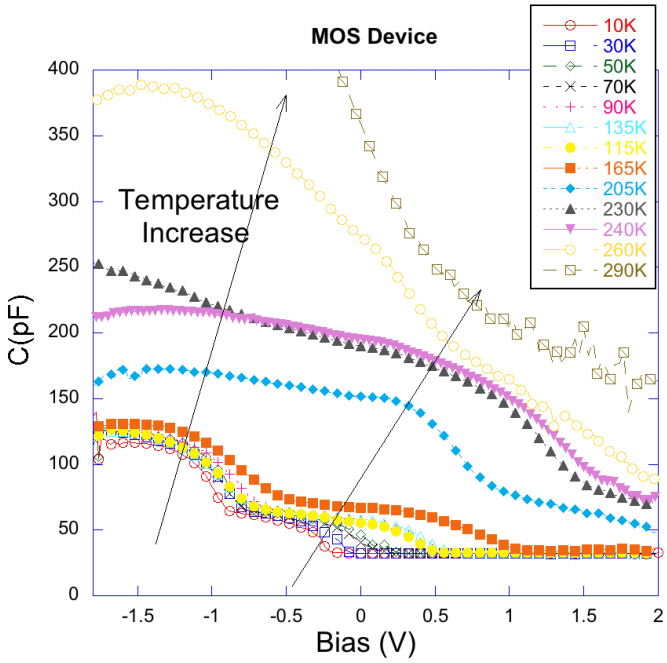

Figure 4.5: MOS Device Measurements.

The plots of figure 4.5 are the measurements of the capacitance in relation to the applied bias voltage performed on a MOS device fabricated with our Gallium Arsenide wafer with differently doped layers. For those measurements, the frequency was kept fixed at 1 kHz and the temperature varied as the arrows indicate. It's straight forward to verify, based on the discussion of the section 3.2.2, that there is no low frequency behavior for any temperature measured.

In the lowest temperatures, the capacitance behaves similarly to the case of the Schottky junction. Right after accumulation, the MOS capacitor starts to operate in depletion and the first and second shoulders (indicated by the arrows), which represent the doping difference between the layers, are present on the capacitance curve. With the increase of the temperature, in the same way as it is for the Schottky contact, the steps on the curve are less sharp and the doping difference among the many layers is subtle. At 290K, they are not seen on the capacitance curve anymore.

4.2.2 MOS - AFM measurements

The measurements for the MOS junction in the AFM are described on figure 4.6. These measurements were performed in the same way as for the Schottky junction case, i.e., each plot is the result of the average of 16 measurements with the tip standing still. The cantilever deflection is fixed and the temperature is at (36 ± 10^{-2})°C. Here, reproducibility is not difficult to reach as it is for the Schottky case since the influences that the native oxide on the surface might cause on the capacitance do not seem to influence the results when the tip is relocated on the crystal's surface[7].

Figure 4.6 displays the capacitance measurements in the AFM for a range of frequencies and the arrows indicate the variation of the capacitance with the decrease of the measurement frequency. In the nanoscale, the capacitor formed by the AFM tip and the wafer present capacitances in the aF (10^{-18}F) regime. Therefore, differently from the devices measurements, the cir-

[7]The thick oxide layer is present anyway and the influence of other bodies beneath it is negligible.

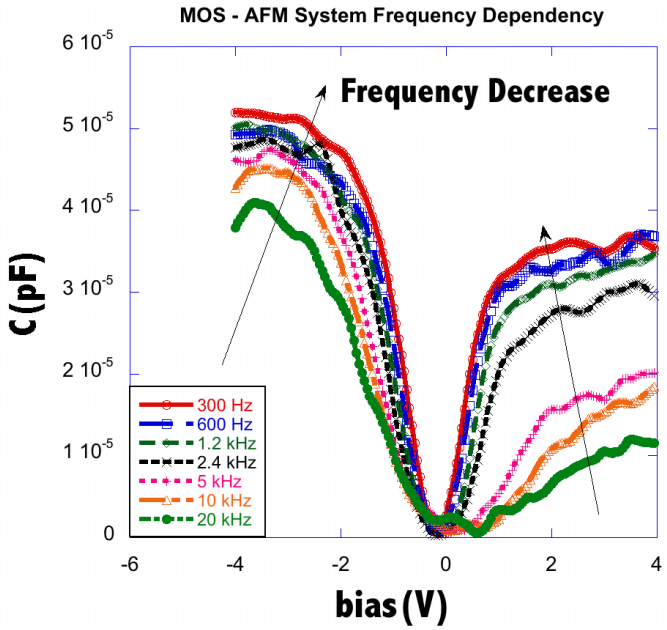

Figure 4.6: AFM Capacitance Measurement at (36 ± 10^{-2})°C.

cuitry capacitance (stray capacitance) play a significant role and must be subtracted. The results displayed on figure 4.6 do not present any apparent features resulting from the differently doped layers in the crystal structure. This fact is in agreement with the device measurements where the layer effects disappeared at higher temperatures. Nevertheless, differently from the device measurements, the AFM measurements indicate a low frequency behavior in the whole frequency range.

The reason for this low frequency behavior showed by the curves of figure 4.6 rely on the surface states (traps)[8], on the charges confined in the oxide and, finally, also on the geometrical aspects of the electrical field generated by the acute tip.

[8]Please refer to [40]

Surface States and Oxide Charges

On the surface of Gallium Arsenide there are the so called surface states that can cause a natural band bending due to the concentration of charge in a potential near the crystal edge. Arsenic oxide has been linked to the surface states in Gallium Arsenide located at about one third of the energy band gap above the valence band. These surface states cause the Fermi energy to be pinned: electrons from the valence band fall into the surface states until the Fermi energy coincides with the level to which the surface states are filled. This causes a natural surface depletion in gallium arsenide and a potential across the semiconductor[19].

The Geometry of the Field Lines

Because of its size, the tip starts to work almost as a point change next to the vast plane that is the oxide-semiconductor surface. Thus, the field lines will not be parallel anymore as in the case of the device where the gate is a large plane. In the case of the tip, field lines will spawn in all directions inside of the crystal and the system cannot be considered one-dimensional anymore. The symmetry to be regarded is approximately spherical and the problem becomes intractable in an analytical way. In this case, computer simulations are needed to extract information by solving the Poisson equation[9].

$$\vec{\nabla}^2 V = -\frac{\rho(V; r, \theta)}{\varepsilon_s}, \tag{4.4}$$

[9]The system has to be considered quasi static and, therefore, the Poisson equation has to be solved at the same time with the drift diffusion equation. Some exemples of these techniques can be seen on the works of T. Kerkhoven [37] and William R. Frensley[38].

where $\rho = qN_d^+(r,\phi)\left[\left(1-e^{\frac{-qV}{kT}}\right)-\left(1-e^{\frac{qV}{kT}}\right)\right]$.

The scheme of the MOS capacitor formed by the tip and the wafer is shown on figure 4.7. The label “surface holes” represents the natural holes accumulation on the surface due to the electric field generated by the mid gap pinnning and the oxide charges. “Inversion” and “depleted electrons” depict the depletion zone densely populated by holes in the inversion regime and the depleted electrons in the back side of the wafer, respectively.

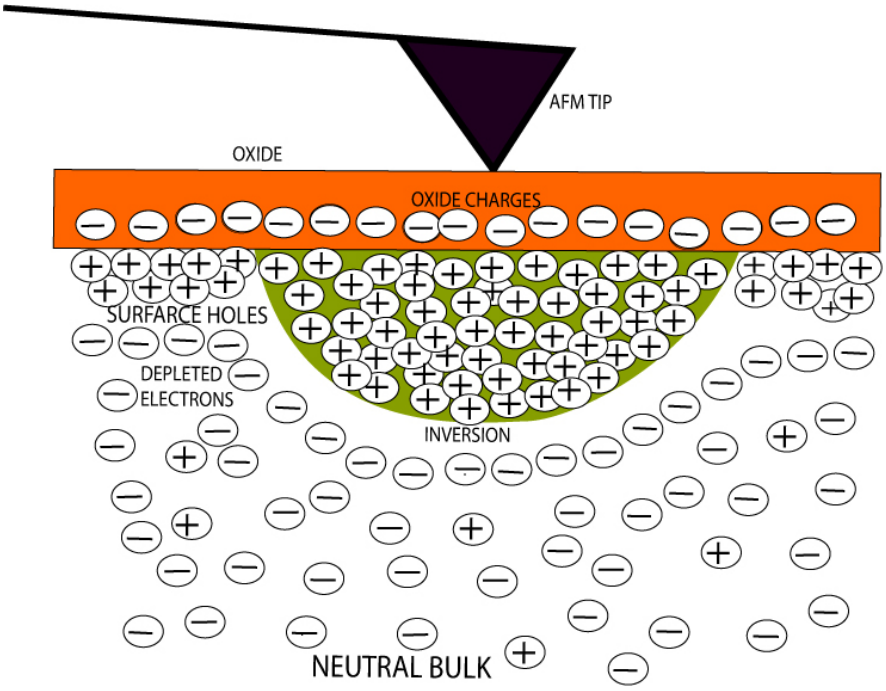

Figure 4.7: MOS in inversion mode with spherical symmetry.

As discussed in section 3.2.2, the low frequency behavior of the capacitance curve depends on the requirement of charge neutrality between the gate and the minorities during the measurement. That means that the electric field generated by the voltage applied on the tip has to be totally or, at least, partially screened in order to have the capacitance due to the minorities

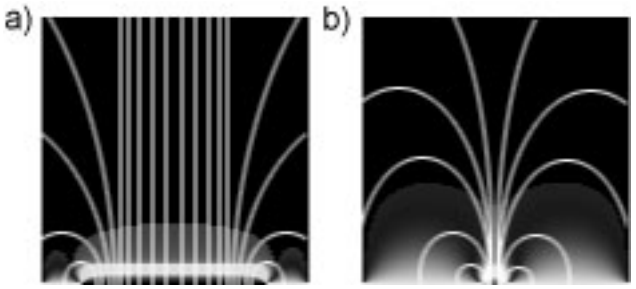

Figure 4.8: Simulation of the field lines for a gate with: a) 800nm and b)30nm. Courtesy of Christian Eckhardt.

(inversion) felt in the measurement. As it is shown in the figure 4.8 “a”, the field lines go in all directions in the wafer and the holes previously accumulated on the surface of the crystal due to the electric potential generated by the midgap pinning are available to quickly respond to the signal applied when the capacitance is measured. This way, the capacitance reading in the accumulation regime turns out to be identified with a low frequency curve.

In the macroscopic device, the situation is different. Due to the large dimension of the gate, as one can see in 4.8 “b”, the field lines are parallel and grow almost in one direction only in the crystal. The holes are still available at the surface but the field lines at the borders of the contact are not strong and long enough to attract the holes sufficiently fast to respond to the signal. As a matter of fact, in large devices, the low frequency behavior of the capacitance curve will depend only on the thermal creation of holes deep in the bulk during the application of the electrical pulse and, according to our measurements, this frequency is clearly below 1kHz[10].

The density of holes on the surface of the wafer can be estimated based on the total oxide charges and also on the band

[10]please refer to figure 4.9

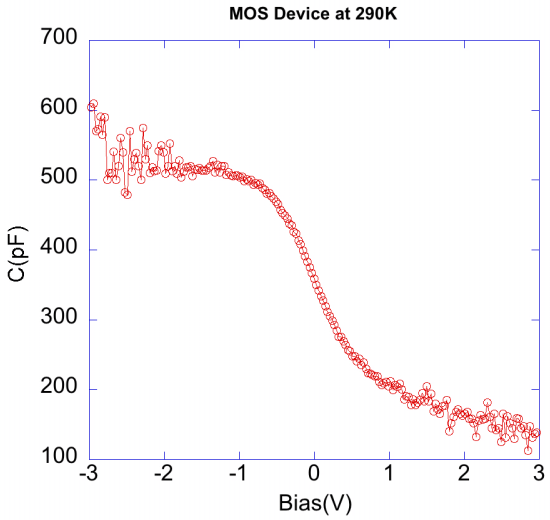

Figure 4.9: Capacitance curve measured for the Device at 290K.

bending caused by the surface states. In general, unlike interface-trapped charges, these oxide charges are independent of bias, so they cause a parallel shift in the gate-bias direction. Then, by comparing the ideal calculated capacitance curve given by section 4.2.2 with the real curve we will be able to determine this shift. The ideal capacitance for zero bias, using the total capacitance of the MOS system, is given by:

$$C = \frac{C_i C_s}{C_i + C_s}, \tag{4.5}$$

where

$$C_i = \frac{\varepsilon_i}{d}. \tag{4.6}$$

Hence, at zero bias, the ideal capacitance of the semiconductor after expanding the equation 3.2.1 will be given by

$$C_s = \frac{\varepsilon_s}{L_D}, \tag{4.7}$$

where $L_D = \sqrt{kT\varepsilon_s/N_d^+ q^2}$. Inserting expressions 4.6 and 4.7 in espression 4.5, the ideal capacitance at zero bias will be given by

$$C = \frac{\varepsilon_i \varepsilon_s}{\varepsilon_s d + \varepsilon_i L_D}. \tag{4.8}$$

After all these calculations, the calculated potential shift due to the oxide charges is 0.08 V.

Now, turning our attentions to the value of the work functions of the aluminum contact (4.08 eV) and of the Gallium Arsenide wafer (4.07 eV)[11], we conclude that there is no significant difference on the work functions and, therefore, the built in potential in the case of the Schottky contact is nothing more than the potential created by surface states of the GaAs wafer. Using the capacitance curve at room temperature of the graph 4.2 and the equations of section 3.1 we were able to calculate this built in potential. After the calculations, we arrived at 0.70 V for this potential[12].

By adding the potential created by the oxide charges (0.08 V) and the band bending caused by the potential of the surface states, we can approximate an “effective” band bending of 0.78 eV for the wafer. Once the energy gap for GaAs is 1.4 eV and the Fermi level is very close to the conduction band due to the high doping, we can estimate the concentration of holes in the oxide-wafer interface as[13]:

$$p = N_v e^{-\frac{(E_V - E_F)}{kT}} \approx 10^8 cm^{-3} \tag{4.9}$$

If we approximate the point where the cloud of holes is concentrated in the wafer right below the tip to a metal contact as

[11] Extracted from reference [20], pg. 790.

[12] Which is in good agreement with the literature [36].

[13] N_v *is the valence band density of states* $9\ 10^{18} cm^{-3}$

in the Schottky case in forward bias, we will be able to extract an estimation for the cutoff (maximum) frequency that the system will stand until it stops showing a low frequency behavior. We can calculate the resistivity for the holes on the surface of the wafer using the expression

$$\rho = \frac{1}{q\mu p}.$$

The value found after the calculations is $\rho = 1.56\ 10^8 \Omega$cm.

Using the expression for the spreading resistance of a point contact[14]

$$R_s \approx \frac{\rho}{2\pi r_0},$$

where r_0 is in the order of magnitude of the tip radius (30nm), and the RC time constant

$$f = \frac{1}{2\pi R_s C} = \frac{r_0}{\rho C}, \tag{4.10}$$

we were able to estimate the cut off frequency of the MOS capacitor in accumulation to be of the order of 3,85kHz. If the gate size is increased to the device scale (μm), the capacitance will be increased by a factor of 10^7. According to the equation 4.10, the cutoff frequency "f" will be roughly ($\frac{10^3}{10^7}$) 10000 times smaller than it is for the AFM set up leading to transition frequencies in the order of 10-100Hz which is in perfect agreement with the data we extracted from the device where, at 1khz, the capacitance was far away from showing a low frequency behavior.

After the previous discussion, there are some points about the capacitance spectroscopy in the AFM with a MOS configuration that can be exposed:

[14] Extracted from [20] p. 182.

1. **The Results**: Differently of the measurements for the Schottky case, the results we have gathered for the MOS case show two totally opposite behaviors when one is concerned with the frequency in which the measurements were taken. It's clear from the data that 1kHz is by far high frequency for the GaAs MOS devices. On the other hand, the measurements performed in the AFM showed the low frequency character up to the highest frequency at which the measurements were taken (20kHz). It is clear that the main reasons for this difference are the geometry aspects and size of each set up. As we have proposed, the size of the tip causes the field lines to be spherically symmetric and, therefore, they make it possible that the holes available on the surface take part on the capacitance measurements. The influence of the size of the device has also to be pointed. As one can see, the two factors that influence the estimated cutoff frequency (R_s and C_i from equation 4.10) are directly influenced by the small size of the gate (tip). This fact could open room for further investigations about influence of the gate size over the capacitance measurements.

2. **The reproducibility of the Measurements**: In the MOS set up, the AFM measurements did not present further complication in order to reproduce the measurements. The oxide surface did not show any substantial irregularities and the measured capacitance was the same in every position on the wafer.

3. **The time of each measurement**: As in the Schottky measurements, time played also an important role in the experiments for the AFM MOS set up. Adding the time spent in the measurement, in the preparation of the sample and also the

wait of 12 hours until the AFM hatch got a stable temperature in the 10 mK magnitude goes up to 3 days. Moving the tip for another measurement on the crystals surface causes another wait of several hours until the piezo is stabilized and the measurement is trustable again. This is another sign of how the measurements in this scale can be delicate.

Chapter 5

Space Charge Region Measurement

In this chapter we present an industrial usage of SCS techniques in the AFM. The solar cell used in these measurements are made of doped Silicon and were provided and produced by Blue Chip Energy[41]. In order to determine the doping profile and carrier concentration, we have performed cross-sectional capacitance measurements.

To maximize the light absorption, the solar cell top part (p-type Si) is molded with pyramid like structures etched into the surface. We have taken some pictures of them with an optical microscope and, as one can see on figure 5.1, their height and base dimensions are of, approximately, 7,50μm and 9,92μm, respectively. Figure 5.2 gives a closer look on the pyramids and the surface density can be calculated to be of about a million pyramids per cm^2.

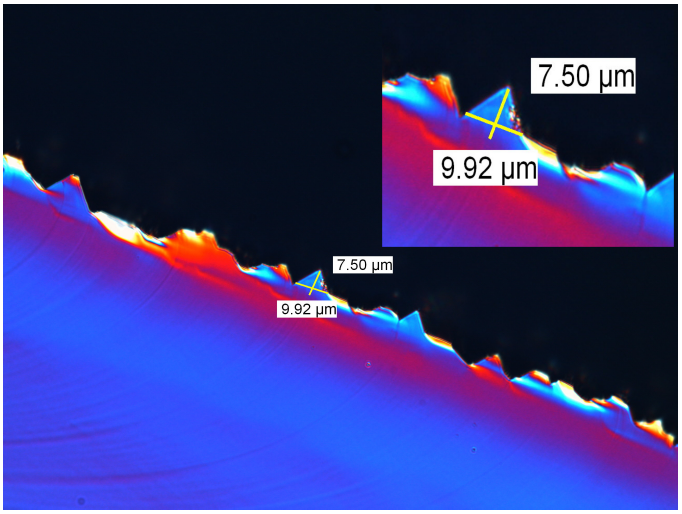

Figure 5.1: Solar Cell Top Pyramids - Cross-sectional Image.

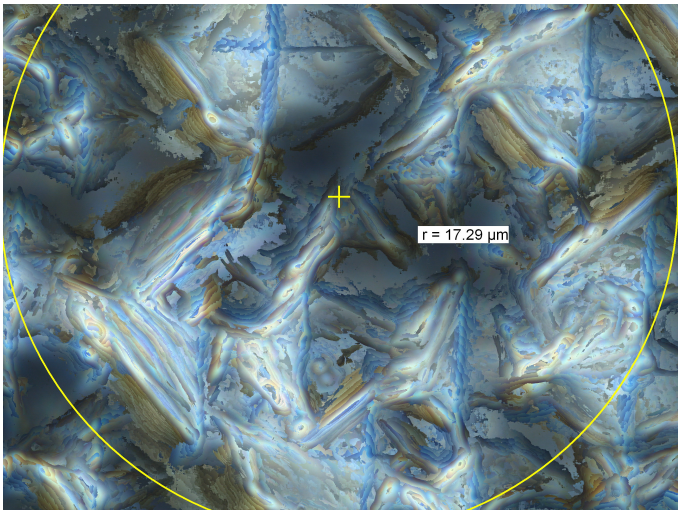

Figure 5.2: Solar Cells Top Pyramids - Top Image.

The Capacitance Measurements

We have performed cross-sectional capacitance measurements at 20kHz starting from the p-type bulk region all the way till the upper end of the wafer after the n-type zone. As one can see on the picture 5.4, the capacitance curves measured are typical of a MOS capacitor. The reasons for this curve are: 1) Silicon, in the contrary of GaAs, has a natural oxide (SiO_2) that grows spontaneously while the wafer is in contact with the oxygen from the atmosphere and 2) the AFM tip used in the measurements was not though enough to break through the oxide.

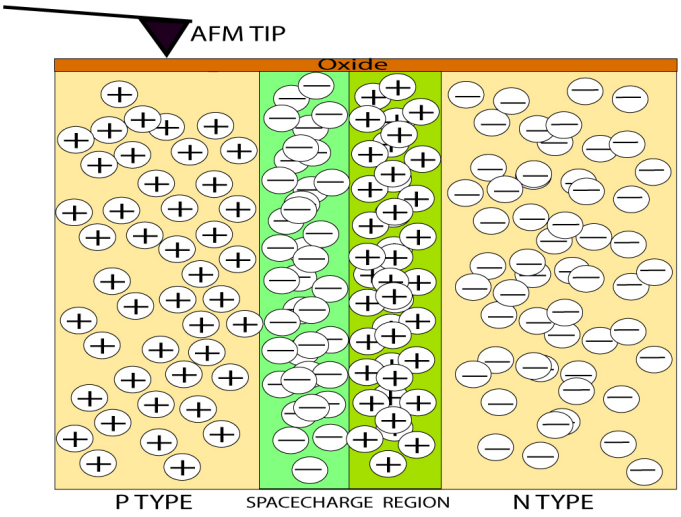

Figure 5.3: Tip and Solar Cell Scheme.

As it is depicted on the figure 5.3, the tip was set somewhere deep in the p-type bulk and, after each step, capacitance spectra were acquired. The idea behind it is that deep in the bulk the capacitance curve must not show low frequency behavior once there are not enough minorities[1] to respond do the signal. But, as we approach the space charge region of the p-n junction, the electrons available in the p-type side will be able to respond to

[1]Note that in the p-type case the minorities are the electrons.

the applied electric field and low frequency curves will be observed.

In other words, the space charge zone will work as a minorities "reservoir" for the MOS capacitor and, when the tip is close enough to attract those electrons, the capacitance will present a low frequency curve. This system will basically work analogously to the case described in section 4.2.2 where holes, deposited next to the oxide because of the action the surface states present in GaAs, made the low frequency capacitance curve for frequencies considered high possible. Just like for the GaAs case, the low frequency here is an effect caused by the combination of geometrical properties of the capacitor and the availability of minorities.

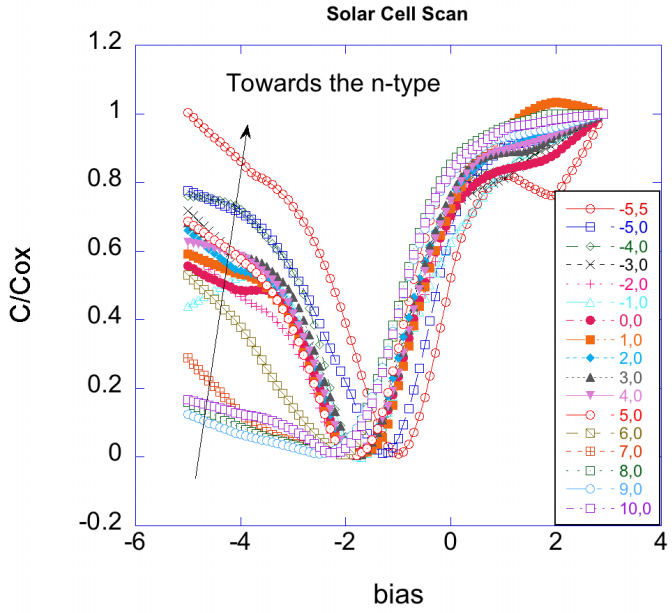

Figure 5.4: Capacitance curves in different positions of the solar cell. The total capacitance C is normalized by the oxide's capacitance C_{ox} Each unit corresponds to a 25nm step on the wafer.

The capacitance curves acquired in the measurements are displayed in the figure 5.4. The curve labeled as 10,0 is the first set

of measurements taken when the tip was set on a position deep in the p-type bulk. Every unit corresponds to a 25 nm step towards the n-type zone.

One can easily identify the capacitance presents a high frequency behavior for positions 10,0 till 7,0 while the tip is positioned deep in the bulk. The low frequency curves are more prominent after position 6,0. From this point on, the low frequency characteristic of the capacitance curve indicates that the tip sits on top of the space charge zone once the electrons -available there- can influence the nature of the curve as we have previously discussed. After the position -5,5, the signal is too noisy and no capacitance can be read.

Using another sample with an oxide layer of 7nm on top, we could estimate the doping profile of the p-type Silicon. The Calculation was done using the one-dimensional model in the following manner: the effective area of the tip can be estimated by using the expression for the oxide capacitance[2]

$$A_{eff} = \frac{C_{ox} d}{\varepsilon_{ox}}. \tag{5.1}$$

The capacitance due to the semiconductor is given by[3].

$$C_s = \frac{\varepsilon_{ox}}{W} A_{eff} = \frac{C_{ox} d}{W}. \tag{5.2}$$

Using the expression above and the fact that

$$\frac{1}{C_s} = \frac{1}{C_{total}} - \frac{1}{C_{ox}},$$

we can deduce an expression for W:

[2]The oxide thickness is given by d.

[3]Here we use the fact that $\varepsilon_{ox} \approx \varepsilon_{semiconductor}$. W is the width of the depletion zone in the semiconductor.

$$W = d\left(\frac{C_{ox}}{C_{total}} - 1\right). \tag{5.3}$$

Finally, using the expression for W give in section 3.1, the doping N_a^- for the p-type Si will be given by

$$N_a^- = \frac{2\varepsilon_{ox}(V_{(bi)} - V)}{qW^2}. \tag{5.4}$$

Estimating the built in voltage ($V_{(bi)}$) to be the difference of the work functions of Si and the tip ($\approx 1V$) and using the data set of figure 5.5 collected from the p-type bulk covered with a 7nm thick oxide layer, we calculated the doping N_a^- to be $(2,78 \pm 1,82)10^{16}cm^{-3}$.

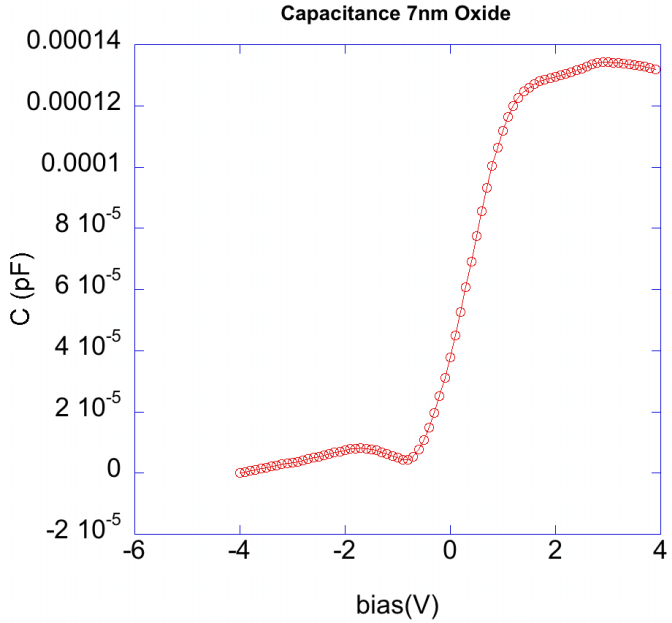

Figure 5.5: Capacitance curve taken deep in the p-type bulk with 7nm oxide on top of the sample used for the doping determination.

Now, from the AFM capacitance curves in the figure 5.4, we will be able to literally measure the size of the space charge zone

in the solar cell. Assuming that the first low frequency curve (at position 6,0) sets the point where the space charge region (SCR) starts and that the n-type Si is highly doped to the point that the size of the SCR is negligible in this side[4], we can calculate the size of the SCR to be the number of low frequency curves times the size of each step: $W = (287,5 \pm 20)nm$. After knowing the size of the space charge region, the built in voltage of the p-n junction can be estimated by using[5]:

$$V_{(bi)} = \frac{W^2 q N_a^-}{2\varepsilon_s}. \tag{5.5}$$

Finally, the doping (N_d^+) of the n-type Si can be estimated by the expression

$$N_d^+ = \left(\frac{n_i^2}{N_a^-}\right) e^{\frac{qV_{(bi)}}{KT}}. \tag{5.6}$$

Nevertheless, the value for the N_d^+ calculated from the data mentioned above is not trustable once the exponential is very sensitive to the value of the p-type doping. This sensitivity of the n-type doping calculation to the p-type doping level is due to the the space charge zone which is measured by us and has its length fixed.

The value of 2,78 10^{16} cm^{-3} for the doping in the p-type gives a doping value N_d^+ for the n-type that is out of any consideration (about $10^{33}cm^{-3}$). However, one has to keep on mind, that the calculated doping profile from the AFM measurements while using a one dimensional model is typically correct only within a factor 2. Therefore, if we use half of the value of the calculated p-type Si doping (1,5 $10^{16}cm^{-3}$), it would give us $N_d^+ = 10^{19}cm^{-3}$

[4]Having the n-type highly doped when compared with the p-type is an industrial standard procedure in the solar cells production.

[5]Where ni is the intrinsic carrier density for Si (10^10) and KT is 0,026 eV.

to the n-type. Note that the factor 2 causes a huge difference because of the exponential nature of the problem.

Based on the arguments above, the sensitivity of the numbers to the smallest variation, suggests that the one dimensional evaluation is not enough to present trustable values for the doping profile using the measured of the length of the space charge zone. Full 3D simulations would be necessary in order to determine the correct doping profiles. However, these simulations are somewhat too complicated and are out of the scope of this work.

Unfortunately, the p-n junction position could not be determined once inversion on the voltage axis was not observed and the capacitance readings were not conclusive after the position -5,5. The short length of the n-type Si and the technical difficulty to set the AFM tip on the edges of the surface pyramids, where the n-type Si is located, can be suggested as the reasons for the non determination of the p-n junction in these measurements. Examples of the p-n junction delineation can be found in the references [42] and [43].

Chapter 6

Closing Remarks

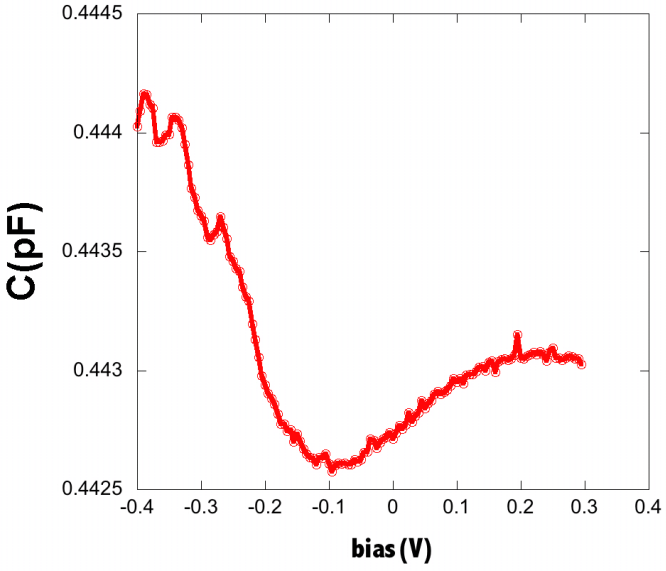

Figure 6.1: SCS curve of a Schottky contact with deflection of 1V at 300K.

In this work we have performed systematic capacitance measurements on a multilayered Gallium Arsenide structure with the Atomic Force Microscope and with the macroscopic device. A parallel between the well understood behavior of the capacitance on the macroscopic device has been made and the results were very

satisfactory in both cases: Schottky and MOS.

In the Schottky case the main difference between the measurements in the device and in the AFM is the parasitic effect [1] that any insulator (oxides, water film, etc.) that lays on the surface of the wafer can cause on the capacitance measurement. In the large scale, these surface impurities will not cause any effect once the size of the contact is much larger than the area of such insulator laying on the surface of the wafer. On the other hand, in the case of the contact of the AFM tip, in the nanometer scale, these insulators can cause severe (or even undesired) changes in the capacitance curve. One example is the curve from figure 6.1 that was taken with a Schottky contact but clearly shows the behavior of a MOS capacitor curve. The main influence here comes from the crystal's surface that cannot be considered isotropic anymore in the nanoscale due to these dielectric agglomerations. Perhaps these effects on the capacitance could give a hint about the growth of natural oxides on GaAs, i.e, which locations on the surface and which conditions are favorable for their growth.

In the MOS case, the difference between device and AFM measurements was astounding. The low frequency behavior was not expected at all for the AFM case and it is strongly indicated by the comparisons we have traced between the AFM and device measurements that the reason for such difference between both of them is basically caused by the size of the gate and the spherical symmetry of the field lines in the latter measurement[2]. Accord-

[1] As techniques improve, the scale of microelectronic components continues to decrease. At smaller scales, the relative impact of intrinsic circuit properties such as interconnections may become more significant. These are called parasitic effects, and the goal of the microelectronics design engineer is to find ways to compensate for or to minimize these effects, while always delivering smaller, faster, and cheaper devices[44].

[2] This aspect of our measurements will be sent for publication in a special-

ing to what was shown here, it may be suggested that GaAs can be used in the fabrication of “nanosized” MOS capacitors to operate at high frequencies, as we have roughly predicted in our calculations, up to 4 kHz[3]. Hopefully, shall this work open the way for more investigations on the nature of this low frequency behavior of the capacitance curve when measured in the AFM not only in GaAs but also in other semiconducting materials.

In chapter 5, the precision of the AFM capacitance measurements performed on the Si made solar cell was used to, literally, measure the size of the space charge region of the p-n junction. From these curves, we have also estimated the respective doping profiles from the space charge region measurements. Even tough the doping level calculation for the n-type turned out to be very sensitive to the precision of the doping level estimation of the p-type Si, we have found reasonable values for them in a one dimensional evaluation. Nevertheless, in order to acquire trustable values for the doping profiles, complicated 3 dimensional models must be used in the case of the p-n junction.

Even though, reproducibility and measurement time are still an enormous challenge for the effective usage of the AFM SCS/SCM techniques in the industry, both for quality control or for new small scaled devices development, there are already significant advances and unexpected phenomena which are not expected in the large devices (just like the low frequency behavior we have described in the previous section) that set these techniques firmly in the development path of modern electronics.

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ized journal.

[3]For macroscopic device, this limiting frequency is of the order of 100 Hz.

Appendix A

List Of Constants

Symbol	Description	Value
eV	Electronvolt Energy	1 eV = 1.60218 10^{-19}J
k	Boltzmann constant	1.3806503(24) 10^{-23} $\frac{J}{K}$
q	Charge of the electron	1.602176462(63) 10^{-19} C
ε_0	Permittivity in vacuum	8.854187817 10^{-14} $\frac{F}{cm}$
μ	Holes Mobility in GaAs	$\leq 400\text{cm}^2V^{-1}s^{-1}$
n_i	Intrinsic carrier density for Si	$10^{10}cm^{-3}$

Appendix B

Gallium Arsenide Constants at 300K

[1]

Crystal structure	Zinc Blende
Group of symmetry	Td2-F43m
Number of atoms in 1 cm^3	4.42 10^{22}
de Broglie electron wavelength	240 A
Debye temperature	360 K
Density	5.32 gcm^{-3}
Dielectric constant (static)	12.9
Dielectric constant (high frequency)	10.89
Effective electron mass me	0.063mo
Effective hole masses mh	0.51mo
Effective hole masses mlp	0.082mo
Electron affinity	4.07 eV
Lattice constant	5.65325 A
Optical phonon energy	0.035 eV
Energy gap	1.424 eV
Intrinsic carrier concentration	2.110^6 cm^{-3}
Intrinsic resistivity	3.310^8 O cm
Effective conduction band density of states	4.710^{17} cm^{-3}
Effective valence band density of states	9.010^{18} cm^{-3}

[1] Extracted from reference [45].

Appendix C

Silicon Constants at 300K

[1]

Crystal structure	Diamond
Group of symmetry	Oh7-Fd3m
Number of atoms in 1 cm3	5 10^{22}
Auger recombination coefficient Cn	1.1 10^{-30} cm6 s^{-1}
Auger recombination coefficient Cp	3 $10^{-31} cm^{6}$ s^{-1}
Debye temperature	640 K
Density	2.329 g cm^{-3}
Dielectric constant	11.7
Effective electron masses ml	0.98mo
Effective electron masses mt	0.19mo
Effective hole masses mh	0.49mo
Effective hole masses mlp	0.16mo
Electron affinity	4.05 eV
Lattice constant	5.431 A
Optical phonon energy	0.063 eV

[1] Extracted from reference [46].

Appendix D

Article Submitted to the Appl. Phys. Lett.

Frequency Dependent Scanning Capacitance Spectroscopy on GaAs – Metal-Oxide-Semiconductor Junctions

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Abstract:

In this work, an unusual low frequency behavior observed in Scanning Capacitance Microscopy (SCM) on Metal-Oxide-Semiconductor (MOS) structures on GaAs is investigated. Using a two-dimensional model we show that the natural surface depletion field on GaAs generates a permanent minority carrier accumulation around the tip apex. In contrast to thermally generated minority carriers in the space charge region of a large area device, the minority carrier distribution around the SCM tip apex is detected up to much higher excitation frequencies. An analytic approach to estimate the transition frequency between the low and high frequency regime is also given.

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In semiconductor physics, various scanning probe microscopy (SPM) methods are used in a wide area of applications ranging from basic research to industrial quality control. For the investigation of semiconductor nanostructures, atomic force microscopy with conducting tips[1,2] is especially helpful as well for the local characterization of dielectric layers[3,4,5,6] as for the investigation of organic films[7]. The technique we want to discuss in this paper is Scanning Capacitance Microscopy/Spectroscopy (SCM/SCS). In SCM, a conductive AFM tip is used to measure the local capacitance between the tip and the sample. In scanning capacitance spectroscopy (SCS), the capacitance is recorded during a DC voltage sweep to obtain a capacitance versus voltage C(V) curve for further analysis. The main application of this method is two-dimensional carrier profiling for failure analysis or process control especially on cross sectional samples.

SCM/SCS measurements, especially if quantitative results are desired, are a major challenge for technical and physical reasons. First, the measured capacitance is in the aF regime only, and to obtain a reasonable signal size at reasonable data collection speed for imaging, lock-in techniques are normally needed. Thus, commercial SCM systems usually yield qualitative dC/dV data only, which have to be calibrated for quantitative results. This, however, is technically complicated due to large difficulties with the reproducibility of the reference sample preparation process, and also the properties of the SCM tip – sample contact have a large impact on the experimental data. More information about this topic can be found in the review articles[8,9], e.g.

In this paper, the low frequency behavior observed in SCM on a GaAs Metal - Oxide - Semiconductor (MOS) junctions is investigated. In detail, the influence of the surface states, the charges confined in the oxide of a GaAs MOS junction, and also the influence of the AFM tip geometry is discussed using a two-dimensional self consistent Poisson solver. All results

are also compared with the situation for a macroscopic MOS device and experimental SCS data.

The samples we used for our studies were MOS-type junctions on n-doped GaAs (N_D= $1\cdot10^{16}$ cm^{-3} confirmed by Hall measurements). For the MOS junctions, Al_2O_3 was used as insulator. To obtain a good oxide quality, the Al_2O_3 has been grown by Atomic Layer Deposition (ALD) at temperatures of 200°C from Trimethylaluminum (TMA) and water precursors. Prior to the deposition, all substrates have been exposed to ammonium hydroxide (NH_4OH) for 3 minutes to remove the native oxide and leave a hydroxylated GaAs surface[10]. After oxide deposition, rapid thermal annealing in inert N_2 atmosphere has been applied for a duration of 30 sec. at 600 °C. Typically, these films have a dielectric constant[11] of k=9, a bandgap of 8.7 eV and are amorphous[12] up to processing temperatures of 850 °C. On all samples used for this work, the oxide thickness was 7nm.

All SCM measurements where carried out using a Digital Instruments DI3100 Atomic Force Microscope. For quantitative SCS, an ultrahigh precision, variable (50Hz-20kHz) frequency capacitance bridge (Andeen Hagerling AH2700A) was attached to the AFM. For all measurements, a modulation voltage of 250 mV was used. As AFM cantilevers we used AFM tips from NanoWorld, which were coated with highly doped (p-type, N_A= 1×10^{20} cm^{-3}) conductive diamond. Typically, these tips have a pyramidal shape with side angle of approximately 45° according to the datasheet. As shown in our previous work[15], these tips have a typical contact area of 30 nm × 30 nm and can regarded to behave completely metallic. More details about the setup used for quantitative SCS can be found in our previous publications[13,14,15].

In Fig. 1 (a) experimental SCS data of a MOS-type tip-sample contact on n-type GaAs substrates with Al_2O_3 oxide layer (d=7 nm) is shown for various frequencies: Curve (1) was measured at 140 Hz, (2) at 300 Hz, (3) at 1.2 kHz, (4) at 5 kHz, (5) at 10 kHz, and curve (6) at

20 kHz, respectively. For all cases, the shown curve is an average over 25 single C(V) spectra acquired at the same position. Normally, the C(V) curves are superimposed on a huge parasitic background capacitance, which always exists between the large tip-holder and the sample. In Fig. 1(a), however, this huge parasitic background capacitance was subtracted and subsequently, the curves were separated by an offset of 10 aF for better viewing. As one can see, the C(V) curves on our GaAs MOS structures show a clear minimum around zero bias ("low frequency behavior") up to 1.2 kHz. Above 5 kHz, the shape of the capacitance curves change into a typical "high frequency behavior", as it is typically observed on macroscopic devices, but also in our previous SCM/S experiments on Silicon samples[16,17] (see Fig. 1(b)).

It must be pointed out, however, that for the GaAs sample, the frequency, where the transition from low frequency to high frequency behavior is observed, is quite unusual. On macroscopic Silicon MOS devices, this transition is usually observed at frequencies between 10 Hz and 100 Hz (see Ref. [18] e.g.), and also in our SCS experiments on Silicon samples, we always observed typical high frequency behavior, too. To illustrate this, typical SCS data of a silicon sample are plotted in Fig. (1b). As one can see, the curve exhibits a clear high frequency behavior, although it was measured at f=140 Hz only. In addition to the SCS data, we have plotted the C(V) curve of a macroscopic GaAs sample with Al_2O_3 (7nm) and an Aluminum electrode on top. This curve was measured at a frequency of f= 1kHz but, in contrast to the SCS data obtained on the same piece of wafer (see Fig. 1(a)), the macroscopic device also shows a clear high frequency behavior for a frequency, where a low frequency behavior is observed in SCS.

In the following, we will show that the low frequency behavior of the SCS curves observed on GaAs MOS structures can be consistently explained by the influence of charged surface states, oxide charges and the geometrical aspects of the electrical field generated by the tip apex. For all calculations a two - dimensional, self – consistent Poisson solver was

used, which we already employed in our previous work[15]. We first discuss the geometrical aspects of the tip-sample geometry:

Fig. 2 shows a two dimensional simulation of the electric field lines of a MOS-type GaAs sample for a device with a gate area of 800 nm x 800 nm (a) and for an AFM tip sample contact with a typical contact size of 30 nm × 30 nm (b). Due to its small size, the tip can be considered as point charge in the large plane of the oxide-semiconductor surface and as a consequence, the field lines reaching from the gate into the substrate are no longer parallel. This situation is illustrated in Fig.2 (b), where we can see, how the field lines spawn into all directions.

In C(V) measurements, the observation of a low or high frequency behavior depends on the question, whether in inversion the cloud of minority carriers under the gate electrode can be charged by the capacitance signal or not. As it becomes clear from Fig. 2 (b), this is especially easy in the case of the SCM tip: The field lines in the substrate radial extend into all directions and the minority carriers (holes), which are permanently accumulated around the tip – sample contact due to the natural surface depletion field in GaAs, are always available to respond to the signal when the capacitance is measured (low frequency behavior). In contrast to that, Silicon MOS structures have no built in natural band bending. As a consequence, the concentration of minority carriers around the tip sample contact at the surface is very small, and thus, the charge transport between the inversion carrier cloud and the backside contact relies on the slow thermal generation rate for minority carriers only. As a consequence, only "high frequency" SCS curves are observed on Silicon only.

Similar arguments like above can be applied to explain the high frequency C(V) curves of our GaAs MOS *device.*

Although a surface depletion is present on GaAs all the time, the field lines under the large area gate contact are parallel and extend into the substrate only in one direction. At the

borders of the large capacitor, minority carriers (holes) holes are available in principle, but the radial components of the electric field at the borders of the gate are not strong enough to attract enough holes sufficiently fast in order to respond to the capacitance signal. Like for silicon, only thermally created carriers are therefore available to charge the cloud of minorities underneath the gate, which therefore leads to the usual high frequency behavior already at very low frequencies.

To illustrate the situation quantitatively, Fig. 3 shows a two-dimensional simulation of the total carrier density, accumulated by the static electric field generated by the surface states and the charges confined in the oxide layer from accumulation to inversion: (a) : substrate bias (tip on ground): +3.6 V, (b): -0.2 V and (c): -1.8 V.

In all cases, the calculated value of the surface potential due to charged surface states and the electric charges confined in the oxide was 0.75 V, which was obtained by fitting the experimental C(V) curves to our model. As one can see in Fig.3 (a), we have strong accumulation conditions at +3.6 V, which means that the electric field generated by the tip apex (30nm x 30nm) clearly penetrates the cloud of minorities. At a substrate bias of -0.2 V the distribution of minority carriers at the surface is quite homogeneous (see Fig. 3 (b)), but rapidly increases underneath the tip at -1.8 V. This is seen nicely in Fig. 3 (c), which shows the large amount of accumulated minorities close to the tip apex. What is also seen nicely, is the permanent minority carrier concentration around the tip apex, which is responsible for the fact that the cloud of inversion carriers can always respond to the capacitance signal so that C(V) curves with low frequency behavior are observed experimentally. The size of the simulation area in Fig. 3 (a)-(c) was 1 μm x 1 μm.

We now try to estimate the frequency at which the transition between low frequency and high frequency is observed in an analytical way. For this purpose we start with the concentration of minority carriers (holes) at the surface of the wafer, which can be calculated

from the band bending at the surface, which is caused by the charged surface states and the oxide charges. Using the well known formula for the concentration of holes in non - degenerate semiconductors: $p = N_V e^{-\frac{(E_F - E_V)}{kT}}$, a value for the valence band density of states in GaAs of N_V = $9 \cdot 10^{18}$cm^{-3}, and a value of 0.75 V for the surface potential at zero bias, (obtained from a quantitative analysis of the C(V) spectra), we finally obtain a value of p ≈ 1.35 10^8 cm^{-3}. With this, we now can calculate the resistivity at the sample surface using the expression $\rho = 1/ep\mu_p$, where μ_p=300 cm^2/Vs is the hole mobility in GaAs and e = 1.6 10^{-19}C. The procedure yields a value of ρ ≈$1.5 \cdot 10^8$ Ωcm. We now calculate the spreading resistance of a point contact using the expression $R_S = \rho/2\pi r_0$= 8.2 10^{12}Ω, where r_0 is the SCM tip radius (30nm). Using the contact capacitance after background subtraction, we can estimate a typical RC time constant of our system, which finally yields a measure for the transition frequency between the high frequency and low frequency behavior of the corresponding C(V) curves. Inserting into $f = \frac{1}{2\pi R_S C_i}$, we get a value of 3.4 kHz, which is in surprisingly good agreement with our experimental observations. If the contact radius is increased to the device scale (800nm) the resistance will be decreased linearly, but the capacitance will increase quadratically, finally leading to transition frequencies in the order of 10 Hz as they are usually observed in macroscopic devices.

In summary, the low frequency behavior of C(V) curves observed in Scanning Capacitance Spectroscopy on MOS-type tip-sample contacts on GaAs substrates was discussed. It was found that the low frequency behavior of the C(V) curves on GaAs is caused by minority carriers, which are accumulated around the AFM tip due to the natural surface depletion field. Using a two-dimensional self-consistent Poisson solver and taking the actual geometry of the SCM tip into account, the concentration of minority carriers around the tip

apex was calculated quantitatively. This also allowed an analytic estimation of the transition frequency below which a low frequency behavior in our SCS spectra can be observed.

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Figure captions:

Figure 1: (a) C(V) curves of a MOS-type GaAs tip-sample contact with Al_2O_3 oxide layer (d=7 nm) for various frequencies: (1): 140 Hz, (2): 300 Hz, (3): 1.2 kHz, (4): 5 kHz, (5): 10 kHz, (6): 20 kHz. Substrate doping was $N_D = 1 \times 10^{16}$ cm^{-3}. (b): SCS data obtained on an Al_2O_3 - Silicon structure at a frequency of f=140 Hz, together with the C(V) curve of a macroscopic Al-Al_2O_3 – Silicon device (area 0.2 mm x 3 mm).

Figure 2: Electric field lines of a GaAs MOS-type sample for a large area device with a gate area of 800 nm x 800 nm (a) and (b) an AFM tip having a contact area of 30 nm × 30 nm. The applied substrate bias is - 0.2V for both cases.

Figure 3: Simulated charge carrier concentration of MOS- type tip-sample contacts on a GaAs substrate having a doping concentration of $N_D = 1 \times 10^{16}$ cm^{-3} for various substrate bias values: (a) +3.6 V (b) -0.2 V and (c) -1.8 V. The size of the simulation area is 1 μm x 1 μm.

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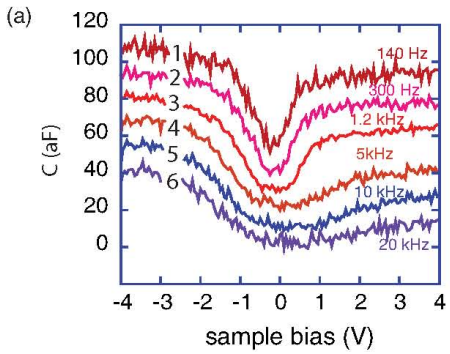
(a)
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3
4
5
6
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1.2 kHz
5kHz
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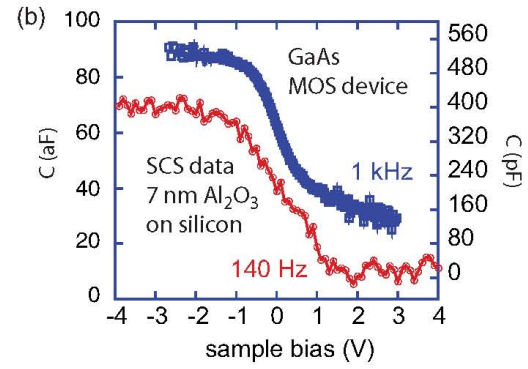
(b)
C (aF)
C (pF)
sample bias (V)
GaAs
MOS device
SCS data
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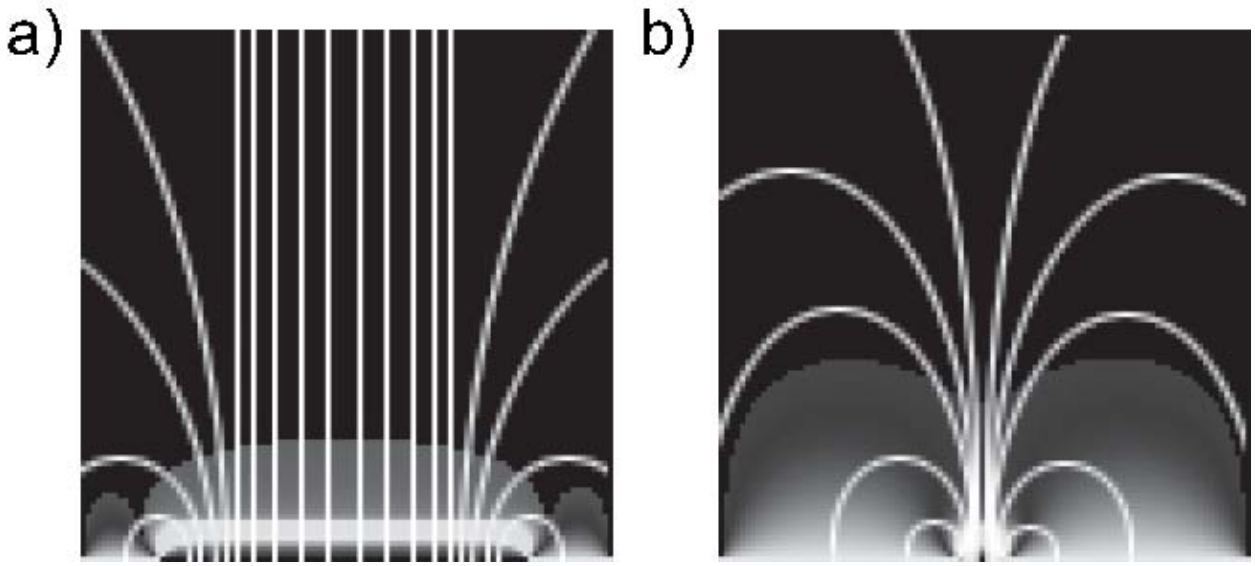
on silicon
1 kHz
140 Hz


a)
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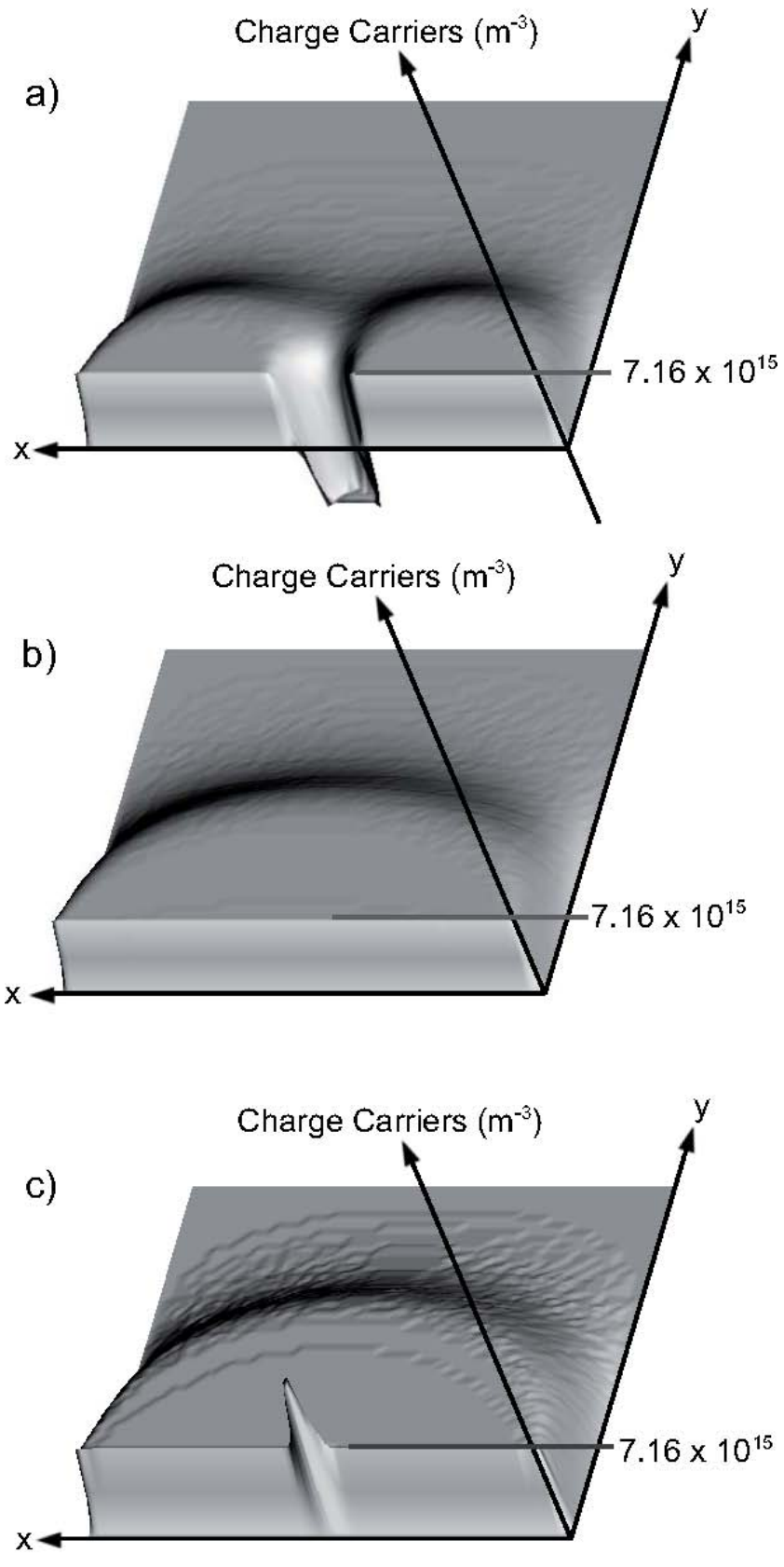
a)
Charge Carriers (m^{-3})
y
x
7.16×10^{15}
b)
Charge Carriers (m^{-3})
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7.16×10^{15}
c)
Charge Carriers (m^{-3})
y
x
7.16×10^{15}

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