A Control Concept for Battery Emulators Using a Reference Governor With a Variable PT1-Element for Constraint Handling

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ABSTRACT This paper presents a method for highly dynamic nonlinear control of DC-DC converters with constraints used in battery emulators. Controlling this system is particularly challenging as the connected units-under-test often behave like constant power loads (CPLs), which introduce unstable system dynamics and render the system nonlinear. In order to achieve fast output dynamics with the DC-DC converters over a large operating range, a special control architecture is proposed where feedback equivalence is established between a nonlinear system description and a linear description. The nonlinear system dynamics can then be transformed into linear ones for controller synthesis by exploiting the flatness property of the system. Additionally, constraints have to be met at any time during operation to prevent damage to components. In order to satisfy the constraints, a reference governor (RG) is added to the loop. This novel RG concept uses a low-pass filter in the shape of a PT1-element to modify the voltage reference. By changing the time constant of the PT1-element, the RG is able to generate smooth constraints-aware trajectories for setpoint changes. Finally, the capabilities of the control concept are demonstrated and discussed based on high-fidelity simulations.

INDEX TERMS Constant power load, constraints handling, DC-DC step-down converter, reference governor, flatness-based control.

I. INTRODUCTION

The electrification of automotive powertrains is an ongoing topic that has attracted significant interest in the past. Generally, an onboard battery provides the energy required to power the powertrain components in an electric vehicle. To shorten development times, individual components are commonly tested in hardware-in-the-loop (HIL) environments. However, using batteries in HIL tests is not only cumbersome as they must be pre-charged and pre-conditioned to achieve the required initial conditions, it is also dangerous, as a faulty unit under test (UUT) can lead to short circuits and fires. A much safer and more efficient solution for HIL testbeds is to use an emulated battery to perform tests in a power-hardware-in-the-loop (P-HIL) testing environment [1]. Consequently, replacing the physical

battery with a battery emulator is highly beneficial in those setups.

Typically, a battery emulator is realized as a DC-DC converter combined with a real-time-capable battery model that generates a reference trajectory for the output voltage [2]. As with every physical system, the DC-DC converter is subject to constraints due to physical limits [3]. If those constraints are not satisfied at all times, component damage is imminent.

A well-known method for constraint handling is limiting the input action. The underlying control scheme in this method is generally not designed with this input saturation in mind, which can lead to stability issues or integrator windup phenomena [3]. Furthermore, this method cannot be easily expanded to enforce constraints on the states. On the other hand, a control scheme designed with the constraints
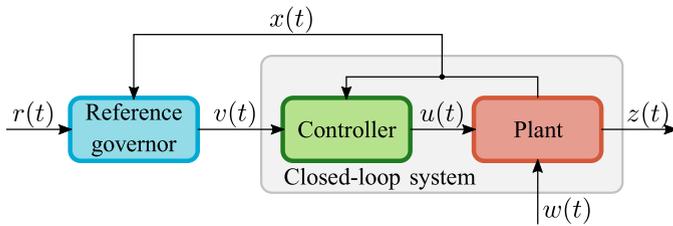
FIGURE 1. Principle of a reference governor applied to a closed-loop system. The external reference r is modified, resulting in the internal reference v, such that the constraints are met $z \in \mathcal{Z}$.

in mind is model predictive control (MPC). In an MPC scheme, future input trajectories are computed by solving a constraint optimization problem at each time step. However, solving such optimization problems is computationally expensive. This is particularly problematic in systems where high sampling frequencies are desired, such as in the presented battery emulator [4]. Considering that future power electronics converters will have even higher switching frequencies (and consequently sampling frequencies), it becomes clear that even modern processors will be pushed to their limits. Another method is modifying the reference for the controller to avoid steering the closed-loop system into constraint regions, as seen in Fig. 1. This so-called reference governor (RG) is an add-on to an existing control concept and can be used to satisfy state and control constraints [5]. Partially contributing to its success, an RG has attractive properties like recursive feasibility and finite-time convergence while also having manageable online computational requirements [6]. Multiple modifications to the original RG introduced by [7] have been proposed throughout the years. The reader is encouraged to check out [5] for an excellent overview of different RG schemes. RGs have been applied (in their original and modified forms) in numerous fields like automotive applications [8], battery management [9], or DC-DC converters [10].

This paper presents a control concept with constraints handling capabilities for battery emulators used in automotive testbeds. As battery emulators are high-performance testing equipment tasked to emulate the almost instantaneous response of a battery, requirements for a highly dynamical output voltage exist [11]. Furthermore, the emulator should operate over a broad range of voltages to emulate a wide variety of battery topologies. Those requirements differ from the usual requirements for conventional power converters, which are typically designed for a single nominal operating point [12]. In order to protect the internal components of the battery emulator from damage and ensure proper operation, a series of constraints must be satisfied. Another difficulty arises when the connected UUT behaves like a constant power load (CPL). An example of an UUT drawing constant power would be a tightly controlled motor inverter [13]. Not only does this lead to nonlinear behavior, but it also destabilizes the system. In order to meet the requirements for a highly dynamical output voltage, a flatness-based controller was proposed in [1]. It has been shown that this controller can stabilize the

unconstraint system over its entire operating range [2]. However, constraints satisfaction is not guaranteed with this controller alone. In order to add constraint handling capabilities during setpoint changes to the control concept, a novel RG scheme is introduced. In this RG, the trajectory of the reference voltage is low-pass filtered via a PT1-element (also known as a first-order lag element) with a variable time constant. The RG then solves an optimization problem in a receding horizon fashion to find the fastest time constant of the PT1-element where no constraints are violated during a setpoint change. By including the PT1-element in the RG scheme, a smoother transition between setpoints can be achieved compared to an RG without the PT1-element. Additionally, the inclusion of the PT1-element also reduces oscillations during setpoint changes.

The remainder of this paper is structured as follows: Section II describes the battery emulator system in more detail, while Section III briefly recaps the utilized control concept proposed in [1]. The constraints given by the physical limits of the system are investigated in Section IV. In Section V, the RG with PT1-element concept is presented, while Section VI shows simulation results detailing the advantages of the RG concept. Section VII offers a comparison to a traditional RG concept without PT1-element. The contents are discussed in Section VIII, and the paper is concluded in Section IX.

II. SYSTEM DESCRIPTION

The electrical circuit of a bidirectional multiphase DC-DC step-down converter used in a battery emulator is illustrated in Fig. 2. This circuit can be separated into the converter stage and the output stage. The switching devices in the converter stage are Insulated Gate Bipolar Transistors (IGBTs), which are controlled via PWM signals with a maximum switching frequency of 12 kHz. However, due to the 4-fold interleaved parallel topology an effective switching frequency of 48 kHz is achieved at the output. The inductance L_1 is chosen for approximately 10 % current ripple in each leg. The dynamic behavior of the total converter stage current i_1 can be approximated via $\frac{\mathrm{d}}{\mathrm{d}t} i_1 = u$, where u is constant over one PWM period, see [1]. The filter capacitance C_1 is chosen for a resonance frequency well below the switching frequency. It is connected to the UUT via a parasitic inductance L_2, caused by the self-inductance of the DC cables. Typically, the converter is located outside the testbed room, such that cable lengths of several tens of meters is often needed. The UUT itself consists of the capacitance C_2 and the CPL. Since the CPL draws constant power, the current $i_p = \frac{P}{v_2}$ is nonlinear with respect to v_2. The whole system is connected to the supply voltage V_{cc}. Finally, one arrives at the following system of differential equations:

$$\frac{\mathrm{d}v_2}{\mathrm{d}t} = \frac{1}{C_2}\left(i_2 - \frac{P}{v_2}\right), \quad (1a)$$

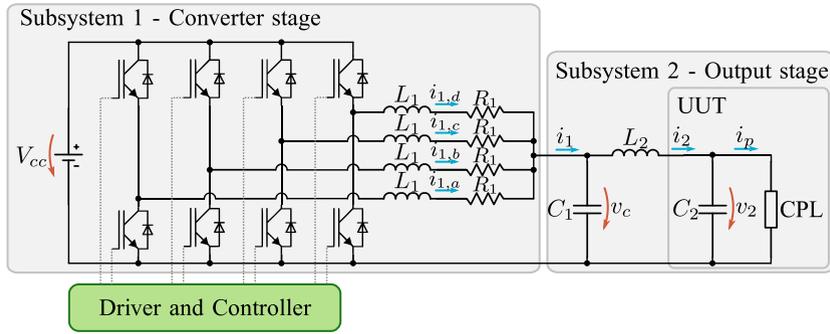$$\frac{\mathrm{d}i_2}{\mathrm{d}t} = \frac{1}{L_2}\left(v_c - v_2\right), \quad (1b)$$

FIGURE 2. The 4-leg bidirectional DC-DC step-down converter can be separated into two subsystems.

$$\frac{dv_c}{dt} = \frac{1}{C_1}(i_1 - i_2), \tag{1c}$$

$$\frac{di_1}{dt} = u. \tag{1d}$$

The output voltage $y = v_2$ should track an external reference voltage r generated by the battery model while also adhering to the physical limits of the circuit, which are given by the following constraints:

$$-i_{1,\text{limit}} \leq i_1 \leq i_{1,\text{limit}}, \tag{2a}$$

$$-i_{2,\text{limit}} \leq i_2 \leq i_{2,\text{limit}}, \tag{2b}$$

$$\frac{-4v_c}{L_1} \leq u \leq \frac{4V_{cc} - 4v_c}{L_1}. \tag{2c}$$

While the inequalities given by (2a) and (2b) represent the maximal rating of the components, the inequalities given by (2c) are owed to the fact that the duty-cycle of the PWM signals has to lie between 0% and 100%. With the state-vector given as $x = [v_2, i_2, v_c, i_1]^T$ one can write down the differential equations (1) as the nonlinear state space model Σ_{nl} in the form:

$$\Sigma_{nl} : \begin{cases} \dot{x} = f(x, P) + gu, & \text{(3a)} \\ y = v_2, & \text{(3b)} \end{cases}$$

where y is the controlled output of the system. Additionally, the constraints given by (2) can be expressed as

$$z = C_z x + D_z u, \quad z \in \mathcal{Z}, \tag{4}$$

where z defines an additional output of the model Σ_{nl}, whose components must lie in the compact convex set $\mathcal{Z}$. Note that even though this so-called constraint output is linear with respect to x and u, the state dynamics in (3a) are nonlinear. However, the system is differentially flat [14] with y having full relative degree (as shown in [2]), which allows the application of a flatness-based control concept.

III. FEEDBACK CONTROLLER DESIGN

As outlined previously, a real-time capable battery model generates a suitable voltage reference for the DC-DC converter. In order to achieve representative testing results, the converter has to follow this reference as fast as possible. Additionally
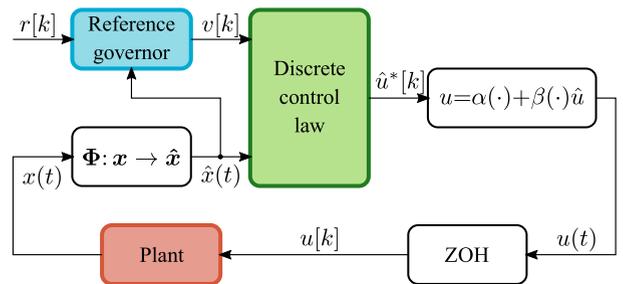

FIGURE 3. Overview of the flatness-based control concept from [1] with a reference governor. For ease of illustration, the influence of P is not shown.

to the requirement for a highly dynamic output, there exists a requirement for a large operating range in order to emulate various battery topologies. Furthermore, the controlled input u for Σ_{nl} has to be constant over one PWM period. Such an input can be realized using a discrete-time control law with a sampling time of $T_s = f_{\text{PWM}}^{-1}$, where f_{PWM} is the frequency of the PWM signal. However, synthesizing a discrete-time control law requires a discrete-time system representation, and due to the nonlinearity introduced by the CPL, the system Σ_{nl} cannot be discretized exactly. It has been shown in [1] that by implementing a flatness-based control concept, it is possible to still arrive at an (almost) constant input over one T_s, which also satisfies the requirements for a highly dynamic output voltage and a large operating range. The main idea behind this concept is to establish feedback equivalence between the nonlinear system Σ_{nl} and a linear system Σ_l. The linear system is then discretized exactly and used to design a control law according to the specifications. Finally, this control law is transformed to be applicable to the nonlinear system Σ_{nl}. Fig. 3 illustrates the essential steps for implementing such a flatness-based control concept; further details can also be found in [1].

By exploiting the differential flatness of the system, one can find a diffeomorphism $\mathbf{\Phi} : x \to \hat{x}$, such that the nonlinear dynamics of the system are rendered linear. The resulting linear system is then given by

$$\Sigma_l : \begin{cases} \dot{\hat{x}} = A_l \hat{x} + B_l \hat{u} + E_l P, & \text{(5a)} \\ \hat{y} = C_l \hat{x}, & \text{(5b)} \end{cases}$$

In order to establish feedback equivalence between Σ_{nl} and Σ_l, a state feedback law in the shape of $u = \alpha(\mathbf{x}, P) + \beta(\mathbf{x}, P)\hat{u}$ has to be defined, such that the smooth functions $\alpha(\cdot)$ and $\beta(\cdot)$ map Σ_{nl} into Σ_l. Note that the transformation given by $\mathbf{\Phi}$, α, and β is not uniquely defined, as one can transform the nonlinear dynamics into any (linear) flat system with a full relative degree. Commonly, the dynamics of Σ_l are chosen as a chain of integrators [15], but one could also use the linearized dynamics of Σ_{nl} around a steady-state operating point [2].

As the system dynamics given by (5a) are linear, the system Σ_l can be discretized exactly with a zero-order-hold (ZOH) element on the input and a sampling time of T_s, yielding

$$\Sigma_d : \begin{cases} \hat{\mathbf{x}}[k+1] = \mathbf{A}_d \hat{\mathbf{x}}[k] + \mathbf{B}_d \hat{u}[k] + \mathbf{E}_d P[k], & (6a) \\ \hat{y}[k] = \mathbf{C}_d \hat{\mathbf{x}}[k], & (6b) \end{cases}$$

where $\hat{\mathbf{x}}[k+1]$ and $\hat{\mathbf{x}}[k]$ with $k \in \mathbb{Z}^+$ are short-hand notations for $\hat{\mathbf{x}}((k+1)T_s)$ and $\hat{\mathbf{x}}(kT_s)$ respectively, which are also applicable to other variables. A transformation into a discrete-time system is necessary for various reasons: It is required to implement the controller on digital hardware with a limited sampling frequency and finite computation speed. Furthermore, the dynamics of the switches in the converter stage are approximated with a constant $\frac{d}{dt}i_1 = u$ over one PWM period. The latter is implicitly satisfied by including a ZOH element on the input with T_s being the length of one PWM period. Using Σ_d to design a discrete-time controller that meets the dynamical requirements, the linear control law is given as

$$\hat{u}^*[k] = -\mathbf{K}_x \hat{\mathbf{x}}[k] + K_v v[k] + K_p P[k], \qquad (7)$$

where v is the reference output voltage and $\mathbf{K}_x$, K_v, and K_p are the state-feedback gain, the pre-filter gain, and the disturbance gain respectively. Note that $\hat{u}^*[k]$ cannot be applied to the plant directly, as it is valid for the dynamics given by Σ_l. However, $\hat{u}^*[k]$ defines a stabilizing output trajectory for Σ_l. The required input u for Σ_{nl} to follow the same stabilizing trajectory as Σ_l can be found as

$$u(t) = \alpha(\mathbf{x}(t), P) + \beta(\mathbf{x}(t), P)\hat{u}^*[k]. \qquad (8)$$

With this transformation of $\hat{u}^*[k]$ into $u(t)$, feedback equivalence is established between Σ_l and Σ_{nl}. The final nonlinear control law for Σ_{nl} is given by combining the diffeomorphism $\mathbf{\Phi}$, (7), and (8). Using this control law to compute the input of the plant would allow for highly dynamic performance over a large operating range. However, even though $\hat{u}^*[k]$ is constant over one T_s, $u(t)$ is generally not after the transformation given by (8) as α and β are state-dependent (and consequently time-dependent). In order to arrive at a $u[k]$ that is constant over one T_s, a ZOH element is introduced, as seen in Fig. 3. This ZOH element samples the input $u(t)$ at every $t = kT_s$, $k \in \mathbb{Z}^+$ and keeps it constant over $u(\tau) \equiv u[k]$, $\tau \in [kT_s, (k+1)T_s)$. Alternatively, this behavior can also be modeled as an input distortion δu such that

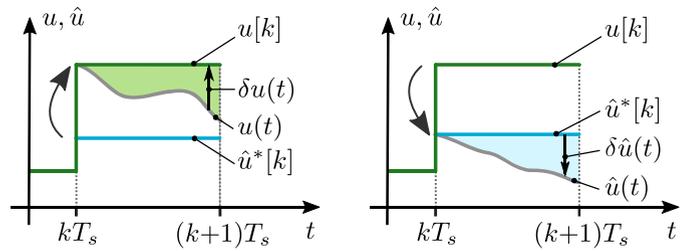$$u[k] = u(t) + \delta u(t) \qquad (9)$$

FIG. 4. Influence of the ZOH element on the input u. Left: Input distortion $\delta u(t)$ when transforming from $\hat{u}^*[k]$ into $u(t)$. Right: Equivalent input distortion $\delta \hat{u}(t)$ of Σ_l for a given constant $u[k]$.

holds, as illustrated on the left part of Fig. 4. The input distortion δu of Σ_{nl} can also be expressed as an equivalent input distortion $\delta \hat{u}$ of Σ_l such that

$$u[k] = \alpha(\mathbf{x}(t), P) + \beta(\mathbf{x}(t), P)(\hat{u}^*[k] + \delta \hat{u}(t)) \qquad (10)$$

is satisfied, shown on the right part of Fig. 4. Finally, applying the distorted input $\hat{u}(t) = \hat{u}^*[k] + \delta \hat{u}(t)$ with (7) to (6) yields the closed-loop system

$$\Sigma_{cl} : \begin{cases} \hat{\mathbf{x}}[k+1] = \mathbf{A}\hat{\mathbf{x}}[k] + \mathbf{B}v[k] + \mathbf{E}P[k] + \mathbf{w}[k], & (11a) \\ \hat{y}[k] = \mathbf{C}\hat{\mathbf{x}}[k], & (11b) \end{cases}$$

where the disturbance caused by $\delta \hat{u}(t)$ is given as

$$\mathbf{w}[k] = \int_{\tau=kT_s}^{(k+1)T_s} e^{\mathbf{A}_l((k+1)T_s - \tau)} \mathbf{B}_l \delta \hat{u}(\tau) \, d\tau. \qquad (12)$$

A similar case of input disturbance was investigated in [3], where a safety margin for constraints satisfaction was computed. For simplicity, in the presented case it is assumed that $\mathbf{w}[k] \in \mathcal{W}$, $\forall k \in \mathbb{Z}^+$, with $\mathcal{W}$ being a compact convex set $\mathcal{W} \subset \mathbb{R}^4$ containing the origin $\mathbf{0} \in \mathcal{W}$. Furthermore, the following assumptions are also considered:

Assumption 1: The unconstrained ($\mathbf{z} \in \mathcal{Z}$), disturbance-free ($\mathbf{w} = 0$), closed-loop system Σ_{cl} is asymptotically stable, i.e., all eigenvalues of $\mathbf{A}$ are strictly inside the unit circle.

Assumption 2: For $\lim_{k \to \infty}$ the closed-loop system output $\hat{y}[k] \equiv v[k]$ for any $P[k]$, if $\mathbf{z}[k] \in \mathcal{Z}$.

Remark 1: While assumption 1 only guarantees stability for the disturbance-free case, stability can also be shown for the system with a disturbance $\mathbf{w}$ given by (12), see [2] for more details.

Assumptions 1–2 are reasonable for controlled closed-loop systems in regions where the constraints $\mathbf{z} \in \mathcal{Z}$ are easily satisfied. However, the controller alone does not ensure that the closed-loop system will always stay in those regions. Especially during setpoint changes, the controller can cause trajectories where $\mathbf{z} \notin \mathcal{Z}$. In order to ensure that the system will only be operated in regions where $\mathbf{z} \in \mathcal{Z}$, a RG scheme is proposed.

IV. CONSTRAINTS TRANSFORMATION
The physical limits of the system presented in (2) are given as a linear combination of the states $\mathbf{x}$ and the input u of

the nonlinear model Σ_{nl} in (4). However, after applying the diffeomorphism $\mathbf{\Phi}$, which transforms the nonlinear dynamics of Σ_{nl} into linear ones, the former linear constraints become nonlinear. Expressing (4) in terms of $\hat{\mathbf{x}}$ and $\hat{u}$ results in

$$z = \mathbf{C}_z \mathbf{\Phi}^{-1}(\hat{\mathbf{x}}, P) + \mathbf{D}_z \alpha(\mathbf{\Phi}^{-1}(\hat{\mathbf{x}}, P), P)$$

$$+ \mathbf{D}_z \beta(\mathbf{\Phi}^{-1}(\hat{\mathbf{x}}, P), P)\hat{u}, \quad (13)$$

where $\mathbf{\Phi}^{-1}(\hat{\mathbf{x}}, P) = \mathbf{x}$ is a function describing the inverse of the diffeomorphism $\mathbf{\Phi} : \mathbf{x} \rightarrow \hat{\mathbf{x}}$ depending on P. Note that $z \in \mathcal{Z}$ still has to hold for constraints satisfaction. For high sampling frequencies, the constraint can be relaxed by only requiring satisfaction at discrete time steps $t = kT_s$, where $k \in \mathbb{Z}^+$. Those so-called pointwise-in-time constraints [16] are expressed as

$$z[k] = \mathbf{C}_z \mathbf{\Phi}^{-1}(\hat{\mathbf{x}}[k], P[k]) + \mathbf{D}_z \alpha(\mathbf{\Phi}^{-1}(\hat{\mathbf{x}}[k], P[k]), P[k])$$

$$+ \mathbf{D}_z \beta(\mathbf{\Phi}^{-1}(\hat{\mathbf{x}}[k], P[k]), P[k])\hat{u}^*[k], \quad z[k] \in \mathcal{Z}. \quad (14)$$

It is worth mentioning that the input distortion $\delta\hat{u}$ does not appear in the above equation, as it vanishes at $t = kT_s$, due to $\hat{u}(t) \equiv \hat{u}^*[k]$. By inserting the control law given by (7) into (14), one can write the constraint output equation of the closed-loop system Σ_{cl} as the nonlinear function

$$z[k] = \mathbf{h}(\hat{\mathbf{x}}[k], v[k], P[k]), \quad (15)$$

where $z[k] \in \mathcal{Z}$ has to hold. Even though the set $\mathcal{Z}$ is convex, the nonlinear function $\mathbf{h}(\cdot)$ is generally no longer convex, possibly rendering the constraints non-convex. Methods for dealing with non-convex constraints in RG schemes have been presented, e.g., in [17], [18].

V. PT1 REFERENCE GOVERNOR DESIGN
In order to handle constraints in the shape of $z[k] \in \mathcal{Z}$ in the discrete-time closed-loop system Σ_{cl}, a RG scheme was developed. The basic idea of an RG is to low-pass filter the external reference r, creating the internal reference v, which ensures constraints satisfaction in the closed-loop. The low-pass filter is realized in the presented RG scheme as a PT1-element, also known as a first-order lag element, with a fixed static gain of 1. By changing the time constant of the PT1-element, the time evolution of the internal reference v can be modified. The RG with a PT1-element as a low-pass filter (PT1-RG) achieves a smooth transition between setpoints in the presented setting. A discrete-time PT1-element with unit gain can be expressed via

$$v[k] = v[k-1] + \kappa(r[k] - v[k-1]), \quad (16)$$

where $\kappa \in [0, 1]$ is related to the time constant, see Fig. 5. One can see that $\kappa = 0$ leads to a rejection of any external reference changes. Instead, the previous value of v is used in the next time step. On the other hand, $\kappa = 1$ results in a $v \equiv r$, meaning that the internal reference follows the external one exactly. In order to achieve the fastest possible tracking behavior, the PT1-RG is tasked to find the
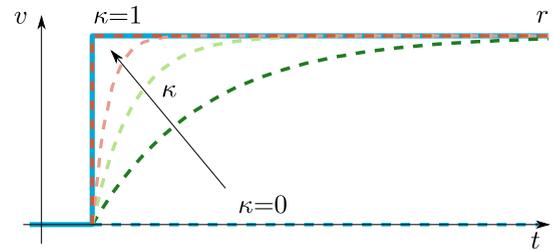

FIG. 5. Time evolution of the internal reference v generated by the PT1-element for the PT1-RG with different values of κ (dashed lines) when following an external reference r (solid line).

maximal value of κ, termed κ^*, which does not lead to constraint violation. The resulting optimization problem for $\kappa^* = \kappa^*(r[k], v[k-1], \hat{\mathbf{x}}[k], P[k])$ is given by:

$$\kappa^* = \max_{\kappa \in [0,1]} \kappa \quad (17a)$$

$$\text{s.t.} \quad \tilde{\mathbf{x}}[n+1] = \mathbf{A}\tilde{\mathbf{x}}[n] + \mathbf{B}\tilde{v}[n] + \mathbf{E}P[k] + \mathbf{w}, \quad (17b)$$

$$\tilde{v}[n] = \tilde{v}[n-1] + \kappa(r[k] - \tilde{v}[n-1]), \quad (17c)$$

$$\tilde{\mathbf{x}}[0] = \hat{\mathbf{x}}[k], \quad (17d)$$

$$\tilde{v}[-1] = v[k-1], \quad (17e)$$

$$\mathbf{h}(\tilde{\mathbf{x}}[n], \tilde{v}[n], P[k]) \in \mathcal{Z}, \ \forall \mathbf{w} \in \mathcal{W}, \ \forall n = 0, \dots, n^*, \quad (17f)$$

where n is the prediction index used to compute the future values of $\tilde{\mathbf{x}}$ with $\tilde{v}$. The initial values for the predictions are initialized in (17d)–(17e) with $\hat{\mathbf{x}}[k]$ and $v[k-1]$ respectively. Constraints satisfaction is enforced via (17f) over the prediction horizon, where $\mathbf{h}(\cdot)$ was derived in (15). The length of the prediction horizon n^* has to be chosen so that prediction steps $n > n^*$ no longer contribute to the constraints. It can be shown that (17) has a so-called finite determination property [19], meaning that there exists a finite value for n^*. Computation of n^* can be carried out offline, although any upper bound for n^* can also be used instead. An algorithm for solving (17) via bisections is given in [17].

VI. RESULTS
A. SIMULATION SETUP
A series of simulations were performed to showcase the necessity and advantages of the PT1-RG scheme. All simulations were implemented in MATLAB Simscape utilizing validated high-fidelity models, including nonlinear switching characteristics and equivalent series resistance components for the capacitors. It has been shown in earlier works [1], [20], [21], that the simulations agree well with results from HIL tests. The simulated battery emulator is rated for a maximum of 250 kW at high voltages. However, at low voltages the maximum current rating is decisive: The converter stage can deliver a maximum continuous output current of 700 A, while the output stage can briefly handle 800 A. The controller is designed to dynamically stabilize the output voltage in the range from 48 V to 800 V for UUTs that behave like a CPL

TABLE I Nominal Parameters of the Model

Description	Notation	Value
DC-link voltage	V_{cc}	820 V
Resistance of each leg	R_1	0 mΩ/1 mΩ*
Inductance of each leg	L_1	300 μH
Inductance of the cable	L_2	25 μH
Capacitance of converter filter	C_1	425 μF
Capacitance of output filter	C_2	2.3 mF
Maximum converter stage current	$i_{1,\text{limit}}$	700 A
Maximum output stage current	$i_{2,\text{limit}}$	800 A
Sampling time	T_s	83.33 μs
Switching frequency	f_{PWM}	12 kHz

*Nominal value for controller synthesis was 0 mΩ, while the value used for simulation was 1 mΩ.

while also delivering a fast rise time of 1 ms for unconstrained setpoint changes. The nominal values given in Table I were utilized for all simulations. Note that a nominal resistance value of $R_1 = 0$ mΩ was used for controller synthesis; however, the simulations were carried out with a value of $R_1 = 1$ mΩ.

B. SINGLE SETPOINT CHANGE

In the first set of simulations, a single setpoint change is investigated. These simulations aim to illustrate the need for a constraint management concept by showcasing the peak currents demanded by the controller during large setpoint changes. The simulations are carried out with the UUT turned off ($P = 0$ kW), illustrating that this issue is not just limited to CPL-like UUTs. In the first simulation, no constraint management scheme is used. The results of this simulation can be seen in Fig. 6, where the upper plot shows the output voltage $y = v_2$ and the internal and external references v and r. As no RG is utilized, $v \equiv r$. The middle plot shows the controlled variable $u = \frac{d}{dt}i_1$, and the limits given by 0 % and 100 % duty cycle respectively. In the lower plot, the currents i_1 and i_2 are illustrated, as well as their respective limits. As expected, the resulting rise time of the output voltage is approximately 1 ms [1]. However, the peak converter stage current demanded by the controller is 1250 A, which also results in a peak current in the output stage of more than 1700 A. Such high currents would trip the fail-safe in the device, resulting in an emergency shutdown to prevent component damage. Furthermore, the requested $\frac{d}{dt}i_1$ would have required a duty cycle of more than 100 %, which is physically impossible.

The PT1-RG was implemented to handle the constraints in the second simulation. The simulation results are illustrated in Fig. 7. Looking at the upper plot, one can see that the PT1-RG manipulated the internal reference v according to (17). This modification resulted in a slower rise time of 1.5 ms. However, the constraints were satisfied during the setpoint change: All the currents were within their limits, as well as the requested $\frac{d}{dt}i_1$.

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[1]The rise time is measured from requesting the setpoint change to achieving 90 % of the step-height.
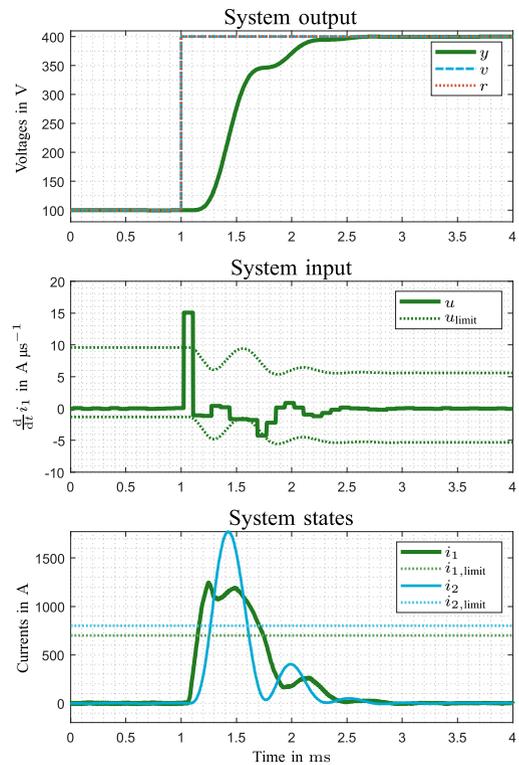
FIG. 6. Simulation results without an RG, performing a single setpoint change with $P = 0$ kW.

C. MULTIPLE SETPOINT CHANGES

Another simulation was carried out to showcase the performance of the developed PT1-RG concept for different setpoint changes. The UUT was turned on for this simulation, drawing a constant power of $P = 50$ kW. First, a series of smaller setpoint changes were carried out in the region of 100 V to 400 V, see Fig. 8. After that, a large setpoint change from 100 V to 700 V is carried out, followed by another setpoint change from 700 V down to 100 V. In the upper plot of Fig. 8, one can see how the PT1-RG manipulated the internal reference v depending on the voltage level and height of the step. The controlled variable stays in the feasible region throughout the simulation, as illustrated in the middle plot. Also, the currents i_1 and i_2 stay within their respective limits, as can be seen in the lower plot of Fig. 8.

Most importantly, the RG computed an internal reference $v \neq r$ only when violations of the constraints were imminent (e.g., during the initial step or the larger steps). During non-critical setpoint changes, the internal reference followed the external one, resulting in fast rise times. Of equal importance, there were no oscillations in the currents during constraint operation.

VII. COMPARISON TO CLASSICAL REFERENCE GOVERNOR DESIGN

This section aims to describe the differences between the PT1-RG and a *classical* RG design, as seen, e.g., in [6]. Similar to before, a low-pass filter is used to generate the internal
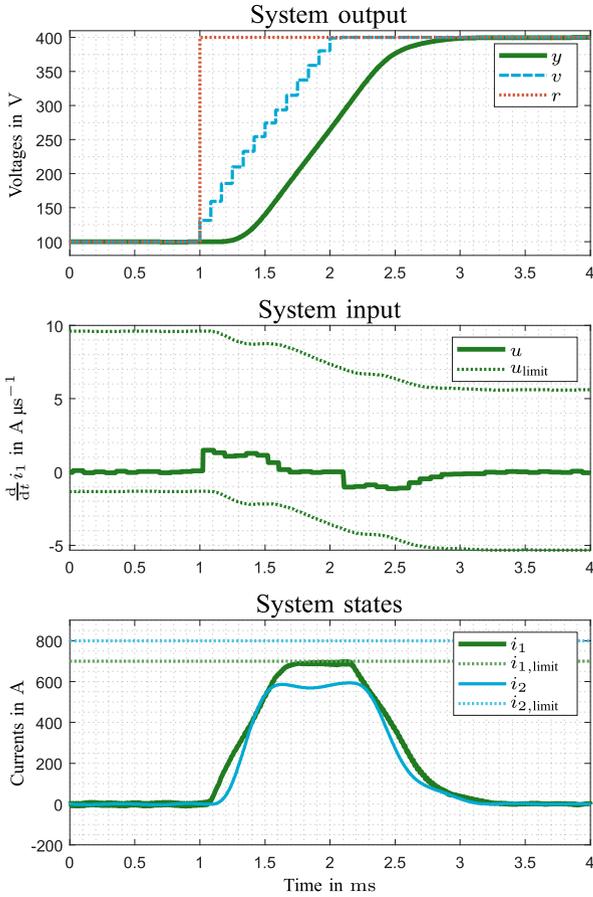
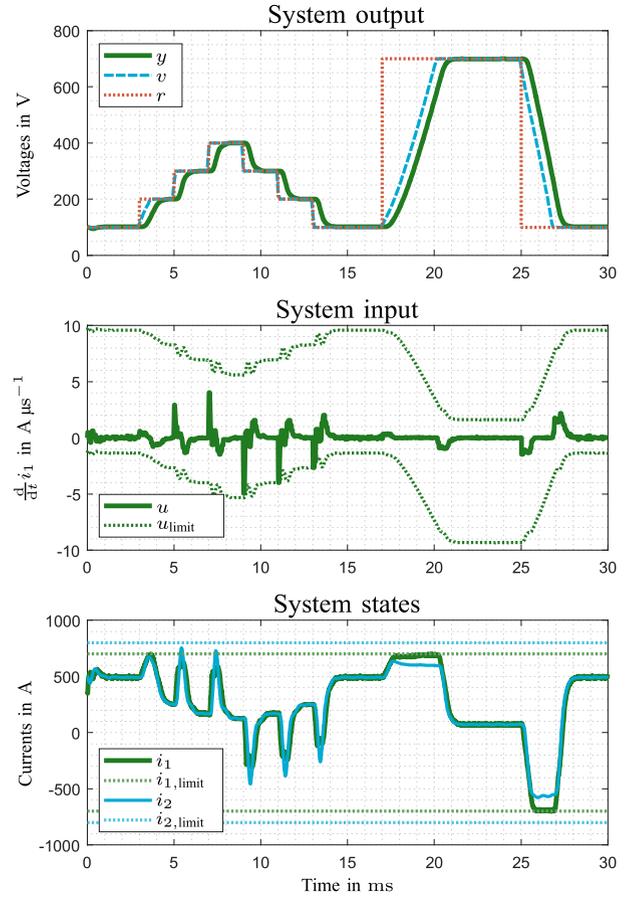**FIG. 7.** Simulation results with a PT1-RG, performing a single setpoint change with $P = 0\,\text{kW}$.

FIG. 8. Simulation results with a PT1-RG, performing multiple setpoint changes with $P = 50\,\text{kW}$.

reference v. However, the predicted future reference values $\tilde{v}$ do not follow any internal dynamics; rather, they are kept constant:

$$\tilde{v}[\infty] = \cdots = \tilde{v}[k+1] = \tilde{v}[k] = v[k-1] + \kappa(r[k] - v[k-1]),$$
$$(18)$$

where κ is again $\in [0, 1]$, as seen in Fig. 9. The resulting optimization problem for $\kappa^* = \kappa^*(r[k], v[k-1], \hat{x}[k], P[k])$ in this case is then given by:

$$\kappa^* = \max_{\kappa \in [0,1]} \kappa \tag{19a}$$

$$\text{s.t.} \quad \tilde{x}[n+1] = A\tilde{x}[n] + B\tilde{v}[n] + EP[k] + w, \tag{19b}$$

$$\tilde{v}[n] = v[k-1] + \kappa(r[k] - v[k-1]), \tag{19c}$$

$$\tilde{x}[0] = \hat{x}[k], \tag{19d}$$

$$h(\tilde{x}[n], \tilde{v}[n], P[k]) \in \mathcal{Z}, \ \forall \, w \in \mathcal{W},$$

$$\forall \, n = 0, \dots, n^*. \tag{19e}$$

In the case of linear constraints, choosing a $\tilde{v}$ according to (18) allows for a greatly reduced computational burden. However, when dealing with nonlinear constraints, as in (19e), one has to use bisection for solving (19) anyways, see [17]. In that
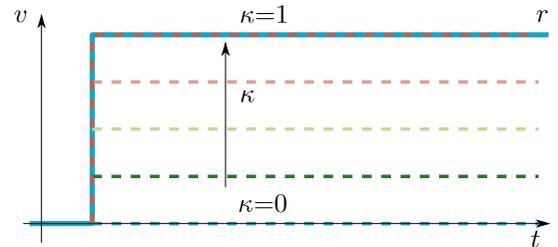
FIG. 9. Time evolution of the internal reference v for a classical RG with different values of κ (dashed lines) when following an external reference r (solid line).

case, the difference in computational burden between (17) and (19) becomes neglectable.

In order to compare the behavior of the classical RG to the proposed PT1-RG, another simulation with the same setup as described in Section VI-B was carried out with the classical RG, as shown in Fig. 10. As expected, all constraints were satisfied as well in this simulation. The rise time is also comparable to the one achieved with the PT1-RG. However, the current i_2, as seen in the lower plot of Fig. 10, shows an undesired oscillation. The requested $\frac{d}{dt}i_1$ is also greater in magnitude with the classical RG compared to the PT1-RG.
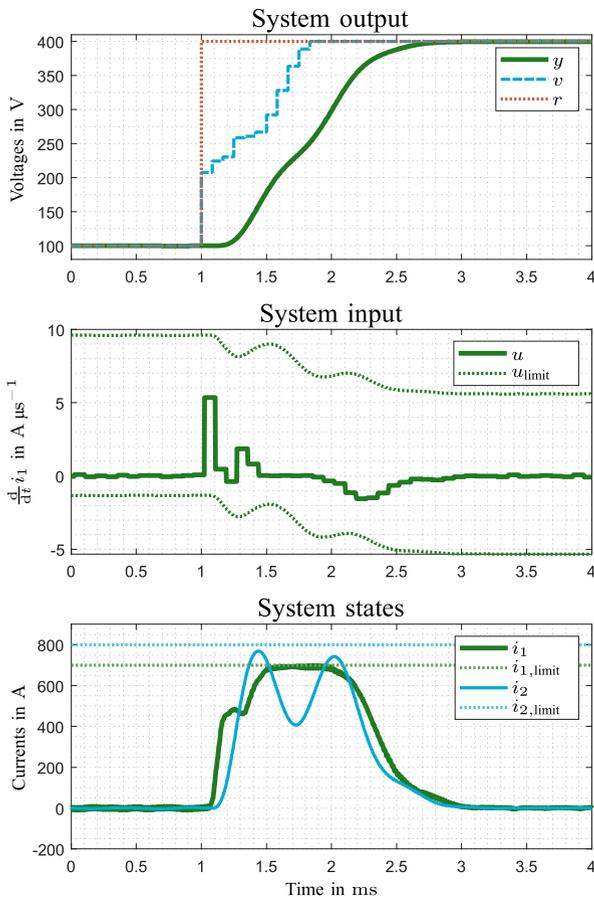
FIG. 10. Simulation results with a classical RG, performing a single setpoint change with $P = 0\,\text{kW}$.

Comparing the results in Fig. 7 and Fig. 10 it is evident that both the PT1-RG and the classical RG are able to satisfy the constraints. However, the controller effort was significantly reduced when using the PT1-RG scheme compared to the classical RG. Additionally, no oscillations on the current i_2 occurred when using the PT1-RG. This is partially owed to the fact that the internal reference v in Fig. 7 has a constant slope, while in Fig. 10, it is composed of multiple steps with different heights.

VIII. DISCUSSION

One might notice some similarities between the proposed RG and MPC schemes. In fact, an RG can also be designed within an MPC framework, as it can be viewed as an MPC controller with a quasi-infinite prediction horizon and a control horizon of 1, see [22]. While both the RG and the MPC require the solution of an optimization problem, the computational complexity for solving the MPC's problem is generally higher. This is the case as the MPC usually computes the input trajectory multiple timesteps into the future over the control horizon. However, only the first element of that planned input trajectory is actually applied. The remaining elements are discarded as the optimization problem is computed anew in a

receding horizon fashion. Consequently, one has to solve an optimization problem with multiple decision variables (one variable for each input at each timestep during the control horizon) for an MPC. On the other hand, with the RG, the optimization problem has only a single decision variable which can be efficiently solved via a bisection algorithm. The bisection algorithm also always provides a feasible (however not optimal) solution if the computation has to be abandoned early due to real-time constraints.

In order to accurately emulate the behavior of a battery, multiple battery-specific effects have to be considered. The most fundamental model for describing the dynamic response of a battery consists of a time-varying equivalent voltage source with an internal impedance, see [11]. This internal impedance results in a direct feedthrough behavior, causing an instantaneous response to sudden load changes. The requirement for a highly dynamical output voltage is rooted in the desire to accurately emulate this effect of the internal impedance of the battery. From a constraint-handling point of view, the other effects play only a minor role as they are slow in comparison and only result in gradual changes in the voltage setpoint. Therefore, the investigation in this publication focused only on step-like changes in the voltage setpoint without considering a specific battery model per se.

IX. CONCLUSION

This paper presents a PT1-RG for constraint handling in a battery emulator. The PT1-RG low-pass filterers the external reference value with a PT1-element, resulting in smoother constraints-aware transitions between two setpoints. Simulations show that the PT1-RG has the same constraint handling capabilities as a classical RG. The PT1-RG is able to consistently handle nonlinear state and input constraints over the entire operating range of the battery emulator. Furthermore, the required control effort is also reduced for the PT1-RG compared to the classical RG, while both have comparable rise times. Combined with a suitable controller, the PT1-RG allows for a safer operation of the battery emulator in the entire operating range as over-current situations are avoided.

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