Communication—The Role of the Metal-Semiconductor Junction in Pt-Assisted Photochemical Etching of Silicon Carbide

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Porous 4H-SiC layers were fabricated by photochemical etching of n-type 4H-SiC samples with varying resistivity. An etching solution of $Na_2S_2O_8$ and HF was used while Pt deposited at the 4H-SiC surface served as catalyst for the reduction of $Na_2S_2O_8$. The contact resistance at the Pt/4H-SiC junction was decreased by annealing and surface near phosphorous doping. This enabled the porosification of 4H-SiC with photochemical etching.

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Compared to porous silicon, porous silicon carbide has many outstanding properties such as an enhanced chemical inertness, high heat conductivity and a relatively large bandgap. Therefore it offers novel application scenarios as electrode material in super-capacitors,[1] membranes for biomedical devices[2] or in the manufacturing of high temperature gas sensors.[3]

Metal assisted photochemical etching (MAPCE) in HF/$S_2O_8^{2-}$ based solutions has up to now not been established as a reliable technique for the generation of porous silicon carbide (SiC). Recently, the formation of a roughened surface or a porous layer on 4H and 6H-SiC was achieved by MAPCE[4,5] where platinum (Pt) was deposited on the surface of SiC serving as catalyst during the porosification process. In the latter reports it is assumed that the oxidation reaction occurs at the Pt/etching solution interface where $S_2O_8^{2-}$ accepts electrons (Equation 1) while at the SiC/etching solution interface holes in the valence band are generated by irradiation with UV light. These holes are necessary for the oxidation of SiC (Equation 2). The formed SiO_2 is then dissolved by HF (Equation 3).

$$4\,S_2O_8^{2-} + 8e^- \rightarrow 8SO_4^{2-} \quad [1]$$

$$SiC + 4H_2O + 8h^+ \rightarrow SiO_2 + 8H^+ + CO_2 \quad [2]$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad [3]$$

Controlling the etching depth for 6H-SiC is still an unresolved issue, while the formation of a porous structure on 4H-SiC is limited to surface regions in the nanometer range.[6,7]

In this letter the formation of porous 4H-SiC by MAPCE is presented for samples having different bulk resistivity by decreasing the contact resistance at the Pt/4H-SiC junction.

Experimental

As substrates, n-type 4H-SiC wafers with low and high resistivity ($\rho = 0.02\ \Omega \cdot$ cm and $\rho = 0.106\ \Omega \cdot$ cm respectively) were purchased from CREE. Square samples of these substrates with an area of 1 cm^2 were used for experiments. For cleaning, all samples were consecutively soaked for 5 minutes in acetone, isopropanol and ethanol. Then a 300 nm thin Pt layer was sputter deposited on the samples with a LS730S Von Ardenne sputter machine, while a 0.7 × 0.7 cm^2 silicon piece in the center of the sample served as shadow mask. Prior to Pt deposition, the samples were cleaned in situ using an inverse sputter etching procedure with Argon plasma for 60 s at 1000 W. Finally the samples were placed in an etching solution containing 0.04 mol/L $Na_2S_2O_8$ and 1.31 mol/L HF for 2 hours under UV irradiation. As etching chamber a porous silicon etching cell from AMMT GmbH with a total volume of 1.5 L was used. Front side illumination was done with a 250 Watt ES280LL mercury arc lamp at full spectrum. The distance from the samples to the UV source was approximately 3 cm. In this configuration the effective volume of the etching solution was 150 mL.

For electrical characterization the Agilent B2911A Precision Source/Measure Unit was used. An array of circular Pt/TiN/Pt tri-layered pads was sputter deposited onto 1 cm^2 square samples. The diameter of the pads was 1 mm and the distance between them was 1 mm. The thickness of the Pt and TiN films at the top and bottom was 300 nm and 150 nm, respectively. Next, current voltage characteristics between adjacent pads were recorded. The pads used for the measurements consisted of Pt/TiN/Pt layers, because partial dewetting of pure Pt pads took place during annealing in argon atmosphere, which lead to unreproducible results in electrical characterization. Due to the high melting point and chemical inertness of TiN dewetting was prevented.

The porous layers were examined with a Hitachi SU8030 scanning electron microscope, with acceleration voltages ranging between 2 and 5 kV.

Results and Discussion

The first samples obtained from pure MAPCE experiments showed non-uniform etching characteristics. The samples having lower resistivity showed etching depths ranging from 0.5 µm to just surface roughening at the same sample. The samples having higher resistivity showed mostly surface roughening, locally parts with etching depths up to 1.3 µm could be observed, featuring a sharp border to the not porous regions. Both samples were etched in the regions not covered with Pt unlike metal assisted etching of Si where etching is mainly enhanced underneath a noble metal catalyst deposited at the surface.[8] For etching to occur, oxidation and reduction reactions are necessary. This means that electrons need to flow from the anode (i.e. 4H-SiC) to the cathode (i.e. Pt). Because the electrical current has to pass the Pt/4H-SiC interface, a low contact resistance should increase the etch rate and the uniformity of the porous layers. Annealing metal layers deposited on silicon carbide is a standard approach to form low ohmic contacts.[9,10]

The MAPCE experiment was carried out again with the difference that after Pt deposition the samples were annealed for 5 minutes in Argon atmosphere at 1100°C[11] with a prior temperature ramp starting at 800°C that lasted for 30 minutes. After 2 hours of MAPCE a porous layer with a more uniform depth of (1.11 ± 0.14) µm was observed at the samples with a resistivity of $\rho = 0.02\ \Omega \cdot$ cm. A cross-sectional view of the obtained porous structure is shown in Figure 1, demonstrating that a porous layer has formed. Figure 2a shows the current voltage characteristics of a sample having a resistivity of $\rho = 0.02\ \Omega \cdot$ cm before and after annealing. It demonstrates that the contact resistance at the Pt/4H-SiC junction had decreased due to the annealing. This has enhanced the formation of a porous layer during the MAPCE process.

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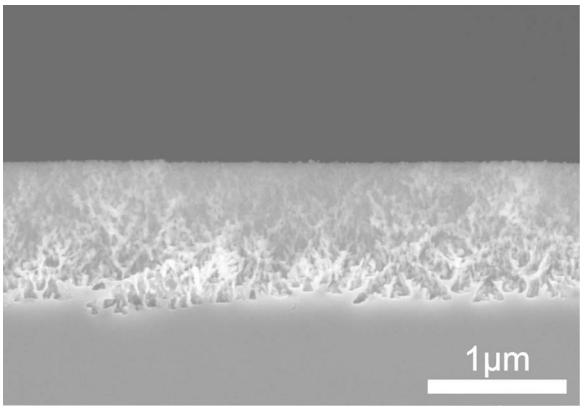

Figure 1. SEM image in cross-sectional view of an n-type 4H-SiC ($\rho = 0.02$ $\Omega \cdot$ cm) sample after MAPCE.

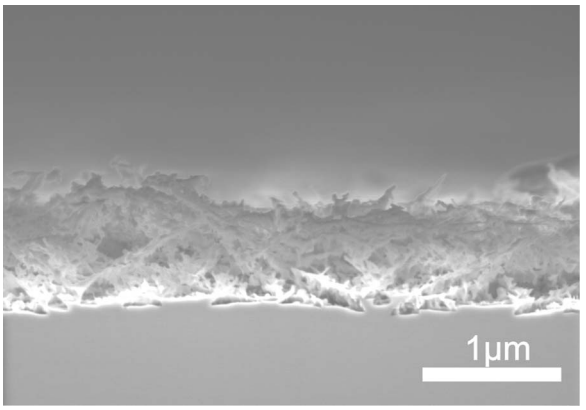

Figure 3. Cross-sectional view of an n-type 4H-SiC sample ($\rho = 0.106$ $\Omega \cdot$ cm) after MAPCE.

The same experiments were not successful using the samples with higher resistivity of $\rho = 0.106$ $\Omega \cdot$cm. This means that just surface roughening or occasional formation of a thin porous layer was observed. At higher resistivity and thus lower dopant concentration the contact resistance is increased at the metal/semiconductor junction. This explains why for the samples with higher resistivity no reproducible porous layer formation was observed even when the samples were annealed. To decrease the contact resistance further a sample with $\rho = 0.106$ $\Omega \cdot$cm was doped with phosphorous near the surface according to a method developed by Mendis et al.[12] Therefore, 0.1 mL of a solution consisting of 50 mL absolute ethanol and 20 mL phosphoric acid (85%) were placed on the sample surface. Next, the sample was annealed in air at 650°C for 30 minutes and in a second step in air at 1100°C for 2 hours. Finally, the sample was cleaned in buffered oxide etch to remove oxidation products, Pt was sputter deposited and annealed like in the previous experiments. These samples showed the formation of a porous layer with uniform depth of (0.78 ± 0.07) µm homogeneously across the sample after 2 hours of MAPCE. A cross-sectional micrograph of the obtained porous layer is shown in Figure 3. Due to the increased dopant concentration near the surface the resistance at the Pt/4H-SiC contact decreased substantially, thus initiating the MAPCE process. This is verified by current voltage measurements of differently processed samples (see Figure 2b), demonstrating the expected impact of annealing and additional doping on contact resistance.

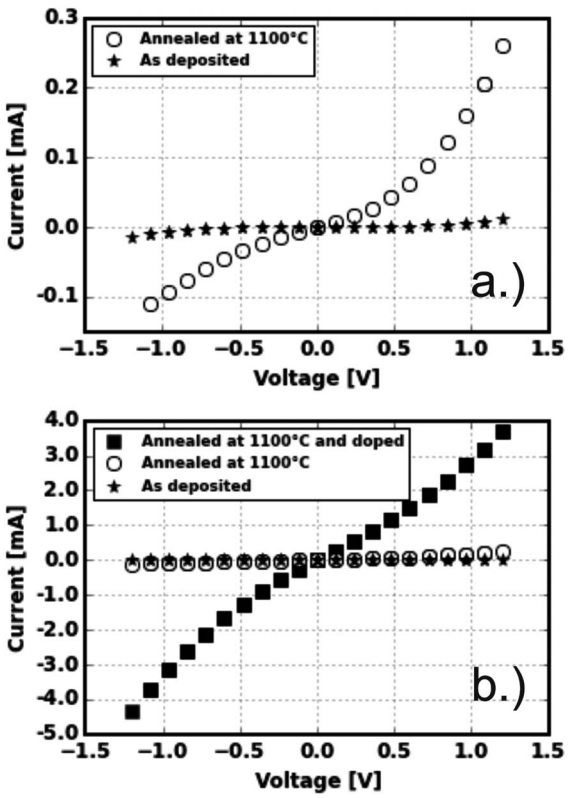

Figure 2. Current voltage characteristics recorded between two adjacent pads of Pt/TiN/Pt stack layers on n-type 4H-SiC before and after annealing. a) Sample with a resistivity of $\rho = 0.02$ $\Omega \cdot$cm. b) Sample with a resistivity of $\rho = 0.106$ $\Omega \cdot$cm including an additional measurement showing the current voltage characteristics after surface near phosphorous doping.

The observed etching depth for the surface near doped sample with $\rho = 0.106$ $\Omega \cdot$cm is large compared to the reported diffusion depth of phosphorous atoms in SiC (about 0.1 µm) during annealing.[13] This means that also not additionally doped 4H-SiC was etched. These observations show that there are three interfaces of interest in Pt assisted photochemical etching of 4H-SiC which determine the performance of the etching process. One is the Pt/4H-SiC junction for which a low contact resistance is needed. Next, at the Pt/etching solution interface persulfate is reduced. Lastly, at the 4H-SiC/etching solution interface holes in the valence band of 4H-SiC are generated by UV light which are needed to increase the etching rate.

Summary

In this letter the metal assisted photochemical etching (MAPCE) of n-type 4H-SiC in a solution of HF/$Na_2S_2O_8$ with Pt as catalytic metal was investigated. It was shown that the Pt/4H-SiC interface plays a crucial role in this process. Decreasing the contact resistance at the Pt/4H-SiC junction by annealing the samples was sufficient to allow photochemical etching of specimens with low resistivity, while additional surface near doping with phosphorous was necessary for samples having high resistivity to initiate the porosification process. Furthermore, UV light illumination is necessary to generate electron-hole pairs in the space charge layer of the etching solution/4H-SiC interface.

There is hardly any literature available regarding MAPCE of 4H-SiC. The presented findings allow the further investigation of 4H-SiC MAPCE with respect to experimental parameters such as the type of the catalytic metal, the spectral distribution properties of the light source or the composition of the etching solution.

Acknowledgments

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