DISSERTATION

Monolithic Microwave Integrated Circuits in SiGe:C Bipolar Technology

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Zusammenfassung

Die vorliegende Arbeit befasst sich mit der Entwicklung und Optimierung von monolithisch integrierten Schaltungen in Silizium-Germanium (SiGe) Bipolartechnologie für Anwendungen im Mikrowellenbereich. Kostengünstige Hochfrequenzschaltungen ermöglichen ein rasantes Wachstum des Marktes für Kommunikationsdienste. Insbesondere mobile Anwendungen wie zum Beispiel WLAN (wireless local area network), GPS (global positioning system) und die Mobiltelefonie (GSM, UMTS), aber auch drahtgebundene Breitbandsysteme erfuhren ernorme Wachstumsraten in den letzten Jahren. Auch Anwendungen im Mikrowellenbereich wie zum Beispiel Abstandsradar für die Automobilindustrie aber auch Breitbandsysteme für die schnelle Datenübertragung könnten zum Massenprodukt werden, falls die Systemkosten wesentlich gesenkt werden. Dies könnte durch eine integrierte Realisierung in einer kostengünstigen silizium-basierten Halbleitertechnologie ermöglicht werden. SiGe bietet neben der Eignung für hohe Frequenzen auch den Vorteil einer hohen Integrationsfähigkeit, die wesentlich die Gesamtkosten eines Systems bestimmt.

Am Beginn der vorliegenden Arbeit wird ein Überblick über die verwendete SiGe:C Bipolartechnologie gegeben. Anschließend wird anhand ausgewählter Beispiele die Realisierung monolithisch integrierter Analogschaltungen für den Mikrowellenbereich gezeigt.

Als erstes Beispiel wird die Entwicklung und die Optimierung eines Breitbandverstärkers zur Verstärkung von Datensignalen sehr hoher Bitrate, aber auch sehr hochfrequenter Sinussignale, demonstriert. Neben einer hohen 3-dB Bandbreite zählen eine flache Übertragungsfunktion sowie ein hoher Ausgangshub zu den wesentlichen Entwurfszielen. Durch sorgfältige Optimierung der Schaltung wird eine Übertragung von Datensignalen mit einer Datenrate von 100 Gbit/s bei gleichzeitig hohem Ausgangshub erreicht. Diese Ergebnisse, welche in [Perndl 04b] publiziert wurden, zeigen eine höhere Datenrate als alle bisher veröffentlichten Analogschaltungen, nicht nur in silizium-basierten, sondern auch in GaAs- und InP-Technologien.

Als zweites Beispiel einer monolithisch integrierten Mikrowellenschaltung dient ein Abwärtsmischer für den Frequenzbereich von 76 GHz bis 81 GHz. Dieses Frequenzband ist für Abstandssensoren in der Automobilindustrie vorgesehen. Bei dieser Schaltung handelt es sich um den ersten Abwärtsmischer für diesen Frequenzbereich, der in silizium-basierter Technologie gefertigt wurde. Eine Zusammenfassung dieser Ergebnisse ist in [Perndl 04a] veröffentlicht.

Schließlich wird ein monolithisch integrierter spannungsgesteuerter Oszillator beschrieben. Das wesentliche Entwicklungsziel dieser Schaltung ist eine möglichst hohe Ausgangsfrequenz. Unter Anwendung innovativer Schaltungskonzepte, wie zum Beispiel eines integrierten Lambda-Viertel-Transformators am Ausgang der Schaltung, gelingt es, eine Ausgangsfrequenz von 98 GHz zu erreichen. Die Ergebnisse dieser Schaltung sind in [Perndl 03] und [Perndl 04c] veröffentlicht.

Abstract

This thesis deals with design and optimization of monolithically integrated circuits for applications at microwave frequencies fabricated in a state-of-the-art low-cost silicon germanium (SiGe) bipolar technology. The rapid growth of the communication market is enabled due to low-cost high-frequency solutions. Especially wireless applications like wireless local area networks (WLAN), global positioning systems (GPS) and mobile telephony (GSM and UMTS) as well as wireline broadband systems came up over the past years. Additionally, applications at microwave frequencies like distance sensors for automotive and industrial systems as well as high-speed data communication could become a new mass market, if system costs can be reduced significantly. For monolithically integrated realization of such systems, silicon germanium bipolar technologies seem to be a promising candidate. Due to constant progress in technology development as well as accurate optimization during the circuit design process, monolithic integrated circuits in the microwave frequency range fabricated in low-cost silicon-based technologies become feasible.

At the beginning of this thesis an overview of the SiGe:C bipolar technology, in which the chips of this work have been fabricated, is presented. Subsequently, monolithic integration of analog building blocks is demonstrated on the basis of three representative circuits for different microwave applications.

The first circuit presented in this work is a broadband amplifier. The amplifier is intended for multiple applications like a preamplifier of high data rate signals, an amplifier for high-frequency single-tone signals and a linear amplifier in conventional high-frequency systems. Due to contradicting requirements of the different applications, tradeoffs between circuit parameters are necessary. A flat frequency response and a high 3-dB bandwidth are the main design targets. By careful optimization of the circuit, outstanding measurement results up to 100 Gbit/s are achieved. These results, which have been published in [Perndl 04b], show the highest bit rate for analog high-frequency circuits in silicon-based as well as GaAs and InP technologies.

The second example of a fully monolithically integrated microwave circuit is a down-conversion mixer in the frequency range from 76 GHz to 81 GHz. This frequency band is intended for automotive distance sensors. With this design, a monolithically integrated active down-conversion mixer for microwave frequencies around 77 GHz is demonstrated for the first time in silicon-based technologies. A summary of these results is published in [Perndl 04a].

Finally, a voltage-controlled oscillator is shown. The main design target is to reach an output frequency as high as possible at reasonable values of phase noise and output power. By application of innovative circuit concepts like a quarter-wave transformer at the output of the circuit an operation frequency up to 98 GHz is reached. These results are published in [Perndl 03] and [Perndl 04c].

Contents

Chapter 1

Introduction

The rapid growth of wireless communication systems such as wireless telephony, global positioning systems (GPS) and wireless local area networks (WLAN) as well as wireline communication systems such as broadband data services is enabled by low-cost and high-performance semiconductor solutions. This evolution tends continuously towards higher operation frequencies, higher integration levels and lower power consumption.

The choice of an appropriate technology for a specific application is of particular importance. Due to the fast progress of technology development this choice is subject to fast changes. Over the past years especially silicon-based technologies made outstanding progress. The introduction of the double-polysilicon self-aligned transistor configuration as well as improvements in the doping profile enabled a strong increase in the transistor's speed. Also the analog properties of the transistors have been improved by enhancements of technological processes. The target of system development is to implement both analog and digital building blocks on a single chip in order to reduce system costs. Due to the different requirements of analog and digital circuits it is a great challenge to monolithically integrate both functions into one semiconductor. State-of-the-art silicon germanium bipolar technologies seem to be promising candidates for such applications due to the capability of high integration levels as well as the constantly increasing speed.

Applications in the microwave frequency range like WLAN at 60 GHz, optical communication at 80 Gbit/s and radar systems at 77 GHz can be realized up to now only in III-V semiconductor technologies. Recent advances in SiGe bipolar technology have stimulated research activities to investigate the realizability of applications at microwave frequencies in silicon-based technologies.

1.1 Objective of the Work

The aim of this work is to demonstrate monolithic integration of analog building blocks for applications at microwave frequencies in a state-of-the-art low-cost SiGe bipolar technology. This will be demonstrated on the basis of a broadband amplifier for high data rate communication systems as well as a down-conversion mixer and a voltage controlled oscillator for distance sensors in automotive and industrial applications. Due to the very high operation frequencies, wave propagation on chip becomes a substantial concern even though chip dimensions are very small. At a frequency of 77 GHz, the wavelength λ in silicon dioxide is only 2 mm, so $\lambda/10$ is smaller than typical chip dimensions. Due to this property, new possibilities in circuit design arise. New circuit architectures become possible and open a wide field of research.

At first, for each design specifications and targets are defined as well as an overview of state-of-the-art circuits is made. Then, circuit architecture and technology have to be selected. The circuit architecture mainly depends on the technology in which the chip is fabricated. Both, active components (transistors) as well as passive components like resistors, capacitors, varactors and the metal layer stack decide whether a circuit concept is feasible in a certain technology or not. If circuit architecture and technology are fixed, the main task is to optimize the various functional blocks of the circuit. At this time, it is essential to make use of the specialities of the technology as well as to compensate for deficiencies of the specific technology by innovative circuit design. Next, the components of the circuit should be optimized regarding an optimum compromise between contradicting circuit characteristics.

Usually this design process consists of several iterations since it is possible that a chosen circuit architecture turns out to be not optimal after intensive investigation. Consequently, the optimization of a circuit requires experience for selecting the architecture, innovation in finding new solutions, creativity for implementation of the various functional blocks, as well as technical know-how about individual components of the technology.

1.2 Thesis Outline

After the introduction, Chapter 2 provides basics of the SiGe:C technology, which is chosen for the fabrication of the chips of this work. Because this technology is still in development, the status quo of September 2004 is provided. First the transistor configuration, the process concept and basics of the fabrication process are explained. Simulation models for large and small signal simulation are provided as well as transistor effects are discussed. Properties of different transistor geometries are pointed out. Transistor results as well as characteristics of passive components and the metal layer stack are shown.

In Chapter 3 design and optimization of a broadband amplifier in SiGe:C bipolar technology are presented. At first, an optical communication system which utilizes the broadband amplifier is introduced and basics about broadband amplifiers are explained. The circuit design process of the amplifier is based on the analysis of a differential amplifier with emitter followers at its input. Then the circuit is adapted to the particular specification. S-parameter measurements, large signal measurements as well as excitation with high data rate signals are presented.

In Chapter 4 the design of a fully integrated active mixer for microwave applications at 76 GHz to 81 GHz is presented. This mixer is intended for distance sensors in automotive and industrial systems based on the frequency modulation continuous wave (FMCW) radar principle. At the beginning of the chapter the FMCW-principle is described as well as an overview about mixer properties is given. Then circuit design of the mixer is presented. The mixer core is based on the Gilbert cell. An LC balun and an LO buffer are used in order to provide differential signals to the mixer core. Finally, the layout and measurement results are presented.

In Chapter 5 a voltage controlled oscillator (VCO) with an output frequency up to 98 GHz is presented. This oscillator is based on the Colpitts oscillator. At the output, the circuit includes a novel quarter-wave transformer for impedance transformation which increases the maximum oscillation frequency. Design and optimization of the oscillator core and the resonator are presented. The measurement results as well as the influence of the measurement system on this particular oscillator are discussed.

Chapter 6 summarizes the results of the work and gives an outlook on future developments in monolithic microwave integrated circuit design.

Chapter 2

Silicon Germanium Bipolar Technology

The aim of this chapter is to present the silicon germanium (SiGe) bipolar technology in which the chips of this work are fabricated. This technology is still in development, so the status quo of September 2004 is described. The chips of this work are fabricated in wafer runs at different stages of the development. The substantial differences are mentioned in the respective chapter.

The first section of this chapter describes the process concept of the technology. Comments on the fabrication process and transistor results are given. Then transistor models for large and small signal simulation are introduced. These models are the starting point for circuit design. Additionally important transistor effects are discussed which must be considered during the design process. Finally passive components and the metallization of the technology is presented.

2.1 Double-polysilicon Self-aligned Transistor Configuration

Figure 2.1 shows the schematic cross section of an npn transistor of Infineon's preproduction process B10HF. The active area of this transistor, which is located beneath the emitter contact, is only small compared to the whole transistor. But the dimension of the external inactive transistor is restricted due to design-rules of the technology, e.g. there are minimum width and minimum spacing of the first metal layer which specify the minimum distance between base, emitter, and collector contact. Optimization of the transistor performance includes both to speed up the intrinsic transistor (active area of the transistor) and to reduce parasitics like capacitances and resistances of the external inactive transistor.

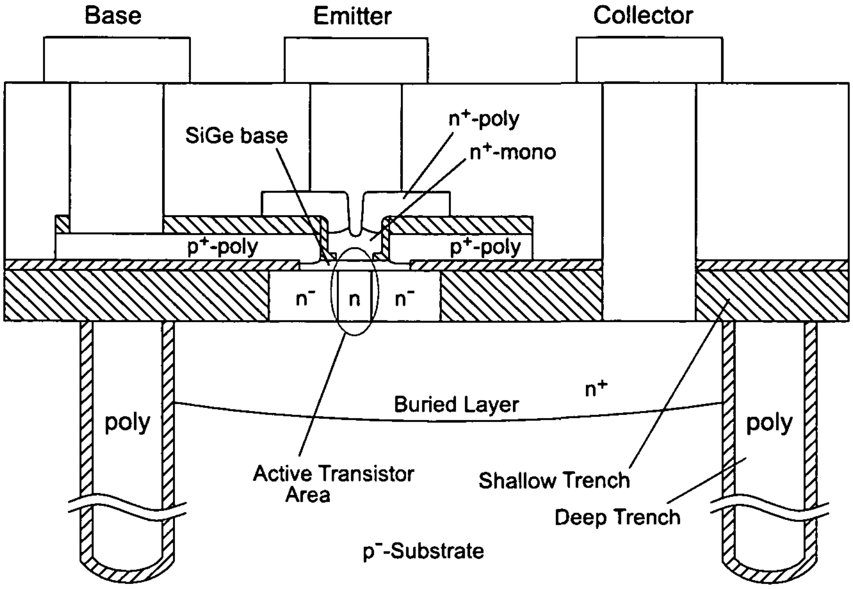


Figure 2.1: Schematic cross section of an npn transistor

Infineon's B10HF silicon germanium bipolar technology is based on a double-polysilicon self-aligned transistor configuration with a selective epitaxial grown SiGe base layer. "Double-polysilicon" means that both, emitter and base contact are realized with polysilicon. This configuration exhibits low parasitic capacitances and a low extrinsic base resistance. The term "self-aligned" refers to the emitter-base isolation which is realized by thin dielectric layers. These so-called spacers are manufactured using anisotropic plasma etching and allow the construction of structures smaller than the lithographic limits.

A double-polysilicon self-aligned transistor with selectively epitaxially grown base was first realized without germanium (Ge) in [Meister 92]. Important further developments of the extrinsic transistor are a silicided polysilicon layer for contacting the base of the active transistor [Böck 98]. As a result of this silicided layer, the external base resistance is reduced by about one decade. Another feature of the technology is a mono-crystalline emitter contact [Meister 03] which reduces the emitter resistance considerably, as compared to conventional polysilicon emitters. Further, the collector-substrate capacitance is reduced by more than 40 % by introducing deep trench (DT) and shallow trench isolation (STI) [Schwerd 03, Böck 04].

The integration of Ge into the base of the transistor enables bandgap engineering and the fabrication of heterojunction bipolar transistors (HBTs) in silicon-based materials [Meister 95]. In the SiGe HBT, germanium is selectively introduced into the base region of the transistor. The smaller base bandgap of SiGe compared to Si enhances electron injection, producing a higher current gain for the same base doping level compared to a Si device. Thus, the base can be doped more heavily in the SiGe HBT in order to lower the total base resistance. At the same time, the Ge content is graded across the base in order to achieve an accelerating drift field for the electrons to increase the cutoff frequency. A doping profile of the fabricated transistors is shown in Fig. 2.2. The n-type emitter is typically doped with arsenide (As), the doping material for the n-type collector is typically phosphor (P), and as acceptor material for the p-type base usually boron (B) is used. At the emitter side the base is lowly doped in order to obtain a small emitter-base capacitance. For realizing high cutoff frequency the thickness of the boron spike must be kept as thin as possible. The incorporation of carbon into the highly boron-doped SiGe base prevents the broadening of the base profile by subsequent processing steps [Böck 01].

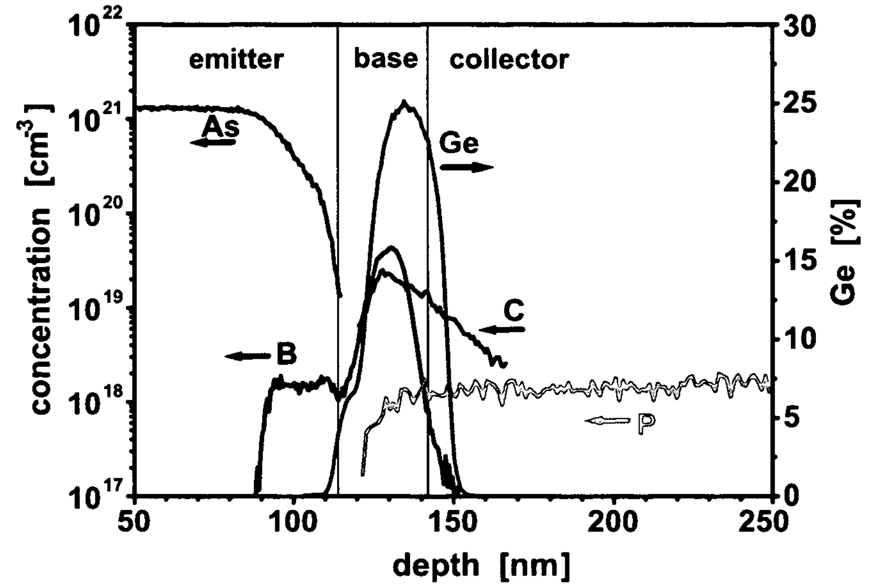


Figure 2.2: Final doping profile of the transistors

Figure 2.3 shows a TEM cross section of a whole npn transistor of Infineon's preproduction process B10HF including the dimensions. In Fig. 2.4 a TEM cross section of the emitter-base complex of a transistor is shown. Mono-crystalline n-type silicon of the emitter and the collector is depicted as light, uniformly colored areas, whereas polysilicon looks granular. The germanium fraction of the base results in a dark bar indicated as "SiGe:C-base".

2.2 Simulation Models

2.2.1 Large Signal Model

The design of radio-frequency integrated circuits requires accurate and compact models of the bipolar transistors. A large variety of bipolar transistor models has been developed so far. The first compact model for bipolar transistors originates from the early 1950s by Ebers and Moll [Ebers 54]. This model describes the DC behavior of the transistor using

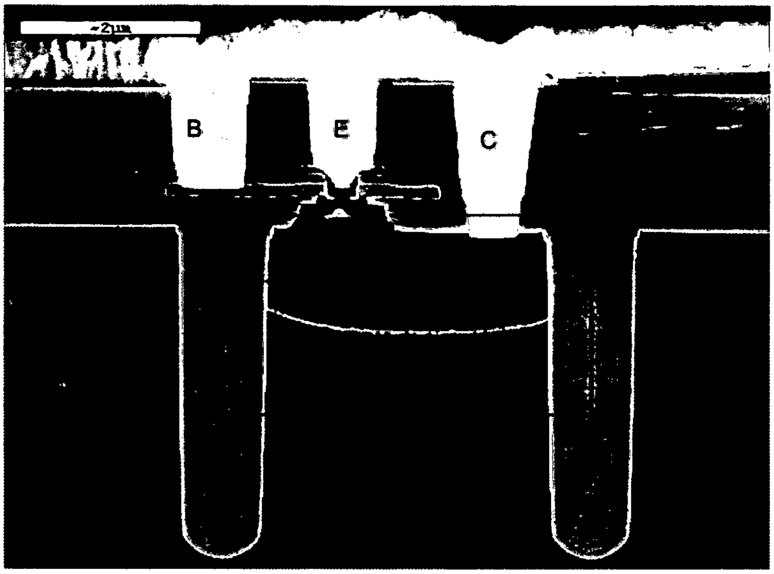


Figure 2.3: TEM of the transistor

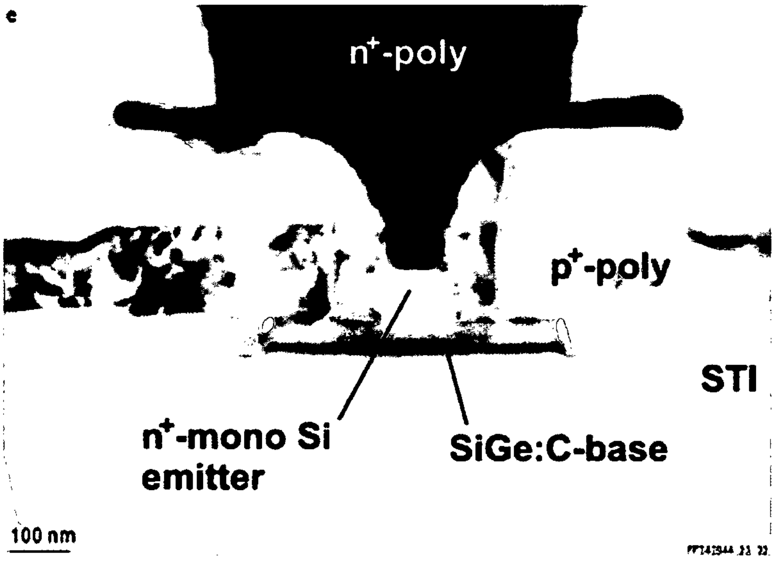


Figure 2.4: TEM of the emitter base complex

four parameters: the ideal forward and reverse common-base current gain (α_F and α_R) and the saturation current of the base-emitter and the base-collector diode (I_{BES} and I_{BCS}). The Ebers-Moll model describes the fundamental DC behavior of the transistors, however many effects like the Early and Kirk effect as well as conductivity modulation are not covered. A compact model that is more appropriate for the descripton of the bipolar transistor is the Gummel-Poon model [Gummel 70]. This model is based on the integral charge control concept by introducing the normalized majority base charge q_b. So, many of the effects not contained in the basic Ebers-Moll model are incorporated in an integral, physical way. The Gummel-Poon model has been implemented in a slightly modified version into the circuit simulation tool SPICE [Nagel 75] (SPICE-Gummel-Poon model) and so it has become a standard for modeling of bipolar transistors. A comprehensive presentation of modeling high-frequency bipolar transistors can be found in [Reisch 03].

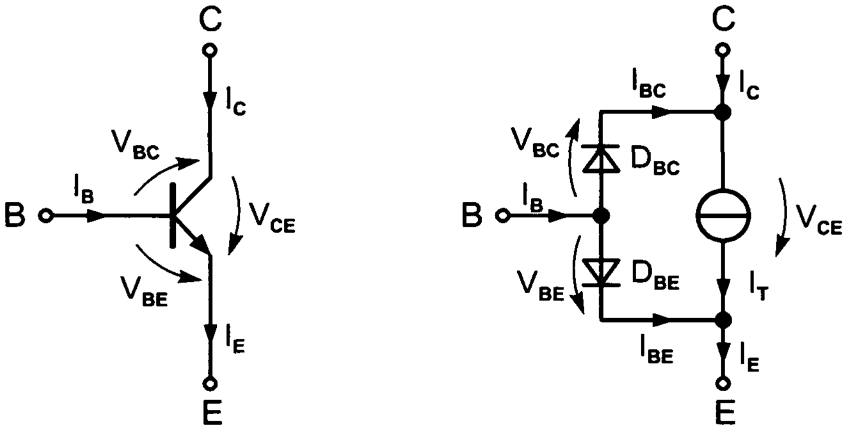


Figure 2.5: A simple equivalent circuit for modeling bipolar transistors [Reisch 03]

The equivalent circuit to describe the transistor characteristics which is shown in Fig. 2.5 is based on the Gummel-Poon model. It employs two diodes D_{BC} and D_{BE} representing the base-emitter (BE) and the base-collector (BC) junctions, together with a voltage-controlled current source, which describes the coupling of the two pn-junctions. In forward operation ($V_{BE} \gg V_T$ and $V_{BC} < 0$) the reverse biased BC diode can be neglected. Then I_{BC}=0 and the collector current I_C equals the transfer current I_T, I_C=I_T. Neglecting series resistances the following equations characterize the large signal behavior of the transistor [Reisch 03]:

$$I_C = I_S \left(1 + \frac{V_{CE}}{V_{AF}}\right) exp\left(\frac{V_{BE}}{V_T}\right), \tag{2.1}$$

$$I_B = \frac{I_S}{\beta_F} exp\left(\frac{V_{BE}}{V_T}\right), \tag{2.2}$$

$$\alpha_F = \frac{\beta_F}{1+\beta_F} , \tag{2.3}$$

where I_S is the transfer saturation current, V_T denotes the thermal voltage, and V_{AF} is the Early voltage. β_F is the common-emitter forward current gain which relates to the already mentioned common-base forward current gain α_F via (2.3).

The SPICE-Gummel-Poon model also incorporates bias-dependent resistances for base and collector contact, an emitter resistance as well as diffusion and depletion capacitances. Further effects like carrier recombination in the space charge region and collector substrate coupling are considered, see [Reisch 03].

In practice, additionally to the SPICE-Gummel-Poon model parasitic elements are modeled by using a sub-circuit as shown in Fig. 2.5. In the external transistor circuit of Fig. 2.6, C_E and C_C characterize oxide capacitances between external contacts. R_B, R_E, and R_C model the external resistances of base, emitter, and collector contact.

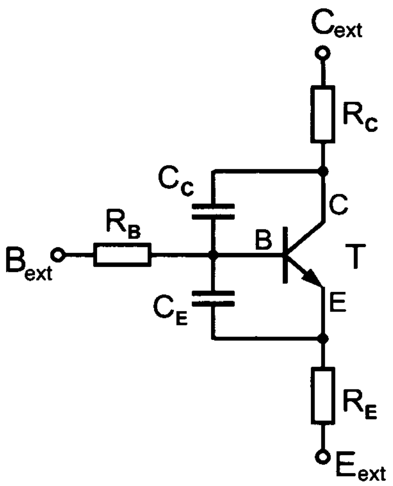


Figure 2.6: External model for the simulation of transistors. T represents an internal transistor model.

2.2.2 Small Signal Model

If the signal levels of analog circuits are small enough compared to bias currents and voltages, linearized small signal models can be used for the analysis of the circuits. In forward operation ($V_{BC} < 0$ and $V_{BE} \gg V_T$) the small signal equivalent circuit shown in Fig. 2.7 can be derived from the large signal model of Fig. 2.5.

The input conductance g_π, the transconductance g_m, and the output conductance g_o can be determined as partial derivatives of the current-voltage characteristics from (2.1) to (2.3) [Reisch 03]:

$$g_\pi = \left(\frac{\partial I_B}{\partial V_{BE}}\right)_{V_{CE}} = \frac{I_B}{V_T}\,, \tag{2.4}$$

$$g_m = \left(\frac{\partial I_C}{\partial V_{BE}}\right)_{V_{CE}} = \frac{I_C}{V_T}\,, \tag{2.5}$$

$$g_o = \left(\frac{\partial I_C}{\partial V_{CE}}\right)_{V_{BE}} = \frac{I_C}{V_{CE} + V_{AF}}\,. \tag{2.6}$$

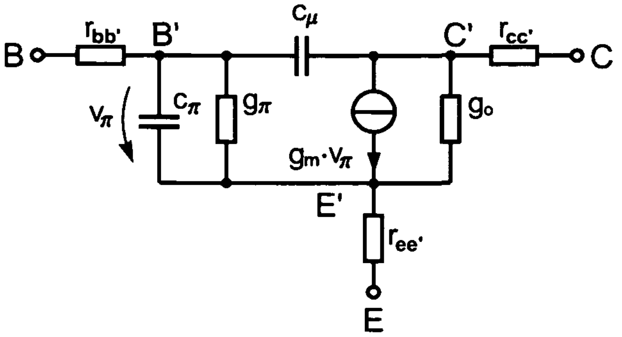


Figure 2.7: High frequency small signal equivalent circuit with series resistances based on the Giacoletto model; $r_{bb'}$, $r_{ee'}$, and $r_{cc'}$ represent linearized resistances of the potentially bias dependent contact resistances $R_{bb'}$, $R_{ee'}$, and $R_{cc'}$.

Often the input resistance $r_\pi = 1/g_\pi$ and the output resistance $r_o = 1/g_o$ are used. The short-circuit, small signal current gain β_0 depends on the DC operating point and can be calculated as:

$$\beta_0 = \left(\frac{\partial I_C}{\partial I_B}\right)_{V_{CE}} . \tag{2.7}$$

The high-frequency behavior of the transistor is modeled by two capacitances c_π and c_μ, see Fig. 2.7. Each capacitance consists of a diffusion and a depletion part. In forward operation, the diffusion charge of the BC diode can be neglected, resulting in:

$$c_\mu = c_{jc} \text{ and } c_\pi = c_{je} + \tau_F g_m \tag{2.8}$$

where c_{je} and c_{jc} denote the depletion capacitances of the BE and BC diodes, and τ_F is the forward transit time. $\tau_F\, g_m$ denotes the diffusion capacitance of the BE diode. The frequency range of a transistor is usually specified by the frequency where the magnitude of the current gain $\beta(f)$ falls to unity

$$\beta(f) = \frac{\beta_0}{1 + j\ f/f_\beta} \ \rightarrow\ f_T = \beta_0\, f_\beta \tag{2.9}$$

where f_β denotes the 3-dB cutoff frequency of β, and f_T denotes the cutoff frequency of the transistor. f_T depends on the bias conditions: for a low collector current I_C, f_T can be calculated as [Reisch 03]:

$$f_T \approx \frac{g_m}{2\pi(c_{je} + c_{jc})} \tag{2.10}$$

which causes f_T to increase with I_C. For large values of I_C, f_T results in [Reisch 03]:

$$f_T \approx \frac{1}{2\pi[\tau_F + (r_{ee'} + r_{cc'})c_{jc}]} \tag{2.11}$$

where τ_F denotes the forward transit time. At high collector currents, τ_F increases with I_C which causes f_T to decrease with increasing I_C. So there is an optimum collector current which leads to a maximum cutoff frequency, see Fig. 2.9.

Another important measure of transistor performance is the maximum oscillation frequency f_{max}. It is defined as the frequency where the unilateral power gain [Vendelin 82] of the transistor becomes unity. It can be calculated [Reisch 03]:

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi(r_{bb'} + r_{ee'} + 1/g_m)c_{jc}}} \,. \tag{2.12}$$

2.2.3 Modeling of Parasitic Resistances

The base resistance $R_{BB'}$ consists of an internal base resistance (within the active area) and an external contact resistance (poly-Si contact region). In order to yield a low base transit time, a very thin base is required. This affects the internal base resistance which depends on the base width, the width of the emitter window, and the doping density in the SiGe:C base. Further it depends on the bias condition of the transistor. The internal base resistance is modeled as [Reisch 03]:

$$R_{BB'} = R_{BM} + \frac{R_B - R_{BM}}{q_B} \tag{2.13}$$

where R_B and R_{BM} denote the maximum and the minimum base resistance, respectively, and q_B denotes the normalized majority base charge. Due to conductivity modulation and emitter current crowding (see Section 2.3), the internal base resistance decreases at high base and collector currents. The external part of the base resistance consists of the contact resistance and the resistance of the external base region. This part is modeled as an ohmic resistance.

The emitter resistance $R_{EE'}$ acts as emitter degeneration and so it reduces the transconductance g_m of the transistor. As a result of the high doping level in the emitter, the resistance of the mono-crystalline emitter is small compared to the poly-contact resistance. Further, the contact resistances between metal and poly-Si as well as between poly-Si and mono-Si must be considered [Gabl 99]. The emitter resistance $R_{EE'}$ is described as an ohmic resistance.

The collector resistance $R_{CC'}$ consists of an internal and an external resistance, too. The external contact resistance is kept low due to a highly doped buried layer. The internal portion of the collector resistance can not be reduced without increasing the BC capacitance and reducing the BC breakdown voltage. $R_{CC'}$ influences the saturation current of the transistor, therefore it is of particular interest in circuits which are subject to saturation and quasi-saturation (see Section 2.3). In our models, $R_{CC'}$ is also described as ohmic resistance.

2.2.4 Modeling of Parasitic Capacitances

Parasitic capacitances of the transistors comprise both pn-junction capacitances (depletion capacitances) and capacitances with silicon oxide as dielectric material.

The depletion capacitance of a pn-junction represents the charge stored by the junction under specified bias conditions. Depending on the applied forward voltage V, this capacitance can be calculated as [Reisch 03]:

$$c_j(V) = \frac{C_{J0}}{(1 - V/V_J)^M} \tag{2.14}$$

where V_J is the so-called built-in voltage and C_{J0} is the depletion capacitance at V=0 V. The exponent M depends on the doping profile of the pn-junction. For abrupt pn-junctions M equals 1/2 and for linear graded pn-junctions it is 1/3. Equation (2.14) is not valid for forward bias voltages greater than $V_J/2$. If V=V_J, (2.14) predicts that $c_J(V)$ approaches infinity. As an approximation, the simulation program SPICE calculates $c_J(V)$ for $V > V_J/2$ by a linear extrapolation of (2.14).

The contact regions of the transistor are separated by silicon oxide. These regions also represent parasitic capacitances, which are modeled by splitting the capacitances into area and perimeter specific parameters.

2.3 Transistor Effects

2.3.1 The Early Effect

The Early effect [Early 52] represents changes of the base-emitter and the base-collector junctions for different bias conditions. Especially an increase in the collector-base reverse bias voltage results in a wider BC depletion region and hence the width of the neutral base is reduced. This causes a steeper gradient of injected minority carriers. Consequently, an increase in collector-base reverse bias voltage leads to an increase in collector current. So the Early effect is observed as a non-zero output conductance. It is modeled by the Early voltage V_{AF}, see (2.1), which is the extrapolated intercept of the collector current

I_C data with the collector-emitter voltage axis. The Early effect is also called "base width modulation".

2.3.2 The Kirk Effect

The Kirk effect [Kirk 62] originates from the finite drift velocity of the electrons in the base-collector depletion region. At high collector currents, an additional negative space charge is present in the depletion region, which partly compensates the positive ionized donors in the n-type side of the depletion region. If the electron density is higher than the doping density, majority carriers from the base can move into the collector region, because there is no negative space charge that forces holes to stay in the base region. The dipole formed by the positively and negatively charged ionized donors and acceptors is pushed into the collector and replaced by positively charged ionized donors and a negatively charged electron accumulation layer. So the effective base width as well as the base transit time are increased substantially, which causes current gain and cutoff frequency to decrease. Increasing the collector doping can shift the Kirk effect towards higher currents. However, this also increases the base-collector capacitance and decreases the collector-base breakdown voltage. The Kirk effect is also referred to as "base-pushout".

2.3.3 Quasi Saturation

Quasi-saturation [Kull 85] is an effect that occurs at high currents due to the collector resistance of the bipolar transistor. In forward operation, the BC diode is reverse biased ($V_{BC} < 0\,\mathrm{V}$). If the voltage drop over the collector resistance is large enough, the BC diode can be forward biased even though it is externally reverse biased. Then holes are injected into the collector region, the base current increases, and β decreases. Due to the increasing base-collector capacitance, the transit frequency f_T decreases when quasi-saturation sets in.

2.3.4 Emitter Current Crowding

Emitter current crowding occurs at high collector currents. The also high DC base current produces a lateral voltage drop in the base, so the BE diode is more forward biased at the edges of the emitter. This leads to a higher collector current at the edges of the emitter in comparison to the middle of the active area. Therefore the effective distance from the base contact to the active area is reduced and consequently the base resistance is reduced.

2.3.5 Base Conductivity Modulation

At high transfer currents, the concentration of injected electrons into the base is comparable with the doping level in the base. This causes an increase in the hole diffusion charge in the base because the majority carriers in the base, the holes, neutralize the injected charge. This process is called dielectric relaxation. Due to the higher hole density, the conductivity of the base region is increased which reduces the lateral voltage drop. So, the base conductivity modulation effect and the emitter current crowding effect counteract each other, but both effects reduce R_B.

2.4 Electrical Characteristics

Figure 2.8 shows the common emitter DC output characteristics of transistors with an emitter area of $0.14 \times 2.6\,\mu\text{m}^2$. The collector-emitter breakdown voltage BV_{CE0}, which is measured with open base, is 1.7 V and the open-emitter collector-base breakdown voltage BV_{CB0} is 5.8 V. The maximum sustainable operating voltage of a SiGe HBT generally lies between BV_{CE0} (worst case) and BV_{CB0} (best case).

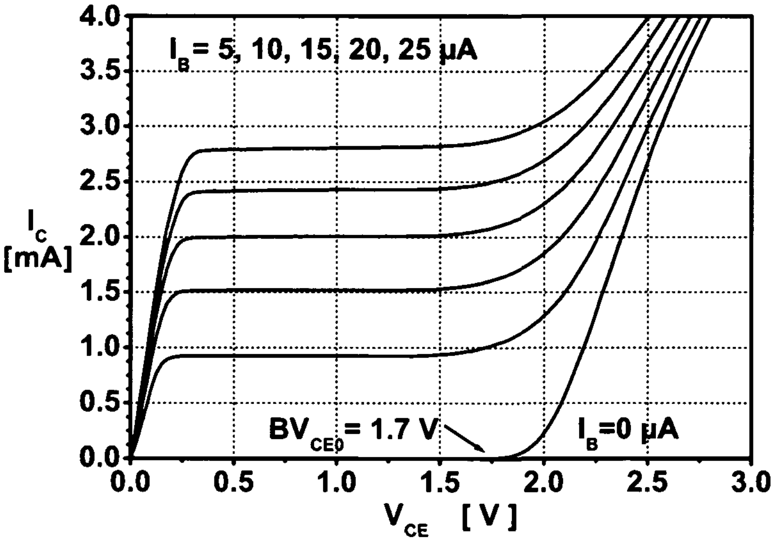


Figure 2.8: Output characteristics ($A_E = 0.14 \times 2.6\,\mu\text{m}^2$)

The high-frequency performance of the SiGe HBTs has been evaluated using S-parameter measurements up to 30 GHz. The cutoff frequency f_T has been extrapolated from the small signal current gain using transistors with an emitter area of $0.14 \times 2.6\,\mu\text{m}^2$. Figure 2.9 shows the dependency of cutoff frequency f_T on the collector current I_C for different base-collector voltages V_{BC}. The transit frequency reaches its maximum of 200 GHz at $V_{BC} = 0\,\text{V}$ and a collector current density of about $8\,\text{mA}/\mu\text{m}^2$.

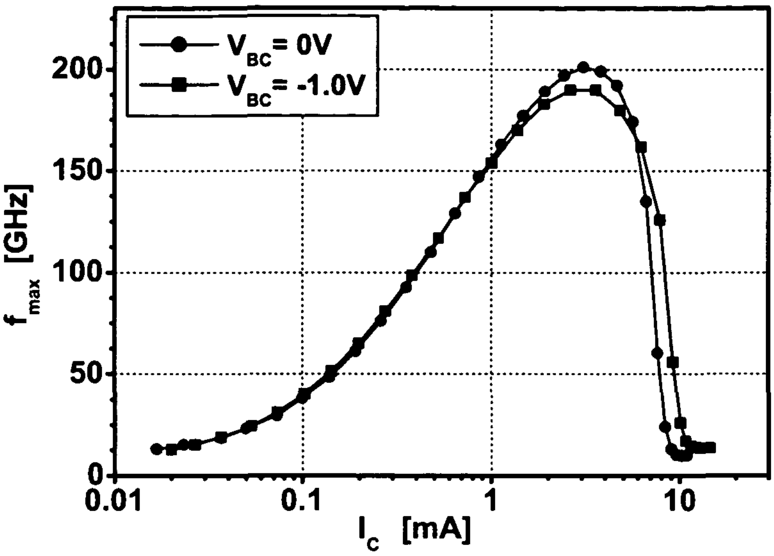


Figure 2.9: Cutoff frequency f_T vs. collector current I_C $(A_E = 0.14 \times 2.6\,\mu\text{m}^2)$

The maximum oscillation frequency f_{max} has been extrapolated from Mason's unilateral gain at 25 GHz with a slope of −20 dB/dec. Figure 2.10 shows the dependency of the maximum oscillation frequency on collector current. At $V_{BC} = -1\,\text{V}$ the maximum oscillation frequency peaks at 275 GHz.

The high values of f_{max} originate from the integration of the thin base layer into a self-aligned transistor architecture providing low capacitances and extrinsic series resistances as well as a careful optimization of the highly boron doped base for achieving

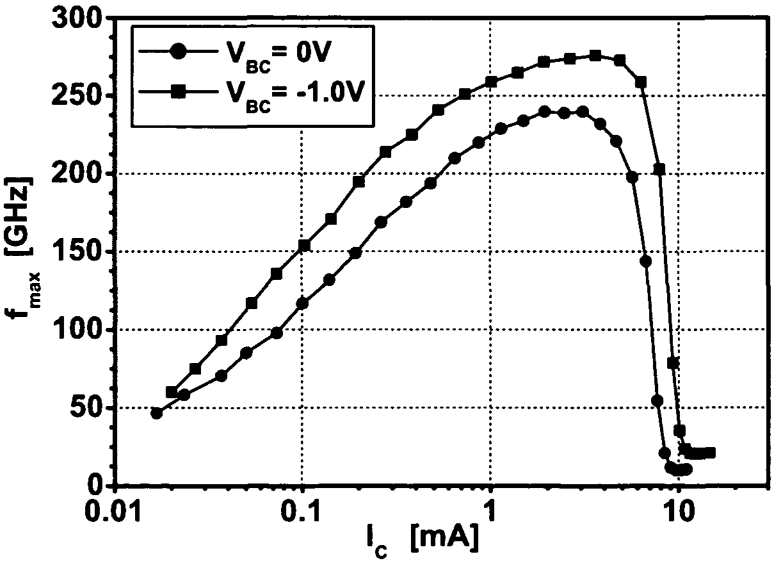


Figure 2.10: Maximum oscillation frequency f_{max} vs. collector current I_C $(A_E = 0.14 \times 2.6\,\mu\text{m}^2)$

simultaneously high cutoff frequency and low base sheet resistance. Table 2.1 summarizes the most important transistor parameters. The tradeoffs between these transistor parameters have been optimized for a balanced compromise to enable high-frequency circuit applications. The high values of cutoff frequency have been combined with a low base resistance R_B of 50 Ω. The values for emitter-base capacitance C_{EB}, base-collector capacitance C_{BC} and collector-substrate capacitance C_{CS} in Tab. 2.1 refer to unbiased junctions and include the wiring parasitic capacitances up to the first metallization layer. Taking into account the high base and collector doping levels, which have been employed in the technology for achieving high cutoff frequency, high current carrying capability, and low base resistance, the double-polysilicon self-aligned emitter-base configuration has provided reasonable low values for emitter-base and base-collector capacitances of 6.3 fF and 5.5 fF, respectively.

A_E	$0.14 \times 2.6\ \mu m^2$
β	250
R_{BI}	2.8 kΩ/□
BV_{CE0}	1.7 V
BV_{CB0}	5.8 V
C_{EB}	6.3 fF
C_{BC}	5.5 fF
C_{CS}	3.7 fF
R_B	50 Ω
R_E	3.5 Ω
R_C	7.5 Ω
f_T	200 GHz
f_{max}	275 GHz
gate delay	3.5 ps

Table 2.1: Device parameters

Transistor Geometries

Design packages usually provide transistors with different geometries. The choice of the correct transistor geometry is of great importance in order to minimize the influence of parasitic capacitances and resistances. In case of maximizing the high frequency capability of the transistor, the optimum collector current I_{C-OPT} is defined by the effective emitter area and the collector current density at maximum cutoff frequency. In this case, the emitter width is usually chosen as small as possible, according to the design rules, in order to assure the lowest base resistance which is possible. The emitter length results from the desired collector current.

For transistors with a low emitter length the area ratio of the "external" to the "internal" transistor becomes worse. But in order to guarantee low power dissipation, collector currents must be kept low which leads to a low emitter length. For high operation frequencies the collector current must be chosen high enough, because parasitic capacitances must be charged very fast. In Fig. 2.11 the optimum collector current, the parasitic base-collector capacitance, the collector-substrate capacitance and the base resistance are compared at different emitter lengths. The diagram is normalized to the values of a transistor with an emitter length of 5 μm. In Fig. 2.11 it can be seen, that for decreasing the emitter length, parasitic capacitances do not decrease as much as the maximum collector current. So, the high frequency behavior of transistors with a low emitter length is dominated by these parasitics.

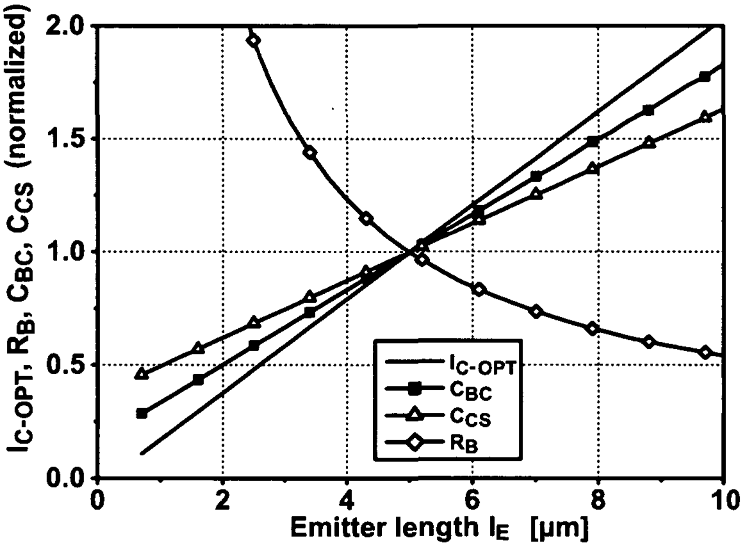


Figure 2.11: Optimum collector current I_{C-OPT}, total base resistance R_B, total base-collector capacitance C_{BC}, and the collector-substrate capacitance C_{CS} vs. emitter length (normalized to an emitter length of 5 μm)

Base, emitter and collector contacts can be arranged in various ways, as long as design rules of the technology are fulfilled. For bipolar transistors the contacts are typically arranged as parallel bars, because this configuration exhibits a good tradeoff between all transistor parameters. Figure 2.12 shows transistors with one and two base contacts with a contact formation of BEC and BEBC, respectively. The double base transistor (BEBC) shows a reduced base resistance compared to the single base transistor (BEC), because the base is contacted from both sides. However the base-collector capacitance of this configuration is higher, because there is a larger overlap between collector and base contact. The collector-substrate capacitance is increased as well, because of the larger buried layer area. Further, there is a higher collector contact resistance because the distance between active transistor and collector contact is enlarged. Table 2.2 shows the quantitative changes of the main parasitics if a double base transistor is used instead of a single base transistor. It is assumed that both transistors operate at the same bias

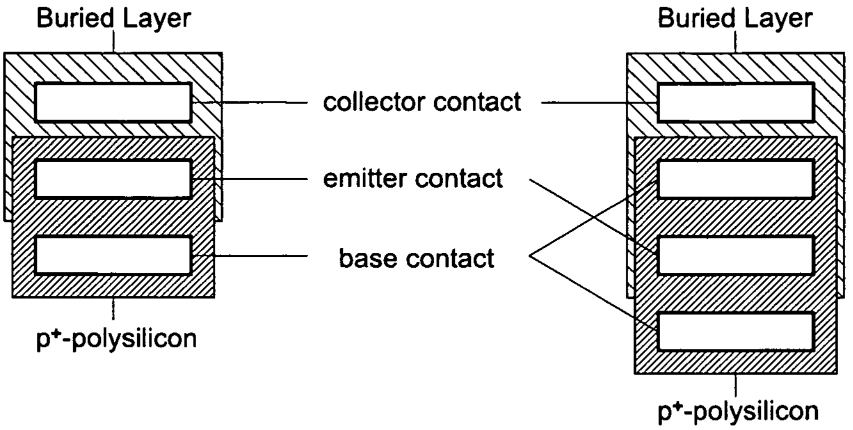


Figure 2.12: Single and double base transistor configuration [Knapp 99]

R_B	$-10\,\%$ (l_E=2 μm) $-18\,\%$ (l_E=10 μm) $-35\,\%$ (l_E=20 μm)
C_{BC}	$+10\,\%$
C_{CS}	$+15\,\%$
R_C	$+25\,\%$

Table 2.2: Difference of parasitics R_B, C_{BC}, C_{CS}, and R_C from transistors with BEBC and BEC configuration. The relative decrease of R_B depends on the emitter length l_E.

conditions and that the only technological difference is the configuration of the contacts.

Depending on the most important parameter of Tab. 2.2 for the particular circuit performance, the optimal transistor geometry and the optimum emitter area must be chosen. In general, the BEBC configuration should be chosen for very long transistors or if especially low base resistances are required. Transistors in low-noise amplifiers or the RF transistors in mixers, for example, should exhibit a low base resistance because of its contribution to the overall noise performance. In many digital circuits, instead, C_{BC} is the most sensitive parameter, especially if low power consumption is required. In such cases, the BEC transistor configuration should be chosen.

In many circuits there are transistors which collectors are connected, e.g. the transistors of a Gilbert Cell are connected crosswise or the transistors of emitter followers in fully-differential circuits. In such cases, it is better to use the transistor configuration shown in Fig. 2.13 instead of two transistors with their collector connected via metallization layers. The transistor configuration in Fig. 2.13 consists of two transistors that use the same collector contact. This configuration exhibits a smaller buried layer area compared to the use of two separated transistors. This results in a decrease of the collector-substrate

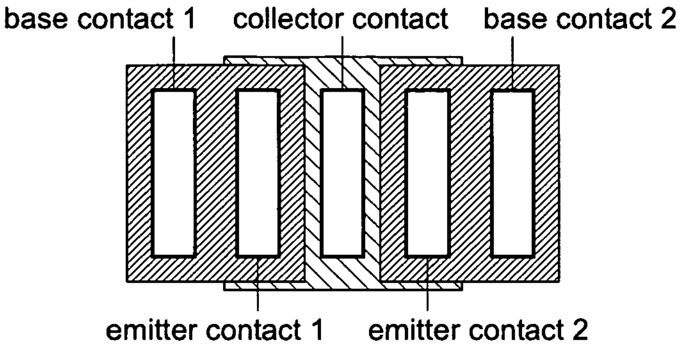


Figure 2.13: Double-transistor with a BECEB contact configuration [Knapp 99]

capacitance of 30 % to 45 %. Other transistor parameters are not affected. Especially for emitter followers in differential circuits an additional inductivity between the collector contacts due to wiring can deteriorate the transfer function. This is avoided by the use of transistors with BECEB configuration. A further advantage is that the double-transistor of Fig. 2.13 requires less space.

2.5 Passive Devices

To enable high performance circuit applications several additional devices have been added to the high frequency npn transistor. Three types of resistors and a MIM capacitor are available. The poly-resistors are made of the p+-polysilicon base electrodes but with less boron doping which results in sheet resistances of $150\,\Omega/\Box$ and $1000\,\Omega/\Box$, respectively. The high precision TaN metal resistor and the MIM capacitor are described in more detail in [Schwerd 03]. The TaN metal resistor is placed between the first and the second copper metallization layer and has a sheet resistance of $20\,\Omega/\Box$. The MIM capacitor has a specific capacitance of $1.4\,\mathrm{fF}/\mu m^2$ and is integrated between the second and third metallization layer. The MIM capacitor uses a 50 nm thick Al_2O_2 dielectric layer which has been deposited by atomic layer deposition.

2.6 Metallization

Figure 2.14 shows the metallization stack of Infineon's preproduction technology B10HF.

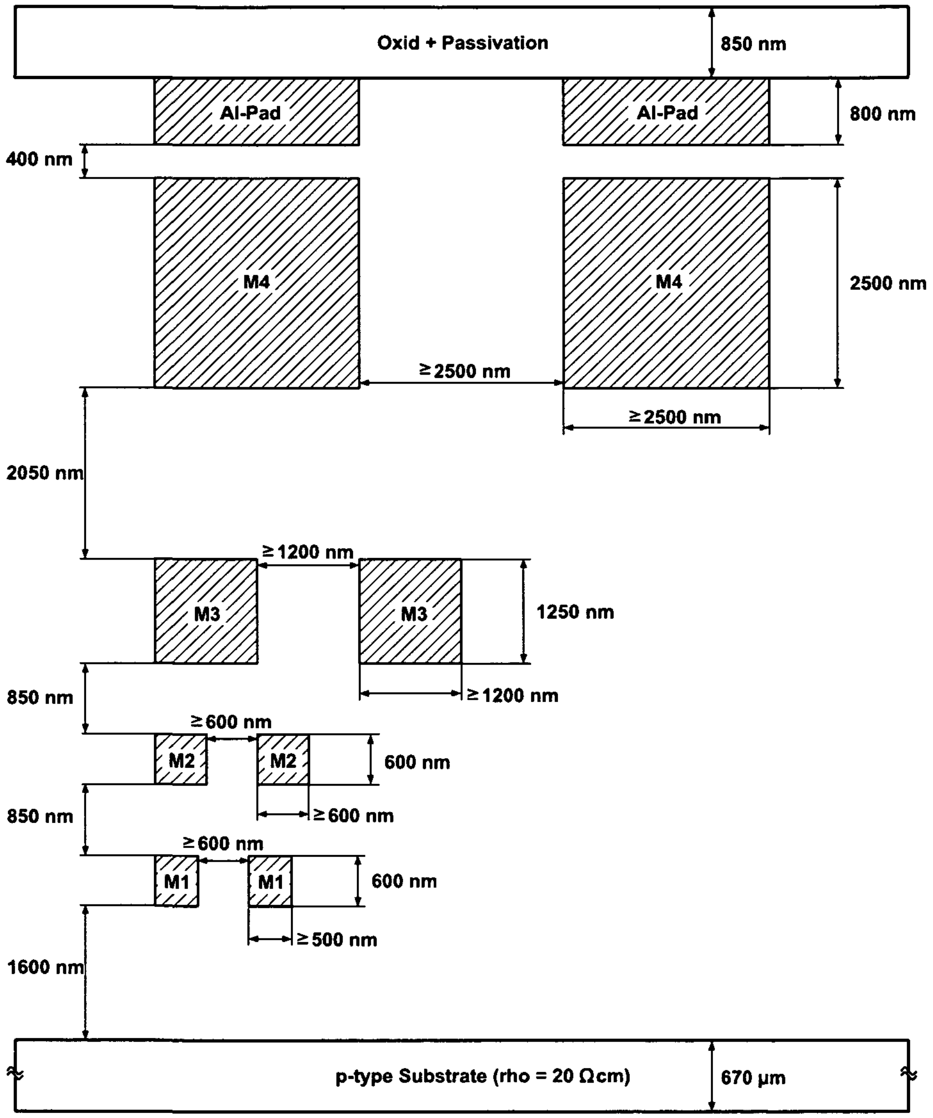


Figure 2.14: Schematic cross section of the metal layer stack including design rules

Chapter 3

Design of a Broadband Amplifier for 100 Gbit/s Data Signals

In this chapter a broadband amplifier in SiGe bipolar technology is presented. The amplifier is based on lumped elements and is designed for very high bit rate applications as well as for amplification of sinusoidal signals of very high frequencies. At first a short introduction and an overview of state-of-the art broadband amplifiers are given. Then important circuit characteristics are discussed before details of the circuit design are presented. Finally the layout and measurement results for sinusoidal signals and data signals are shown.

3.1 Introduction

In the last decade the demand on data communication has exploded and it is still growing. Innovative compression algorithms try to reduce the amount of data but they can not keep pace with the increasing volume of data traffic. Due to this trend, continuous development of communication systems towards higher bit rates is required.

In Fig. 3.1 an optical communication system is shown. On top of the figure there is the transmitter which consists of a multiplexer (MUX), the modulator, and the laser. The multiplexer combines parallel data channels of low bit rate into one data stream of high bit rate by time division multiplex. The conversion of electrical into optical signals is done either by switching a laser on and off or by modulating a constant laser source. Optical transceivers for very high bit rates usually use a modulator because of its higher bandwidth. This modulator needs an excitation around 2 to 5 V_{PP}. On this account the high bit rate data signal must be amplified with as little distortion on the signal waveform as possible.

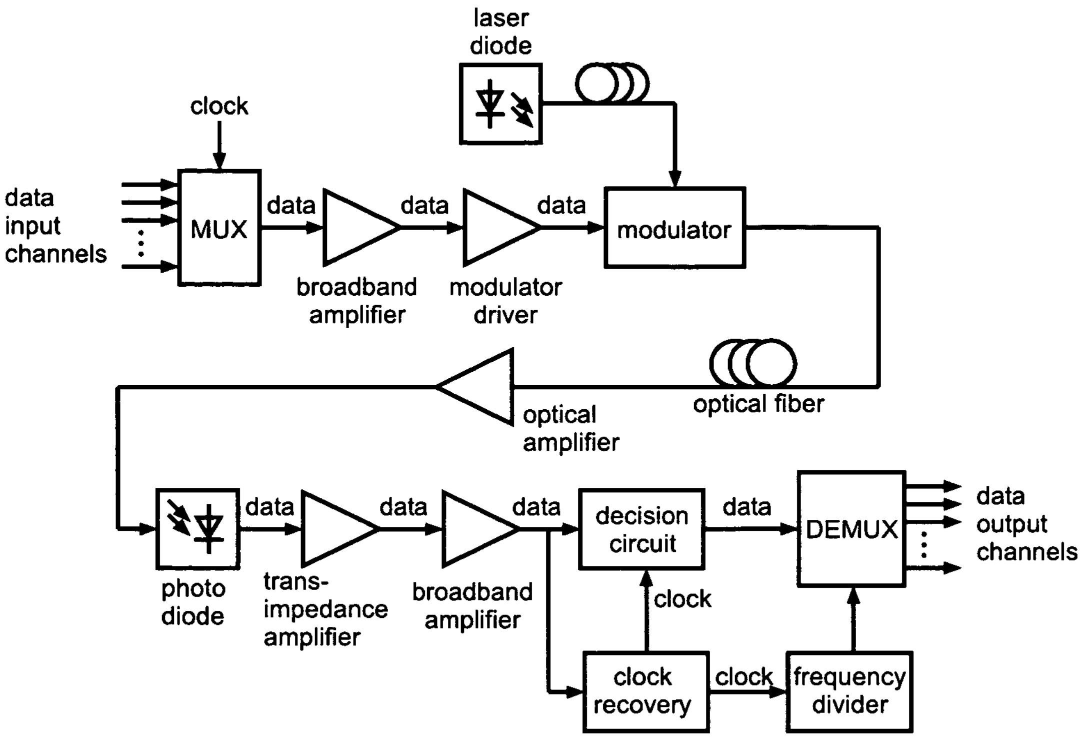


Figure 3.1: Block diagram of an optical transmission system

The modulated light is injected into an optical fiber which transmits the light to the receiver. In wide area networks, optical fiber amplifiers are used in order to enhance the maximum distance between transmitter and receiver.

At the receiver a photodiode converts the high bit rate optical data stream back into an electrical signal. A transimpedance amplifier provides low-noise amplification of the data sequence. The subsequent amplifier is used for further amplification and for limiting the amplitude, which is done by either automatic gain control or by operation in the limiting mode. This signal is sampled and digitized in the decision circuit and then separated into its original, low bit rate data signals in the demultiplexer (DEMUX). The clock signals for the decision circuit and the demultiplexer are generated by the clock recovery unit and a frequency divider, respectively.

The performance of the transmission system is basically defined by the analog components (transimpedance amplifier, modulator driver and broadband amplifier) and the optoelectronic interconnections (modulator and photodiode). Digital circuits have been published so far up to much higher data rates, e.g. in [Meghelli 04a] a 4:1 multiplexer up to 108 Gbit/s, in [Wohlgemuth 04] a demultiplexer up to 86 GHz and in [Rylyakov 04] and [Knapp 03] state-of-the-art static frequency dividers are shown. In [Meghelli 04b], [Reinhold 01], and [Wurzer 98] clock recovery systems up to a data rate of 43 Gbit/s and 40 Gbit/s, respectively, are presented. These circuits have been fabricated in silicon-based technologies.

Analog building blocks have not reached such high data rates up to now. In [Weiner 04] a SiGe transimpedance amplifier with a measured output data stream of 40 Gbit/s is presented. Broadband amplifiers and modulator drivers are reported also for data rates up to slightly more than 40 Gbit/s. An overview of state-of-the-art broadband amplifiers is given in Tab. 3.1.

The aim of this work is the design and optimization of broadband amplifiers based on lumped elements using an advanced SiGe bipolar technology. The amplifier is intended as preamplifier of high bit rate data streams either in front of the modulator driver or in front of the decision circuit or the clock recovery, see Fig. 3.1. In this field of applications the amplifier should provide clear data signals with sufficiently high amplitude.

Another application area is the amplification of single-frequency signals like the clock signals in Fig. 3.1. Although these signals are narrow-band, a broadband amplifier is advantageous. Especially in the development stage the system is tested with various clock rates, so a broadband amplifier with a high bandwidth covers the whole frequency range.

Further fields of application are as linear amplifier in conventional high frequency systems. The amplifier is also applicable in ultra wideband (UWB) communication systems like orthogonal frequency division multiplex (OFDM) systems for terrestrial TV tuners or wideband radar detectors.

3.1.1 State of the Art

Broadband amplifiers are either based on a lumped or on a distributed concept. In Section 3.2 the two concepts are discussed. In this section outstanding results for broadband amplifiers of both concepts are mentioned and an overview of state-of-the-art amplifiers is given.

In Tab. 3.1 published broadband amplifiers are compared. In the upper part of the table, lumped broadband amplifiers are listed. The lower part of the table gives results for broadband amplifiers based on a distributed concept.

Broadband amplifiers based on lumped elements are presented in [Wohlgemuth 03], [Baeyens 02], and [Choudhury 04]. In [Wohlgemuth 03] an amplifier using SiGe hetero junction bipolar transistors (HBTs) is presented which exhibits a gain of 36 dB and a bandwidth of 26 GHz. An InP HBT amplifier is described in [Baeyens 02] with 21 dB gain and 38 GHz bandwidth. Another InP HBT based wideband amplifier with bessel transfer function, a gain of 11 dB, and a bandwidth of more than 50 GHz is presented in [Choudhury 04].

Broadband amplifiers based on distributed concepts using InP high electron mobility transistors (HEMTs) are presented in [Masuda 02] and [Meliani 02] and exhibit a bandwidth of more than 110 GHz and 92 GHz, respectively. The highest bandwidth of a distributed amplifier using SiGe HBTs reaches a bandwidth of 80 GHz [Wohlgemuth 03]. In the summary of this chapter the results achieved in this work are compared with the state of the art.

Reference	measured 3-db bandwidth [GHz]	measured gain [dB]	measured eye diagram [Gbit/s]	Technology
[Lao 97]	30	36	—	GaAs HEMT
[Krishnan 00]	80	8.2	—	InAs HBT
[Krishnan 00]	50	18	—	InAs HBT
[Ohhata 01]	47.8	21.5	40	GaAs HEMT
[Baeyens 02]	38	21	40	InP HBT
[Freeman 02]	35	28	40	SiGe BiCMOS
[Toifl 03]	23	18	30	CMOS
[Wohlgemuth 03]	26	36	43	SiGe HBT
[Choudhury 04]	50	11	—	InP HBT
[Krishnan 00]	80	11.5	—	InAs HBT
[Leich 01]	66	12	40	GaAs HEMT
[Baeyens 02]	80	25	—	InP HBT
[Baeyens 02]	58	15	40	InP HBT
[Masuda 02]	110	7.5	—	InP HEMT
[Masuda 02]	94	14.5	—	InP HEMT
[Meliani 02]	92	13	—	InP HEMT
[Wohlgemuth 03]	81	13	—	SiGe HBT
[Wohlgemuth 03]	37	27	43	SiGe HBT
[Shigematsu 04]	39	4	40	CMOS
[Kim 04]	90	11	—	CMOS

Table 3.1: Comparison of state-of-the-art monolithical integrated broadband amplifiers. In the upper part of the table lumped amplifiers are listed, in the lower part of the table data for distributed broadband amplifiers is given.

3.1.2 Specification of Circuit Parameters

In this work a broadband amplifier for multiple applications is designed. The amplifier should be applicable for high bit rate data streams, as well as high frequency sinusoidal signals and ultra-wideband signals. Due to different fields of applications, tradeoffs between circuit parameters are necessary. The most important requirements for the broadband amplifier of this work are:

1. Differential gain = 16 dB:
   High Gain and high bandwidth are contradicting requirements. In this design the bandwidth of the amplifier is optimized for a differential gain of 16 dB.

2. Bandwidth:
   High bandwidth is of particular importance in the case of amplifying sinusoidal signals of high frequencies, for example, clock signals. In digital applications a gradual decrease of the gain opposed to high bandwidth often avoids excessive group delay peaking and deteriorated eye diagrams. Therefore, in this work bandwidth is maximized after specification of a transfer characteristic.

3. Frequency response:
   In this work, a Butterworth characteristic is chosen as frequency response since it is a good compromise between high bandwidth and small overshoot of the step response in the time domain.

4. Output Voltage Swing $\geq 1\,\mathrm{V_{PP}}$:
   A high output voltage swing is required for excitation of the modulator driver. Recent developments of electroabsorption modulators tend to driving voltages of 1.1 V [Fukano 04], so a broadband amplifier with high output voltage swing can replace the modulator driver.

5. Data rate $\geq$ 80 Gbit/s:
   The aim of this development is to reach clear output eye diagrams at a bit rate of 80 Gbit/s or more.

6. Matching at input and output:
   Due to the high operation frequency and the high bandwidth, matching at the input and the output is required within the whole frequency range.

7. Linearity:
   If the broadband amplifier is used as linear amplifier a high 1-dB compression point and a high 3^{rd}-order intercept point are desirable. High linearity can be achieved more easily in combination with a high output voltage swing.

8. Supply Voltage:
   A negative supply voltage of -5 V is chosen.

3.2 Fundamental Circuit Characteristics

3.2.1 Broadband Amplifier Concepts

Basically, there are two concepts on which broadband amplifiers can be based on, see Fig. 3.2. The lumped broadband amplifier, shown in Fig. 3.2(a) consists of one or several stages of emitter follower and differential amplifier combinations. The total gain of lumped amplifiers is the product of the gain of each stage. However, the overall bandwidth is less than the bandwidth of each stage because the gain fall-off in each stage will accumulate. The inherent parasitic capacitances of the transistors cause the bandwidth limitation in broadband amplifiers.

An approach to increase the bandwidth of broadband amplifiers is distributed amplification [Wong 93]. A distributed amplifier, see Fig. 3.2(b), consists of gain stages which are separated by transmission lines. The total gain of distributed amplifiers is the sum of the gain of each stage. Distributed amplifiers obtain high bandwidth by absorbing the transistor capacitances into a synthetic transmission line at the input and at the output. Equal delays of the input and output transmission line are required, so that the output currents of the stages are added in-phase at the load. Since input capacitances are usually larger than output capacitances, additional capacitances at the output line are necessary. In the absence of loss, the gain-bandwidth product of the amplifier can be improved arbitrarily by increasing the number of stages. In practice, the improvement is limited by the loss of the transmission line, which is composed of the loss in each transmission line segment between the stages and the input resistance of the transistors. Due to the parasitic base resistance of bipolar transistors the distributed concept is particularly suitable for field-effect based devices, like CMOS transistors or HEMT's.

The design of distributed amplifiers requires careful electromagnetic simulations and very accurate modeling of transistor parasitics in order to obtain a constant gain. It is very

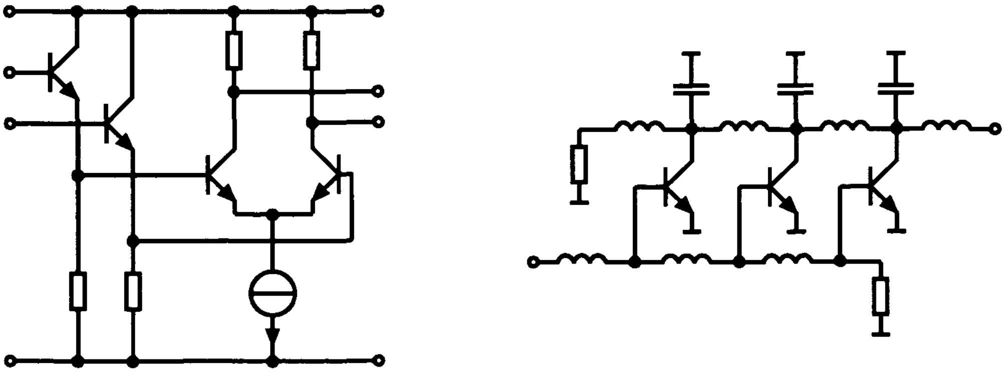

(a) lumped amplifier (b) distributed amplifier

Figure 3.2: Basic concepts of broadband amplifiers

difficult to simultaneously yield a linear phase over the pass-band which is required in order to avoid distortion of data signals.

A disadvantage of distributed amplifiers is that there is a DC level at the input and output line which involves AC coupling. From this it follows that there is a lower cutoff frequency, so distributed amplifiers do not work at DC or low frequencies. In order to yield high gain with distributed amplifiers, many stages are required since the gain is added from all stages as compared to lumped amplifiers where the gain of all stages is multiplied. Distributed amplifiers often exhibit a very sharp gain fall-off which leads to excessive group delay peaking and deteriorated eye diagrams.

Due to the wide-spread field of applications the amplifier of this work is intended for, a concept based on lumped elements is chosen. The main difficulties are to maximize the bandwidth of the circuit at a predefined gain.

3.2.2 Frequency Response

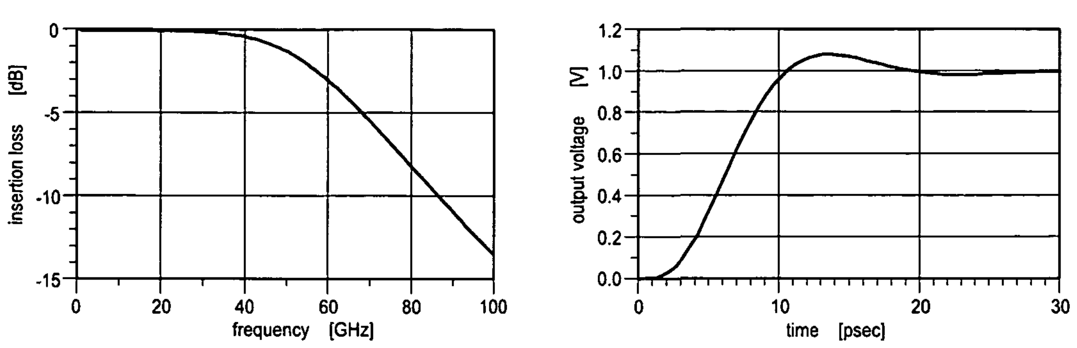
A broadband amplifier should exhibit a near-constant gain and linear phase in the pass-band at a high bandwidth. Between these requirements a compromise is necessary. Constant gain at high bandwidth causes group delay peaking. A flat group delay (=linear phase) results in a slowly decaying gain, which can only be realized at a lower bandwidth. In this work, Butterworth characteristic is chosen as frequency response since it is a good compromise between high bandwidth, a flat group delay, and a small overshoot of the step response in the time domain. Above all, a differential amplifier with emitter followers at its input shows a frequency response which is similar to the Butterworth characteristic.

The frequency response $|H(f)|$ of a Butterworth low-pass filter at a frequency f can be calculated as

$$|H(f)|^2 = 10 \log \left(\frac{1}{1 + (f/f_c)^{2n}} \right) \tag{3.1}$$

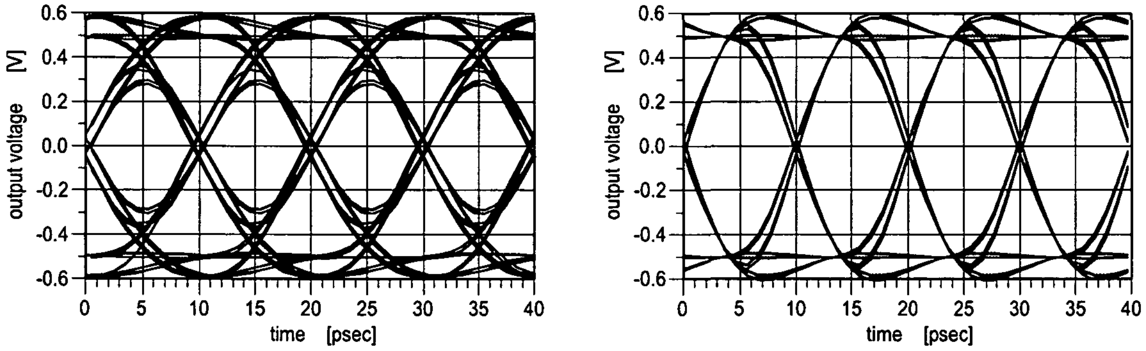
where f_c denotes the 3-dB bandwidth and n is the order of the filter. In Fig. 3.3(a) this frequency response and the step response for a 3^{rd}-order Butterworth filter with a bandwidth of 60 GHz are plotted. The step response of the Butterworth filter exhibits overshoot depending on the filter order, see Tab. 3.2.

In Fig. 3.4 simulated output eye diagrams at a data rate of 100 Gbit/s from a transmission system with a Butterworth transfer characteristic of 3^{rd}-order are shown for different filter bandwidths. It can be seen that a filter-bandwidth to data rate ratio of 2 : 3 is sufficient for obtaining clear eye diagrams. Further, an increase of the time-jitter at the zero-crossings at lower filter bandwidths can be observed.

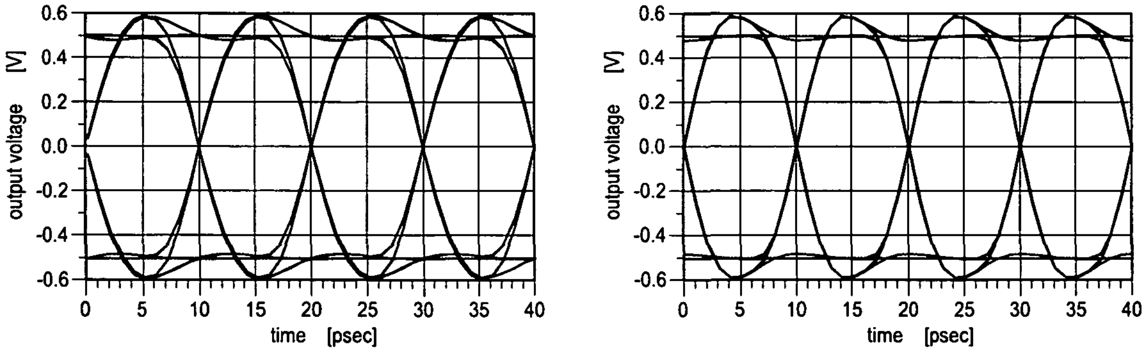


(a) Frequency response (b) Step response

Figure 3.3: Simulated frequency response and step response of a 3rd-order Butterworth filter with a 3-dB bandwidth of 60 GHz



(a) Filter bandwidth = 40 GHz (b) Filter bandwidth = 60 GHz



(c) Filter bandwidth = 80 GHz (d) Filter bandwidth = 100 GHz

Figure 3.4: Simulated 100 Gbit/s eye diagrams at the output of a system with a Butterworth transfer characteristic (filter order = 3, filter bandwidth = 40, 60, 80 and 100 GHz)

Filter order	Overshoot
2	4 %
4	11 %
6	14 %
8	16 %

Table 3.2: Time-domain performance comparison of Butterworth low-pass filters with different order [Horowitz 89]

3.2.3 Operation in Limiting Mode

A typical transfer characteristic of an amplifier is shown in Fig. 3.5. In the case of small signal excitation the amplifier exhibits an almost linear behavior. In case of high amplitudes, the top and bottom portions of the waveform are clipped. This property can be beneficial for amplification of distorted data signals. In Fig. 3.5 regeneration of a distorted data signal is provided by operation of the amplifier in limiting mode.

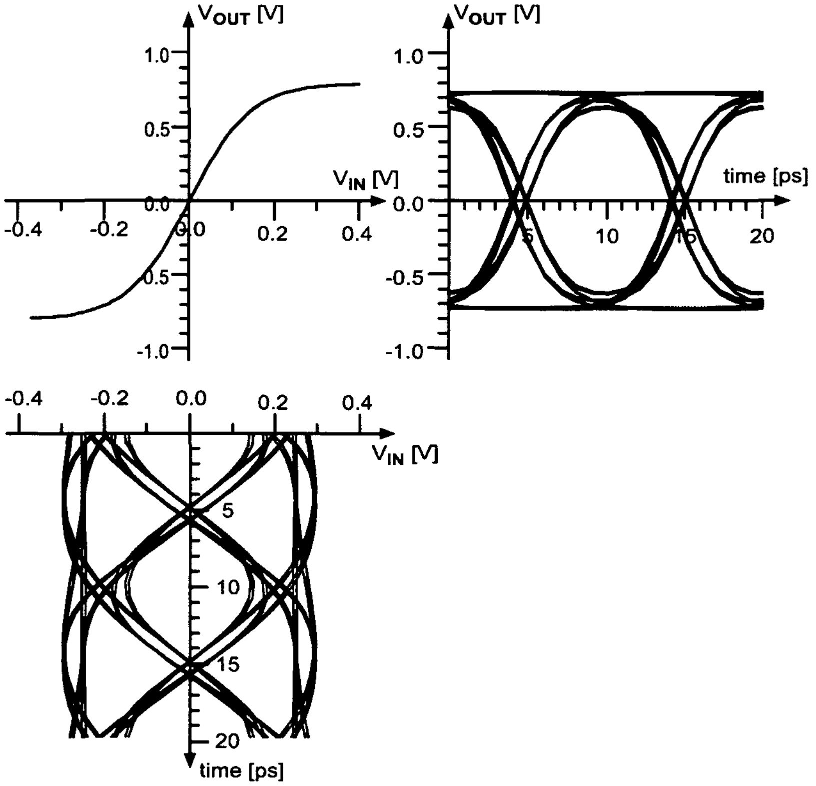


Figure 3.5: Differential amplifier in limiting mode

3.2.4 Linearity

In the case of small signal excitation the amplifier can be treated in good approximation as linear circuit. The limits of the linear operation region are characterized by the 1-dB compression point and the 3rd-order intercept point, which are the most common measures of linearity. A nonlinear transfer function can be written as series expansion:

$$v_{OUT}(t) = k_0 + k_1\, v_{IN}(t) + k_2\, v_{IN}^2(t) + k_3\, v_{IN}^3(t) + \dots \tag{3.2}$$

In the following calculations (3.2) is assumed as a noninverting function with compression at high signal amplitudes V, which results in $k_1 > 0$ and $k_3 < 0$. Due to the nonlinear behavior, harmonics and mixing products occur at the device output at signal frequencies of $2\omega_1$, $2\omega_2$, $3\omega_1$, $3\omega_2$, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, $2\omega_2 \pm \omega_1$, … . Harmonics and even order mixing products are uncritical because they can be easily filtered out. Of all unwanted terms, mixing frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most troublesome, since they are near the signal frequencies, if ω_1 is close to ω_2. Table 3.3 shows amplitudes of signal components of the output of a nonlinear device excited by a single or double tone input signal. For this calculation the first three terms of the series expansion are considered.

frequency	$v_{IN} = V\,[\cos(\omega_1 t) + \cos(\omega_2 t)]$	$v_{IN} = V \cos(\omega t)$
DC	$k_0 + k_2 V^2$	$k_0 + \frac{1}{2} k_2 V^2$
ω_1 ω_2	$k_1 V + \frac{9}{4} k_3 V^3$	$k_1 V + \frac{3}{4} k_3 V^3$
$2\omega_1 - \omega_2$ $2\omega_2 - \omega_1$	$\frac{3}{4}\,\lvert k_3\rvert\, V^3$	——

Table 3.3: Amplitudes of frequency components of an output signal v_{out} for single and double tone excitation of a nonlinear function. The nonlinear behavior is described by a series expansion of third order, see (3.2).

3.2.5 Third-Order Intercept Point

The third-order intercept point is measured by applying two signals with frequencies ω_1 and ω_2 and equal amplitudes to the circuit. The third-order intercept point (IP3) is a theoretical point either referred to the input or the output where the output amplitudes of the intermodulation tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitudes of the fundamental tones at ω_1 and ω_2. For small amplitudes V the fundamental tone rises linearly (20 dB/decade) and the intermodulation products of 3rd-order rise as the cube of the input (60 dB/decade). So the 3rd-order intercept point can be expressed as:

$$\frac{k_1\, V}{\frac{3}{4}\,|k_3|\, V^3} = 1 \tag{3.3}$$

This can be solved for $V = V_{IP3}$:

$$V_{IP3} = 2\sqrt{\frac{k_1}{3\,|k_3|}} \tag{3.4}$$

where V_{IP3} is the input voltage at the 3rd-order intercept point.

3.2.6 1-dB Compression Point

The 1-dB compression point is measured by applying only one signal to the circuit. The 1-dB compression point is the power level, referred to the input or the output, where the output power is 1 dB less than it would have been with an ideally linear device. The input voltage at the 1-dB compression point can be calculated as the ratio of the real to the ideal amplitude of the fundamental tone:

$$\frac{k_1\, V + \frac{3}{4}\, k_3\, V^3}{k_1\, V} = 0.89125 \tag{3.5}$$

where 0.89125 corresponds to −1 dB. Provided that $k_1 > 0$ and $k_3 < 0$ the voltage $V = V_{1dB}$ results to:

$$V_{1dB} = 0.381\sqrt{\frac{k_1}{|k_3|}} \tag{3.6}$$

Note that this analysis is valid for third order nonlinearity. For higher order nonlinearities additional components occur. Third order approximation gives a good estimate of the behavior.

3.2.7 Relationship between 1-dB Compression and IP3 Points

The relationship between the 1-dB compression point and the IP3 can be derived from (3.4) and (3.6) as:

$$\frac{V_{IP3}}{V_{1dB}} = \frac{2\sqrt{\frac{k_1}{3|k_3|}}}{0.381\sqrt{\frac{k_1}{|k_3|}}} = 3.04 \triangleq 9.66\,\mathrm{dB} \tag{3.7}$$

The voltage ratio of 3.04 corresponds to approximately 10 dB. So it is a good estimate that the IP3 is about 10 dB higher than the 1-dB compression point.

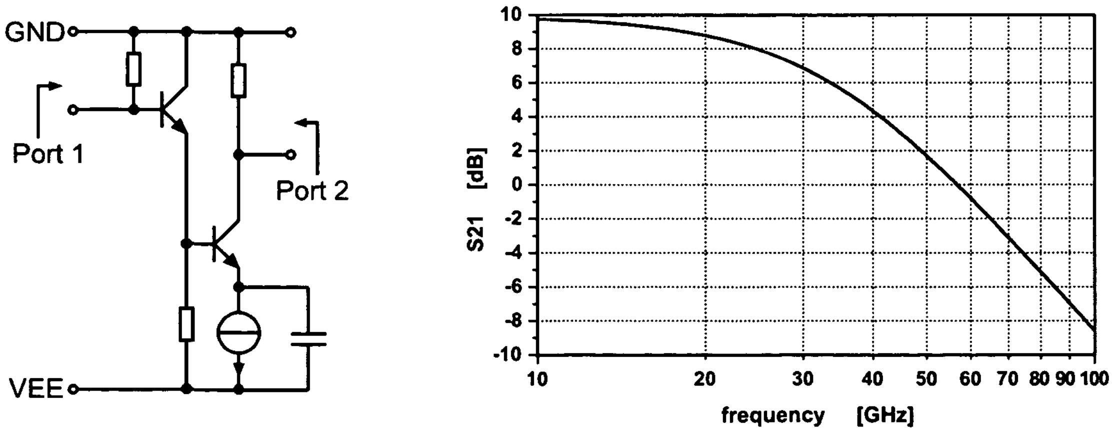
3.3 Circuit Design

The broadband amplifier in this work consists of two stages. Each stage comprises a differential amplifier with emitter followers at its input. At first, a differential amplifier is analyzed with one, two, and three emitter followers at the input. Then the design of the two stage amplifier is shown.

Emitter followers are often used as a buffer circuit due to the high input impedance and the low output impedance at a almost unity gain. In [Gray 84] the input and output impedances of the emitter follower as a function of frequency are derived for resistive source and load termination. It is calculated that the input impedance appears capacitively and that the output can show inductive behavior. This inductive output behavior can result in resonances, especially when capacitive loads are driven. This resonances can be used in order to increase the bandwidth of the whole stage. The size of the transistors and their current densities must be carefully optimized in order to yield a high bandwidth and in order to avoid resonant peaks in the frequency response.

Differential Amplifier with one Emitter Follower

In Fig. 3.6 the circuit diagram and the frequency response of a differential amplifier with one emitter follower at its input is shown. In this and the following representations an equivalent half-circuit of the fully differential circuit is simulated. The circuits of Fig. 3.6, Fig. 3.7, and Fig. 3.8 are designed for equal gain and equal output voltage swing. The 3-dB bandwidth of the circuit in Fig. 3.6 is simulated to 29.3 GHz.



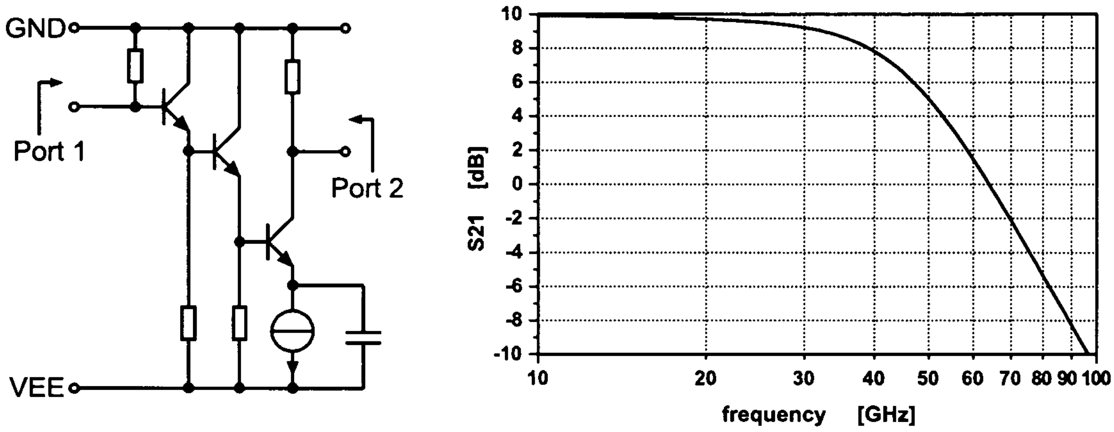
(a) Circuit Diagram

(b) Frequency response

Figure 3.6: Differential amplifier with one emitter follower

Differential Amplifier with two Emitter Followers

In Fig. 3.7 the circuit diagram and the frequency response of a differential amplifier with two emitter followers at its input is shown. The 3-dB bandwidth of this circuit is simulated to 43.3 GHz.



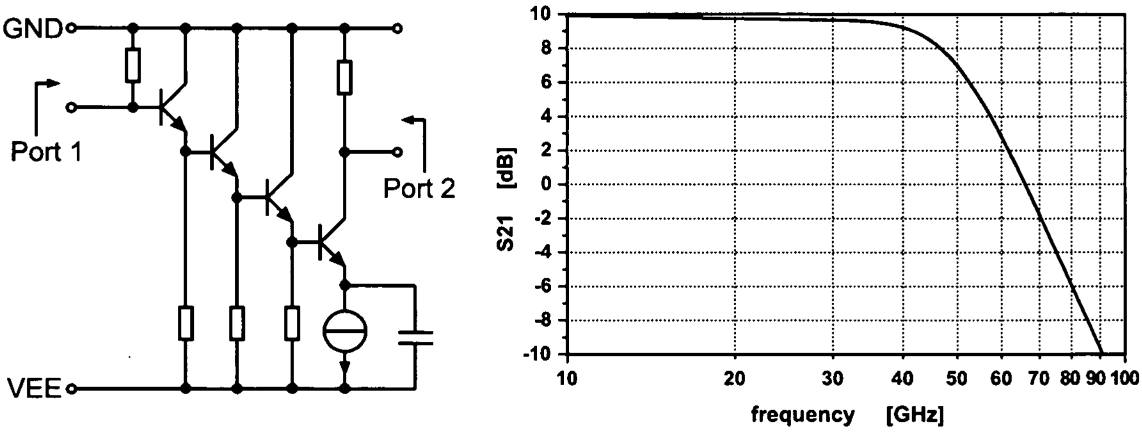
(a) Circuit diagram

(b) Frequency response

Figure 3.7: Differential amplifier with two emitter followers

Differential Amplifier with three Emitter Followers

In Fig. 3.8 the circuit diagram and the frequency response of a differential amplifier with three emitter followers at its input is shown. In this case the 3-dB bandwidth results to 49.9 GHz.



(a) Circuit diagram

(b) Frequency response

Figure 3.8: Differential amplifier with three emitter followers

Comparison of the Frequency Characteristics

In Fig. 3.9 the frequency responses from Fig. 3.6 to Fig. 3.8 are compared. It can be seen that the bandwidth of the circuit with three emitter followers is the highest. Further, the plot shows that the increase in bandwidth from one to two emitter followers is higher than the increase from two to three emitter followers.

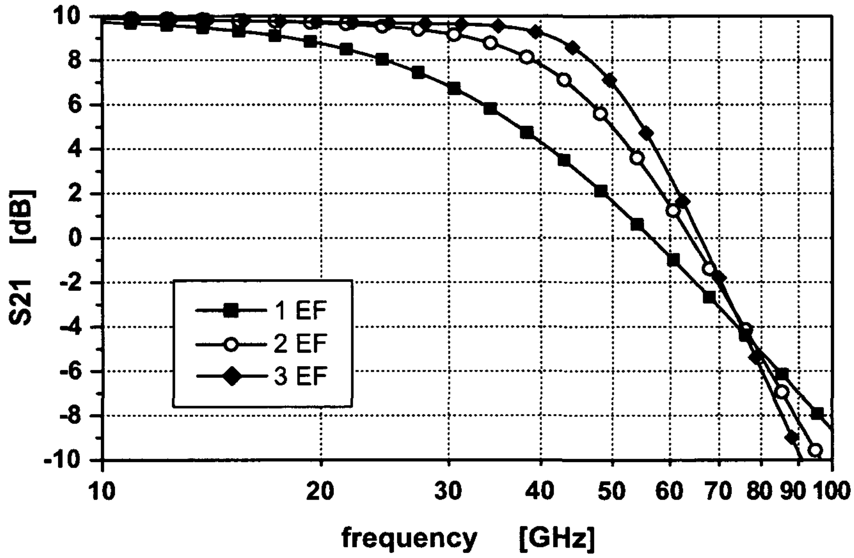


Figure 3.9: Comparison of the frequency responses from Fig. 3.6 to Fig. 3.8

3.3.1 Schematic of the two-stage Amplifier

The circuit diagram of the broadband amplifier is shown in Fig. 3.10. The broadband amplifier is based on a fully differential design and consists of two stages. The first stage consists of two emitter follower pairs and a differential amplifier. The second stage consists of three emitter follower pairs and a differential amplifier at the output. 50 Ω on-chip resistors are provided at the input and the output for broadband matching. In order to achieve a high output swing, high currents in the differential amplifiers are necessary. In addition, emitter degeneration and low load resistors are used for increasing the 3-dB bandwidth at a well-defined gain. Emitter degeneration resistors also improve the linearity of the circuit. As an adequate dimensioning for the first stage we obtained load resistors of 30 Ω and emitter degeneration resistors of 10 Ω each. In the second stage emitter degeneration resistors of 5 Ω are used. Carefully adjusted transistor sizes and currents enable a flat frequency response and a high bandwidth. The differential amplifier of the second stage is implemented as cascode configuration in order to prohibit avalanche breakdown of the output transistorgs. The cascode stage additionally minimizes the Miller effect, thereby bandwidth is increased.

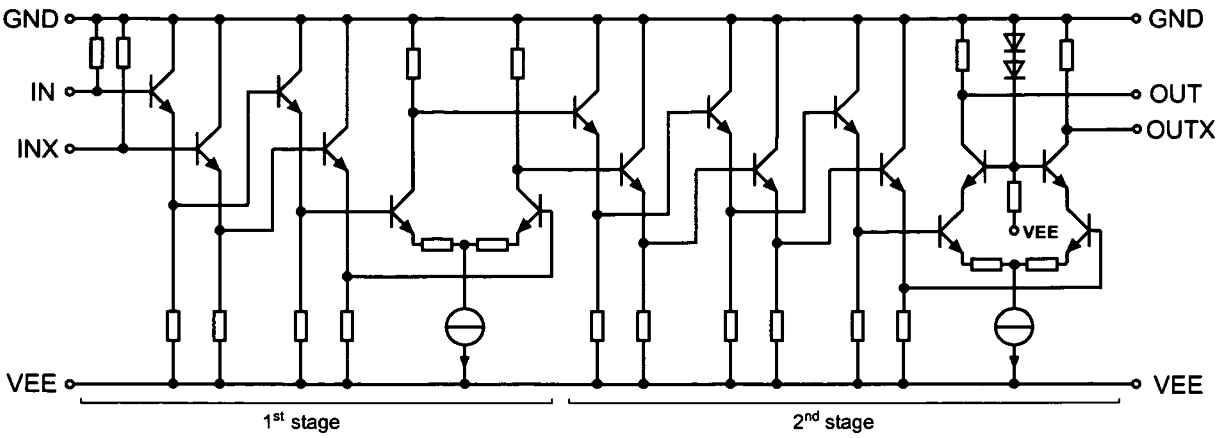


Figure 3.10: Schematic of the broadband amplifier

3.3.2 Simulation Results

Figure 3.11 shows the simulated frequency response of the schematic presented in Fig. 3.10. The simulated low frequency differential gain is 15.2 dB at a 3-dB bandwidth of 63.4 GHz.

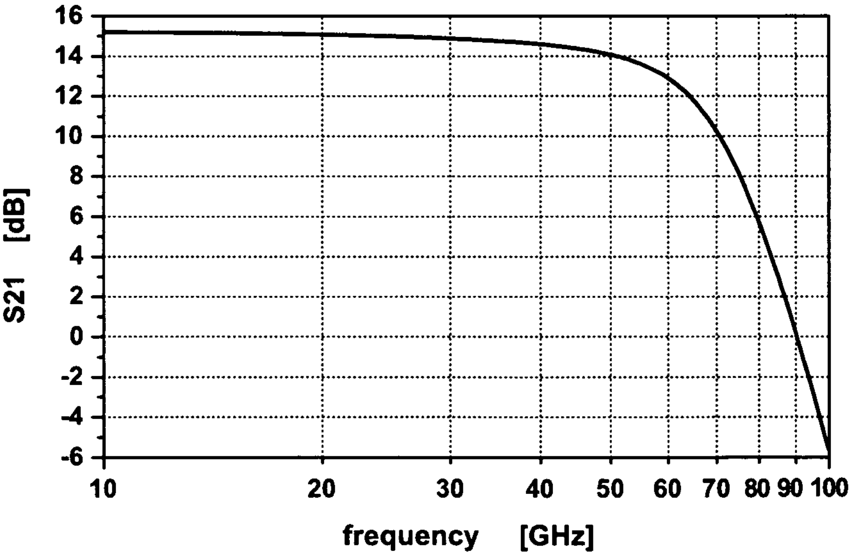


Figure 3.11: Simulated frequency response of the broadband amplifier

3.4 Layout

In Fig. 3.12 a chip photograph of the broadband amplifier is shown. The first and the second stage as well as the pads are indicated in the photograph. It can be seen that the active part of the circuit only requires a small part of the whole chip area. The die size is 550 μm × 550 μm.

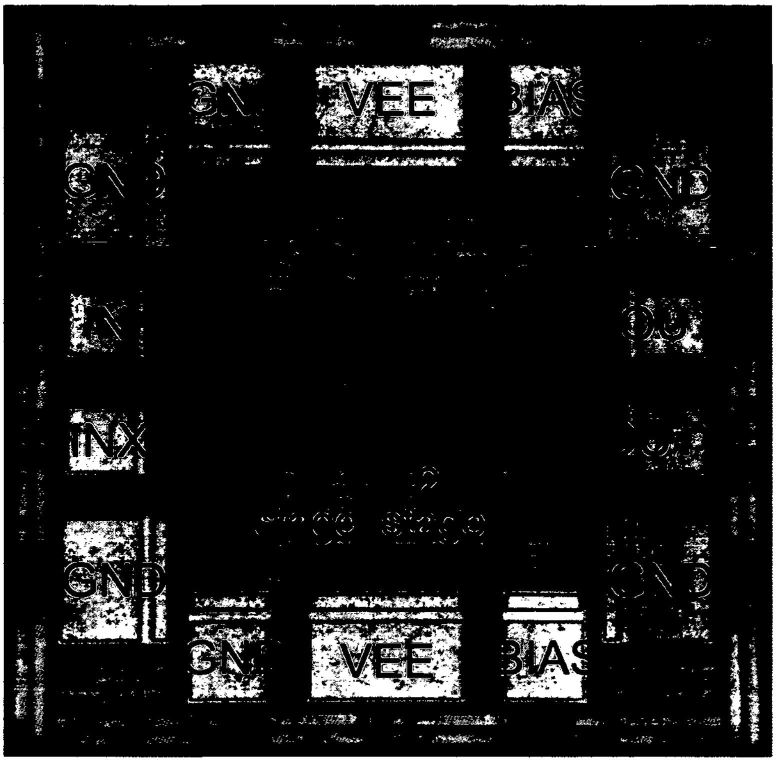


Figure 3.12: Chip photograph of the broadband amplifier (chip size: 550 μm × 550 μm)

Layout issues play an important role in monolithic circuits operating at microwave frequencies, e.g. [Rein 96]. The layout is created fully symmetrical around the horizontal axis in the middle of the chip. Only the bias feeds are asymmetrical. Symmetry is required in order to achieve a matched propagation delay for the differential signals and so avoid additional time jitter. Further, the influence of electrical and thermal interactions is reduced. The active components of the circuit are placed as close as possible in order to avoid parasitic capacitances and inductances due to complex wiring.

Another important aspect is the careful design of signal lines. Lines with a length of more than $\lambda/10$ are realized as transmission lines with a well-defined impedance, so the input and output lines are carried out as 50 Ω microstrip lines with the signal line in the top and the ground plane in the second metallization layer.

The ground (GND) and the supply (VEE) wiring is accomplished by a metal grid over the whole chip, with the exception of the active area and the pads. With this measure the parasitic inductances in the supply path are reduced. Underneath the signal pads the metal grid is excepted because this would constitute a capacitance and decrease the bandwidth. Often the buried layer is used as ground plane underneath the signal pads in order to avoid coupling into the substrate or to avoid coupling from the input to the output via the substrate. But if the ground potential is noisy this could lead to problems [Rein 96].

3.5 Measurement Results

The amplifier has been carefully characterized by S-parameter and large signal measurements as well as by excitation with high data rate signals. All measurements have been performed by applying the high frequency signals via microwave probes. The supply voltage of the broadband amplifier is −5 V. At this voltage the supply current is 155 mA which equals a power consumption of about 770 mW.

3.5.1 S-Parameter

S-parameter measurements have been performed single-ended, on-wafer using an Anritsu 360B vector network analyzer with 67 GHz GS and SG probes, respectively. In Fig. 3.13 a block diagram of the measurement setup is shown. In this diagram the GND and the VEE connection are not display.

Figure 3.14 shows the single-ended measured gain and the input and output return loss at 50 Ω source and load impedance. The single-ended low-frequency gain is 10 dB and the 3-dB bandwidth is 62 GHz. The differential gain is 16 dB. The output return loss

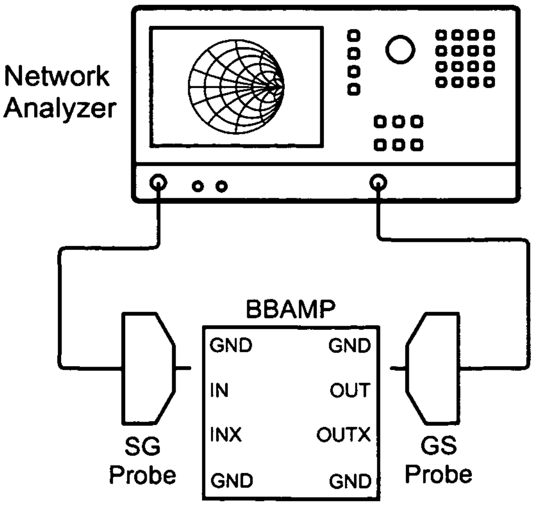


Figure 3.13: Measurement setup for S-parameter measurements

S_{22} degrades at a frequency of about 50 GHz. This results from a decrease of the output impedance with increasing frequency caused by the base-collector and the collector-substrate capacitance of the output transistor. Due to the unbalanced measurement procedure the frequency response deviates from the designed Butterworth characteristic. In the case of a single-ended excitation even a small inductance in the supply path can cause a resonance at high frequencies. In differential operation such an inductance would have no effect.

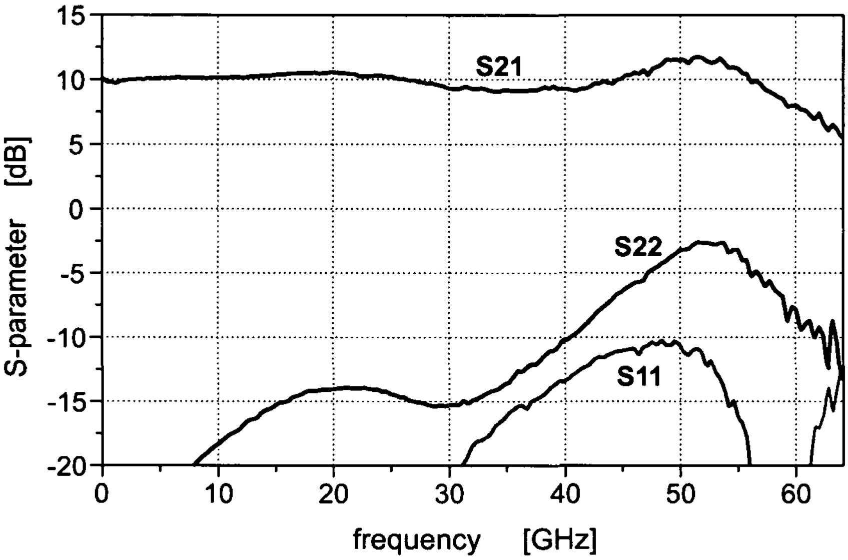


Figure 3.14: Single-ended on-wafer measurement of the S-parameters

Single-Ended versus Differential Gain

In this section the relation between single-ended and differentially measured power gain is provided. At first the voltage gain of a differential amplifier is calculated. In [Gray 84] the common-mode rejection ratio (CMRR) of a differential amplifier is derived. In the case of an ideal CMRR, the output voltage does not depend on whether the input voltage is applied single-ended or differentially. However at the output, the differential voltage is twice as high as the single-ended voltage. So the differential voltage gain A_D is twice as high as the single-ended voltage gain A_S:

$$A_S = \frac{v_{OS}}{v_{IS}}\ , \quad A_D = \frac{v_{OD}}{v_{ID}} = 2 \cdot A_S \tag{3.8}$$

For power gain considerations the input and output impedances must be taken into account. If input and output operate in differential mode, the differential power gain is 6 dB higher than the single-ended power gain because of the factor 2 in the voltage gain:

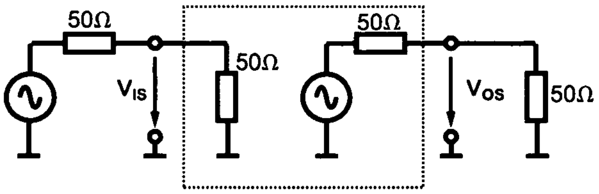


Figure 3.15: Single-ended operation mode at both input and output

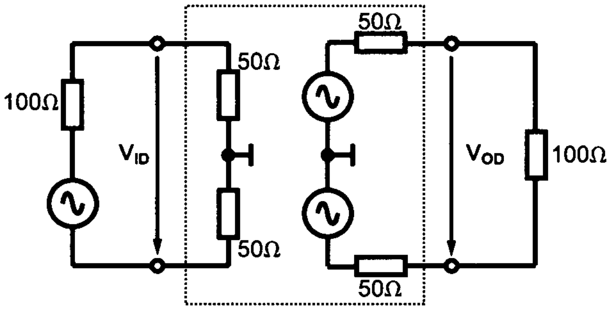


Figure 3.16: Differential operation mode at both input and output

$$G_S = \frac{\frac{v_{OS}^2}{2 \cdot 50\Omega}}{\frac{v_{IS}^2}{2 \cdot 50\Omega}} = \frac{v_{OS}^2}{v_{IS}^2} = A_S^2 \tag{3.9}$$

$$G_D = \frac{\frac{v_{OD}^2}{2 \cdot 100\Omega}}{\frac{v_{ID}^2}{2 \cdot 100\Omega}} = \frac{v_{OD}^2}{v_{ID}^2} = A_D^2 = 4 \cdot A_S^2 = 4 \cdot G_S \tag{3.10}$$

Differential operation at the output and single-ended operation at the input is present in the case the amplifier is used to symmetrize a single-ended signal. In this case, the voltage gain is twice the voltage gain of single-ended operation. But the power gain is only 3 dB higher than the single-ended power gain because the impedances at the input and the output are different.

If a differential signal is applied to the amplifier and the output is taken single-ended, the voltage gain is equal to fully single-ended operation. Also in this case the power gain is 3 dB higher than the power gain in single-ended mode due to the different impedances at input and output.

3.5.2 Single-Tone Compression Point

The large signal behavior of the broadband amplifier is analyzed on-wafer with 40 GHz GSSG-probes. In Fig. 3.17 a block diagram of the measurement setup for 1-dB compression point measurement is shown. The supply of the chip as well as DC blocks are not depicted. The synthesizer used in this configuration is a HP83650A and the spectrum analyzer is a HP8565EC, both from Agilent. The hybrids are used to provide differential signals to the circuit. Prior to the measurement, the attenuation of the hybrids, the probes, the DC blocks, and the RF cables must be determined at the signal frequency. The compression point is measured at a signal frequency of 40 GHz which is the maximum frequency of the hybrids and the probes. The output power was measured by the spectrum analyzer as well as by a power meter.

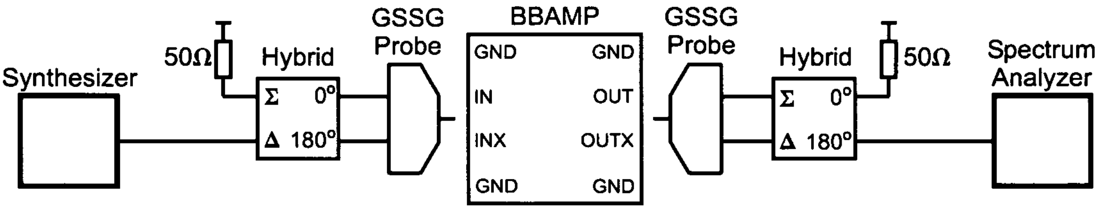


Figure 3.17: Setup for compression point measurement

In Fig. 3.18 the 1-dB compression point of the amplifier is shown. It results to −9.5 dBm referred to the input and +4.8 dBm referred to the output, measured at a signal frequency of 40 GHz.

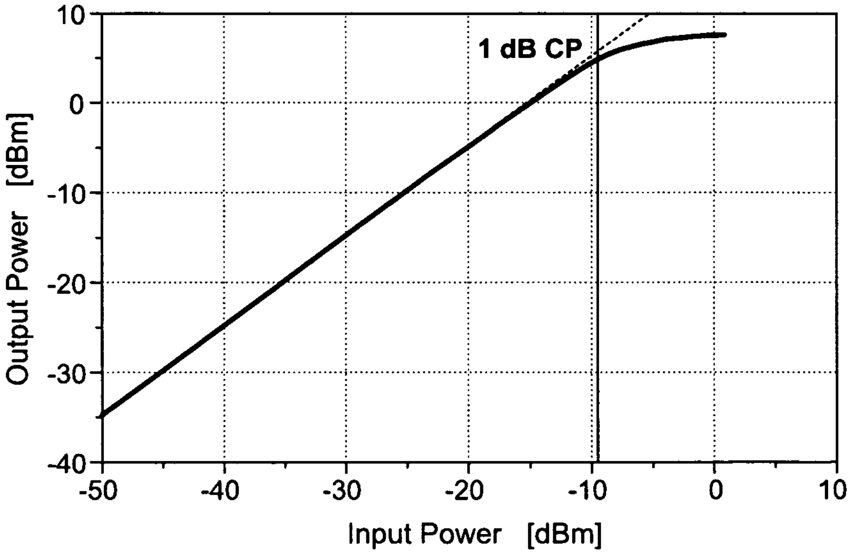


Figure 3.18: Differential on-wafer measurement of the 1-dB compression point (input frequency: 40 GHz)

3.5.3 Two-Tone Third-Order Intermodulation

The setup for intermodulation measurements is shown in Fig. 3.19. It is similar to the 1-dB compression point measurement except that two signals with equal amplitudes are applied to the circuit via a 3-dB power combiner. The attenuation of the components must be evaluated before the measurement again.

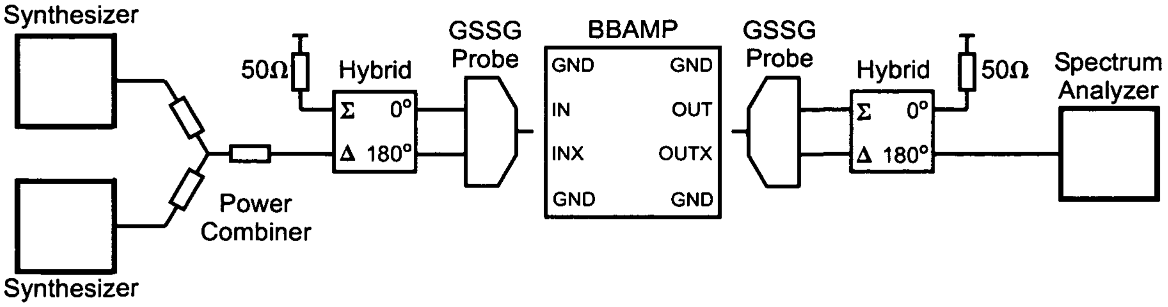


Figure 3.19: Setup for IP3-measurement

Figure 3.20 shows the third-order intermodulation for a two-tone excitation with input frequencies of 40 GHz and 40.002 GHz. The third-order intercept point is +2.1 dBm referred to the input and +17.1 dBm referred to the output.

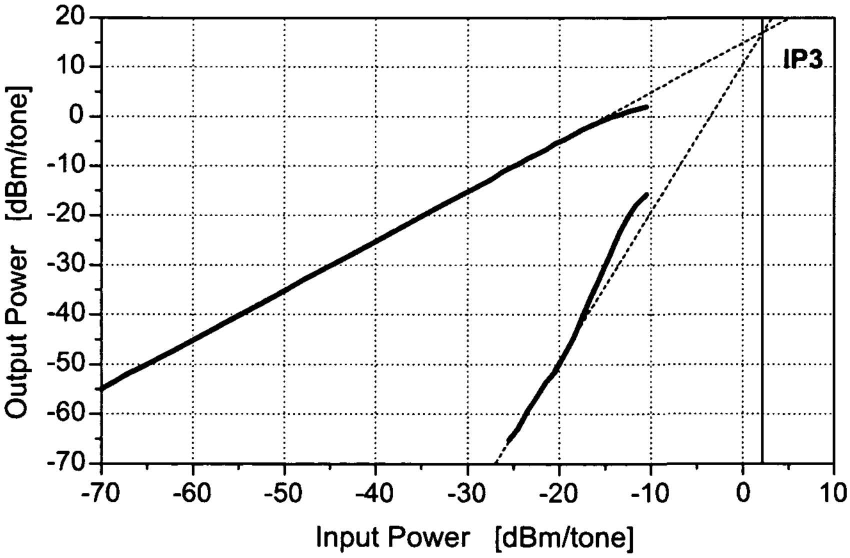


Figure 3.20: Differential on-wafer measurement of the third-order intercept point (input frequencies: 40 GHz and 40.002 GHz)

3.5.4 High Data Rate Signals

Further measurements have been performed by excitation with high data rate signals. The data signal is generated by a pseudo-random-bit-sequence (PRBS) generator chip [Knapp 04]. The PRBS generator is capable of operating at data rates up to 100 Gbit/s. So the broadband amplifier is tested at the maximum available data rate.

Figure 3.21 illustrates the measurement setup for this measurement. The PRBS generator requires a clock signal at half the output data rate. This signal is provided by the synthesizer via a hybrid and the GSSG probe. An amplifier is used in order to ensure sufficient signal level at the clock input. A trigger output provides a trigger signal which is synchronous with the start of a new PRBS cycle. The oscilloscope triggers on this signal when measuring the bit pattern. In case of measuring eye diagrams, the precision time base of the oscilloscope is used in order to reduce the time jitter of the measurement setup. Therefore the clock signal is also provided to the precision time base of the digital sampling oscilloscope.

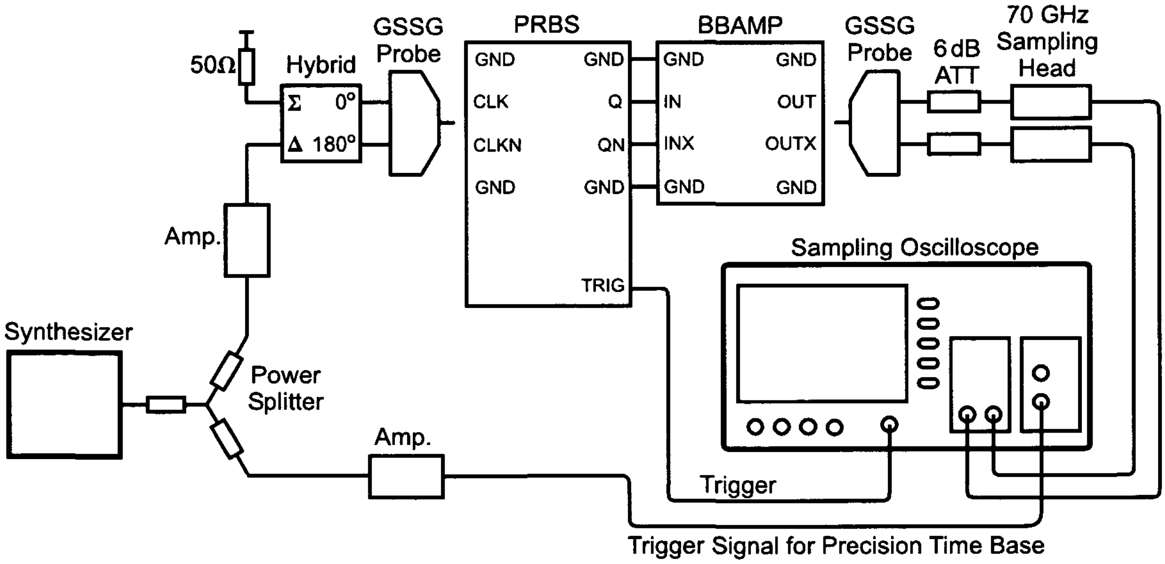


Figure 3.21: Measurement setup for high data rate signals

The PRBS generator chip and the broadband amplifier chip have been mounted closely on a substrate, as shown in Fig. 3.22. Short bond wires connect the outputs of the PRBS generator and the inputs of the amplifier in order to prohibit signal distortion. At the output of the amplifier the voltage is measured via a GSSG probe. An attenuation of 6 dB is required in order to prevent the oscilloscope from saturation.

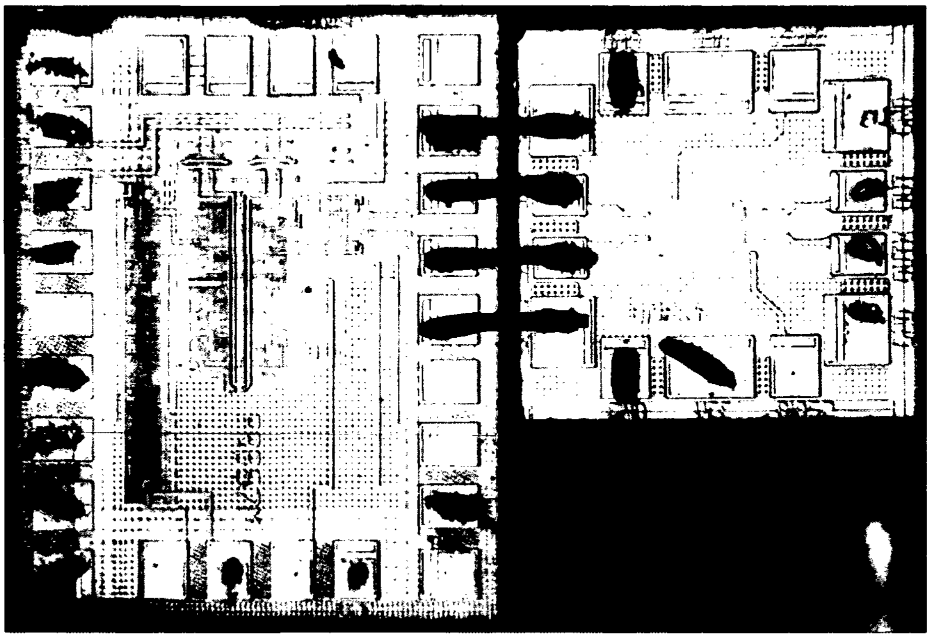


Figure 3.22: Photograph of the arrangement of the PRBS and the amplifier chip

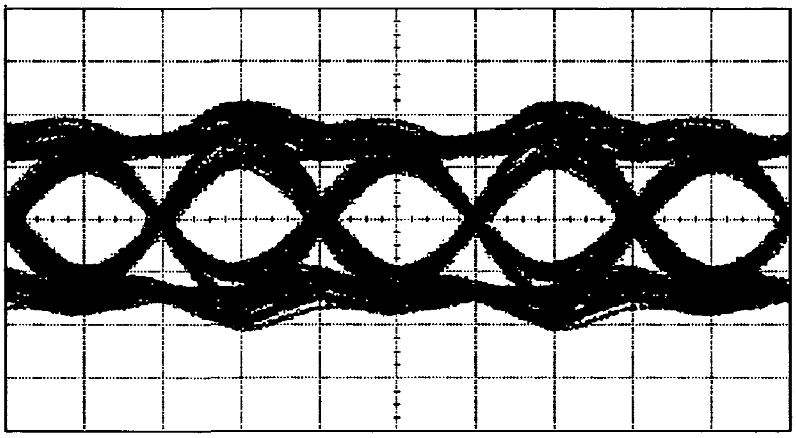


Figure 3.23: Measured output eye diagram of the $2^7 - 1$ PRBS generator at 100 Gbit/s (100 mV/div, 5 ps/div) [Knapp 04]

80 Gbit/s Data Signal

Figure 3.24 shows the differential 80 Gbit/s output eye diagram of the amplifier. The amplitude is 2×750 mV$_{PP}$ and the eye opening is about 1 V$_{PP}$. In Fig. 3.25 the bit pattern of the same signal is shown. The amplitude of the input signal is about 2×150 mV$_{PP}$. So the large signal gain for this measurement is about 14 dB which means that the amplifier is slightly in the limiting mode.

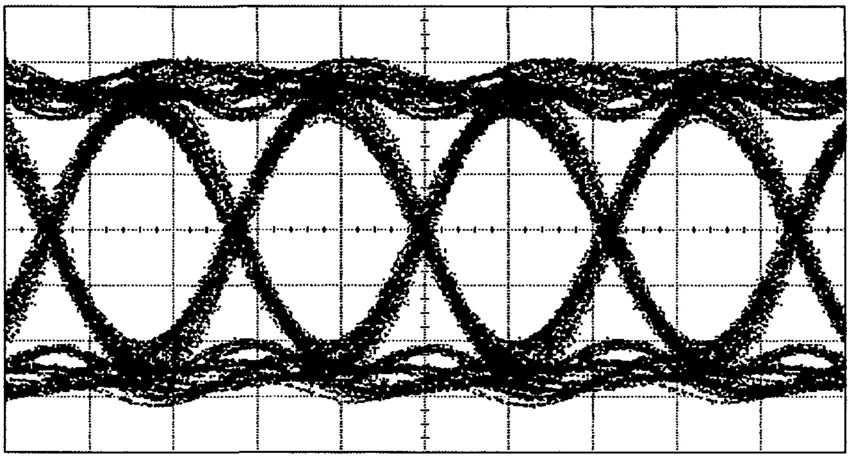


Figure 3.24: Measured 80 Gbit/s differential output eye diagram (250 mV/div, 5.6 ps/div)

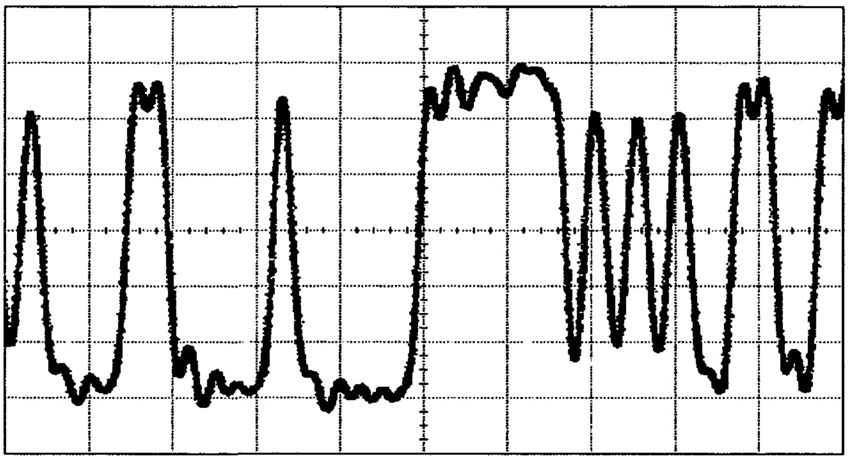


Figure 3.25: Measured 80 Gbit/s differential output signal (250 mV/div, 50 ps/div)

100 Gbit/s Data Signal

In Fig. 3.26 and Fig. 3.27 the output eye diagram and the output bit pattern for a 100 Gbit/s excitation signal are shown. At this data rate the eye opening is 680 mV$_{PP}$. The degradation of the eye diagram is caused by both the limited bandwidth of the measurement equipment, the bandwidth of the broadband amplifier as well as a degraded input signal, see Fig. 3.23. The bandwidth of our differential probes is only 40 GHz.

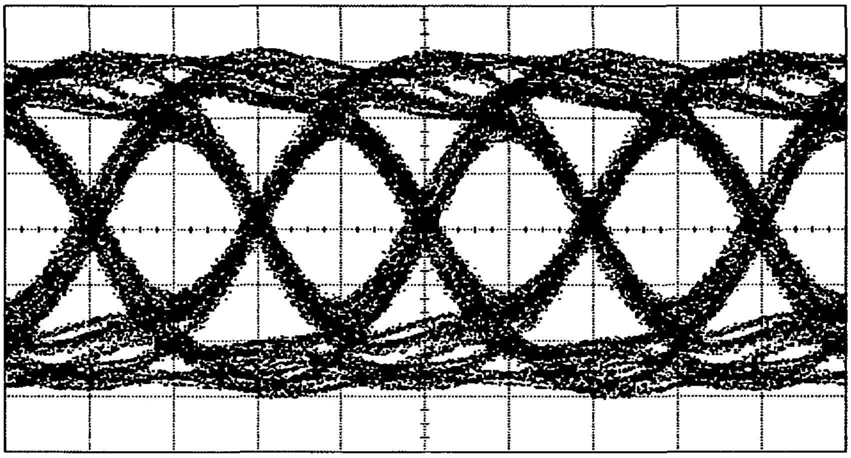


Figure 3.26: Measured 100 Gbit/s differential output eye diagram (250 mV/div, 5 ps/div)

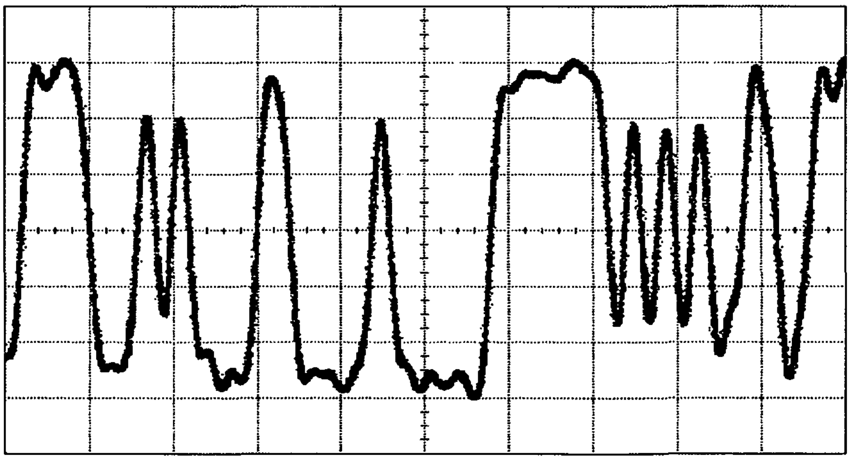


Figure 3.27: Measured 100 Gbit/s differential output signal (250 mV/div, 50 ps/div)

3.6 Summary

In this work a broadband amplifier for versatile fields of applications is presented. The circuit topology is based on a differential amplifier with emitter followers in front of it. By careful optimization of the circuit, a flat frequency response and a high 3-dB bandwidth is achieved.

The circuit exhibits 16 dB gain, a bandwidth of 62 GHz and it consumes 155 mA at a supply voltage of −5 V. The 1-dB compression point is −9.5 dBm and the third-order intercept point is +2.1 dBm, both referred to the input. With this chip, clear output eye diagrams at 100 Gbit/s are demonstrated for analog building blocks the first time. In comparison with state-of-the-art broadband amplifiers based on lumped elements in Table 3.1 the circuit of this work exhibits the highest bandwidth for circuits fabricated in silicon-based technologies. The demonstrated output data signal at 100 Gbit/s shows by far the highest bit rate for all yet published broadband amplifiers. Because of the versatility of this circuit and the outstanding results, there is quite high interest on this chip from developers of measurement equipment as well as from other departments of Infineon for experimental setups.

Technical data of the chip is summarized in Tab. 3.4.

Technology	200 GHz f_T SiGe bipolar
Supply voltage	−5.0 V
Supply current	155 mA
Differential gain	16 dB
3-dB bandwidth	62 GHz
1-dB compression point	−9.5 dBm (in) / +4.8 dBm (out)
Third-order intercept point	+2.1 dBm (in) / +17.1 dBm (out)
Chip size	550 μm × 550 μm

Table 3.4: Summary of technical data

Chapter 4

An Active Mixer for 77 GHz Applications

In this chapter the design of a fully monolithic integrated active mixer for automotive radar applications at 76 GHz to 81 GHz is presented. The mixer consists of an active mixer core based on the Gilbert cell and a new type of on-chip balun at the RF input in order to provide a single-ended input. At first a target application of the mixer is introduced. Then an overview of state-of-the-art integrated microwave mixers and their most important characteristics are given. Further, different types of mixers are discussed and the design of the mixer is presented. Finally the measurement procedure and the results are provided and discussed.

4.1 Introduction

Radio frequency communication systems become more and more important. Right now, mobile telephony, wireless local area networks (WLAN) and the global positioning system (GPS) are standard applications for many people. Mixers which operate at radio frequency (RF) are essential components of all such communication systems. Very high frequency applications like wireless LANs at 60 GHz and radar systems around 77 GHz can be realized up to now only in expensive III-V technologies. Recent advances in SiGe bipolar technologies have stimulated research activities to investigate the use of silicon-based circuits for emerging applications in these frequency bands. A common application in the future could be automotive distance radar, if the system costs can be reduced significantly.

In Fig. 4.1 a block diagram of an automotive radar system based on the FMCW principle is shown. The transmitter of the radar system consists of a voltage controlled oscillator (VCO), a prescaler, a power amplifier, and the transmit (TX) antenna. The VCO and

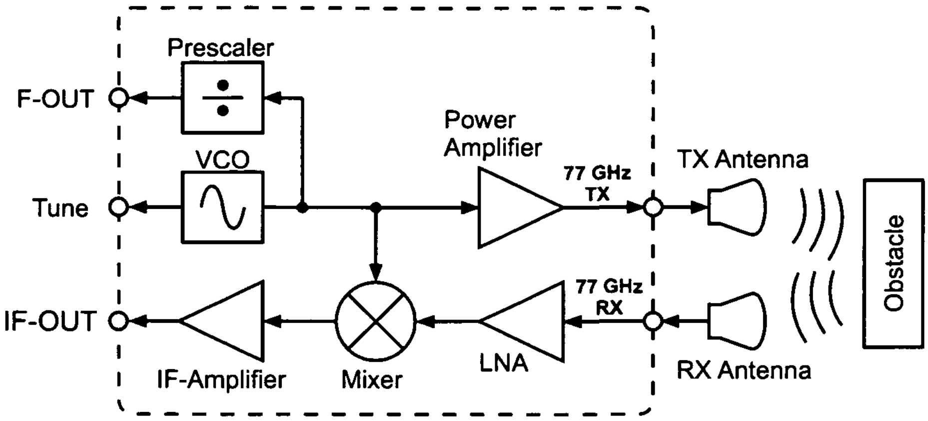


Figure 4.1: Simplified block diagram of the FMCW-Radar

the prescaler are required in order to build a phase-locked-loop (PLL), which generates the transmit signal. The frequency of the transmitted signal has to be changed either according to a sawtooth-ramp or according to a triangle, as shown in Fig. 4.2. The power amplifier in the transmit path is required in order to provide a high output power which is necessary for long range radars.

At the receiver, at first a low-noise amplifier (LNA) is used to amplify the RF signal to reduce the noise contribution from subsequent building blocks. In the down-conversion mixer the received signal from the LNA is mixed with the transmit signal. The intermediate frequency (IF) is the difference of the transmitted and the received signal frequency. In Fig. 4.2 the transmitted and the received signal are depicted. In the lower part of Fig. 4.2 the IF of the system is shown in the case of a relative movement between radar and obstacle. Due to the frequency sweep and the propagation delay of the wave, the

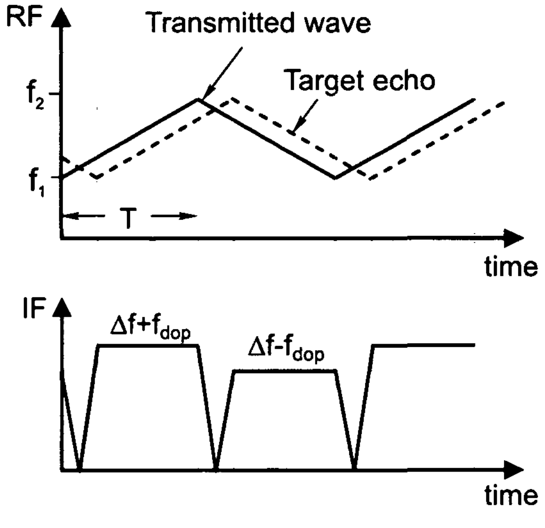


Figure 4.2: Waveform of radar signals and FMCW-principle

difference-frequency Δf which equals the IF corresponds to the distance of the detected obstacle according to:

$$\Delta f = \frac{f_2 - f_1}{T} \cdot \frac{2d}{c} \tag{4.1}$$

where $(f_2 - f_1)/T$ denotes the slope of the frequency sweep, c is speed of light and d is the distance of the obstacle from the radar system. In the case of relative movement between radar and obstacle, doppler shift f_{dop} occurs according to

$$f_{dop} = \frac{2 \cdot v_r}{\lambda} \tag{4.2}$$

where v_r denotes the relative speed between radar and obstacle and λ is the wavelength.

The performance of the radar system mainly depends on the analog building blocks like the VCO, power amplifier, LNA, and the mixer. A prescaler manufactured in SiGe which exceeds the target frequency range is already presented in [Knapp 03]. VCOs suitable for the transmitter of automotive radar systems at 77 GHz have been presented in [Li 04] as well as in Chapter 5. However, no receiver building blocks in SiGe for this application have been reported so far. The down-conversion mixer is a very important building block because its performance affects the system performance as well as the requirements of its adjacent building blocks like the LNA.

The aim of this work is the development of an active down-conversion mixer in SiGe bipolar technology for microwave frequencies around 77 GHz. Key design aspects are low noise figure and high conversion gain in the target frequency range of 76 GHz to 81 GHz. For FMCW radar applications, good noise performance at low IF is essential.

4.1.1 State of the Art

Mixers at microwave frequencies are either realized as passive or active mixers. A passive diode ring-mixer with Si-Schottky diodes, for example, exhibits a conversion loss of 10 dB and a SSB noise figure of 18 dB at an IF frequency of 100 kHz [Siweris 00]. A single balanced diode mixer fabricated in a MESFET technology exhibits a conversion loss of 6 dB and a double-sideband noise (DSB) figure of 7 dB at an RF frequency of 94 GHz [Dieudonne 92]. A state of the art GaAs HEMT mixer is presented in [Siweris 03] which exhibits a conversion loss below 11 dB and SSB noise figure of 20 dB at 1 MHz intermediate frequency.

An active V-band mixer in InP HEMT with a gain of 5 dB and a SSB noise figure of 11.5 dB at a frequency range from 61 GHz to 71 GHz is presented in [Schefer 97]. An active down-conversion mixer up to 40 GHz in a silicon-based technology is presented in [Hackl 02] with a gain of 25 dB and a DSB noise figure of 15 dB. A 60 GHz transceiver in SiGe bipolar technology is presented in [Reynolds 04]. The mixer of this transceiver shows a gain of 18.6 dB and a noise figure of 13.3 dB at 60 GHz.

In Tab. 4.1 an overview of state-of-the-art down-conversion mixers is given. In the upper part passive mixers, and in the lower part of the table active mixers are listed. In Section 4.6 the results of this work are compared with state-of-the-art mixers.

Reference	measured conversion gain [dB]	measured frequency range [GHz]	measured SSB noise figure [1] [dB]	Technology
[Dieudonne 92]	−6	94	7	GaAs MESFET
[Saito 93]	−4.3	60	5.3	GaAs HEMT
[Siweris 00]	−10	76-77	18	Si Shottky diode
[Siweris 03]	−11	76-77	20	GaAs HEMT
[Maas 86a]	0	43.5-45.5	8	GaAs HEMT
[Chow 91]	2.4	94	7.3	InP HEMT
[Schefer 97]	5	61-71	11.5	InP HEMT
[Kawakami 98]	8.2	50	—	GaAs-HEMT
[Wurzer 00]	5.9	DC-30	13.2	SiGe HBT
[Hackl 02]	25	12-42	19	SiGe HBT
[Lynch 03]	12	17	14.5	SiGe BiCMOS
[Bao 03]	2	23	13	SiGe BiCMOS
[Kobayashi 03]	12	0-40	—	InP HBT
[Reynolds 04]	16	61.5	14.8	SiGe HBT

Table 4.1: Comparison of state-of-the-art integrated microwave mixers

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[1] If only the DSB noise figure is mentioned in the publication, the SSB noise figure of this table is calculated by adding 3 dB.

4.1.2 Specification of Circuit Parameters

The aim of this work is to develop a down-conversion mixer for automotive radar systems at 77 GHz. At first, the technical feasibility in silicon-based technologies should be analyzed. Next to the optimization of technical characteristics, also aspects like reliability and production costs should be considered in order to enable mass production in a further development stage. The most important requirements of the down-conversion mixer are:

1. Conversion gain
   The mixer should provide a high conversion gain in order to reduce noise contribution of the IF stage. But on the other hand the gain should not be too high as then small input signals may saturate the mixer.

2. Frequency Range = 76 GHz - 81 GHz:
   The mixer is intended for automotive radar systems. The frequency range from 76 GHz to 77 GHz is provided for long-range radar. A frequency band around 79 GHz is specified for short-range radar. So the target frequency range of the mixer is set to 76 GHz to 81 GHz.

3. SSB Noise Figure:
   A low noise figure of the mixer is required in order to relax the gain requirements of the LNA. If the system does not contain an LNA, the noise figure of the mixer directly sets the sensitivity of the system. For FMCW radar systems as shown in Fig. 4.1 especially good noise performance at low IF is essential.

4. Linearity:
   In a frequency modulation system like the FMCW radar, signal distortion due to gain compression does not influence the transmission quality. However, a strong undesired signal can overload the mixer and cause gain compression of the small desired signal unless the mixer exhibits a high 1-dB compression point.

5. Single-ended high-frequency inputs with 50 Ω matching:
   The received signal from the antenna is usually single-ended. So the RF input is required as a single-ended input. The realization of the LO input depends on the VCO of the system. But in order to ease the measurements, also the LO input should be provided single-ended. 50 Ω matching of the microwave frequency inputs is required.

6. Supply Voltage:
   A negative supply voltage of $-5\,\mathrm{V}$ is chosen.

4.2 Fundamental Mixer Characteristics

4.2.1 Mixer Topologies

Mixers can be classified regarding to different criteria. One possibility of classification is to subdivide mixers into passive and active mixers. Passive mixers [Maas 86b], like diode mixers and resistive mixers, have no conversion gain but usually they achieve a higher linearity and higher speed. Active mixers instead, generally provide gain which reduces noise contributions of subsequent stages.

Active and passive mixers can be categorized in either unbalanced, single-balanced, or double-balanced topology [Fong 99]. In the following an overview of active mixer topologies is given.

Unbalanced Mixers

The simplest circuit among active mixers is the unbalanced mixer, shown in Fig. 4.3. The mixing operation is performed by modulating the transconductance of the transistor by the LO signal. LO and RF signal are applied to the base of the mixing transistor via the LO and the RF filter, respectively. Additive mixing is performed by the nonlinear transfer characteristic of the transistor.

Unbalanced mixers do not reject RF-IF and LO-IF, nor LO-RF feedthrough. The LO signal is injected into the RF port through the RF filter. In the case of low IF, LO and RF frequency are similar. So LO-RF rejection becomes difficult since high-order filters would be required.

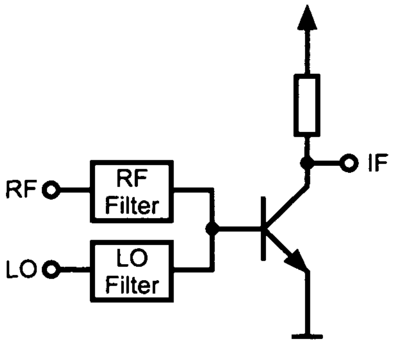


Figure 4.3: Unbalanced active mixer

Single-Balanced Mixers

Figure 4.4 shows the circuit topology of a single-balanced active mixer. It consists of a common-emitter amplifier and a switching pair. Multiplicative mixing is performed by the switching pair which should switch instantaneously from one to the other transistor. Therefore a high LO power level is required. A low LO power causes degradation of the gain and noise figure. The single-balanced mixer rejects RF-IF and LO-to-RF, but not LO-IF feedthrough.

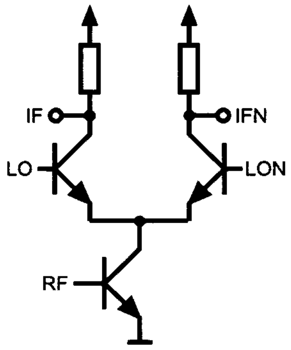


Figure 4.4: Single-balanced active mixer

Double-Balanced Mixers

Figure 4.5 shows the circuit topology of a double-balanced active mixer. The mixer consists of a differential amplifier and a switching quad. In the differential amplifier the RF signal is amplified in order to reduce the influence of signal degradation due to the switching process. The switching quad performs the mixing process. The LO-IF and RF-IF feedthrough are prohibited due to the balanced circuit structure. Also LO-RF feedthrough is rejected if the switching quad is driven differentially.

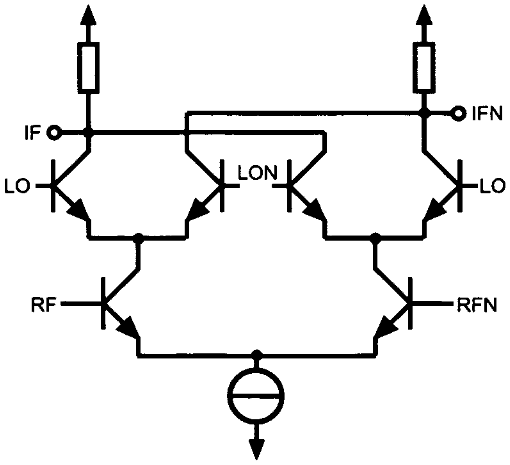


Figure 4.5: Double-balanced active mixer

4.2.2 Performance Parameters

Conversion Gain

The voltage conversion gain of a mixer is defined as the amplitude of the IF signal divided by the amplitude of the RF signal. In this case, signal amplitudes are compared at different frequencies.

The power conversion gain[2] is the IF power delivered to the load divided by the available RF power from the source. If the input and output impedance of the mixer are the same, voltage gain and power gain are equal if expressed in decibel.

The load resistor of integrated mixers is typically not $50\,\Omega$ in order to achieve appropriate conversion gain. At the input matching to $50\,\Omega$ is usually desired. This difference in input and output impedance requires careful notation of gain, noise figure, linearity and so on.

Noise Figure

The noise figure (F) is the signal-to-noise ratio (SNR) at the input divided by the signal-to-noise ratio at the output. The noise figure is indicated either as single-sideband (SSB) noise figure or as double-sideband (DSB) noise figure. The SSB noise figure is used in the case that the desired signal is either in the upper or the lower sideband. This is the case in a heterodyne mixer architecture. In the case of a homodyne architecture, where the signal appears in both sidebands, the DSB noise figure is used.

The noise figure of an amplifier can be expressed as:

$$F = \frac{SNR_{IN}}{SNR_{OUT}} = \frac{kTBG + N_a}{kTBG} \tag{4.3}$$

where k is the Boltzmann constant, T is the source temperature which is usually 290 K, B is the measurement bandwidth, G is the gain of the amplifier, and N_a is the output referred noise power of the circuit. This can be seen as the ratio of the total output noise to the output noise which results only from the input noise.

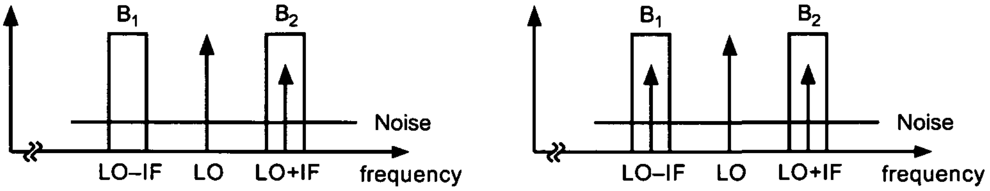
For mixers, SSB and DSB noise figure are defined as follows. In the case that the signal is contained in only one sideband, no image signal is included although noise contributions are included from the desired and the image frequency band. So the definition of the SSB NF is:

---

[2] In the following, the term "gain" or "conversion gain" always corresponds to "power conversion gain".

$$F_{SSB} = \frac{kTB_1G_1 + kTB_2G_2 + N_a}{kTB_2G_2} \tag{4.4}$$

where B_1 and G_1 denote bandwidth and gain at the lower sideband. B_2 and G_2 denote bandwidth and gain at the upper sideband. The corresponding spectrum can be seen in Fig. 4.6(a).



(a) SSB-Input (b) DSB-Input

Figure 4.6: Input spectrum for SSB and DSB mixer

If the signal appears in both the lower and the upper sideband, the DSB noise figure is defined as:

$$F_{DSB} = \frac{kTB_1G_1 + kTB_2G_2 + N_a}{kTB_1G_1 + kTB_2G_2} \tag{4.5}$$

The spectrum in this case is shown in Fig. 4.6(b). The relation between F_{SSB} and F_{DSB} can be derived as:

$$F_{SSB} = F_{DSB}\left(1 + \frac{G_1}{G_2}\right) \tag{4.6}$$

For equal bandwidth and conversion gain in the upper and the lower sideband, SSB noise figure is twice the DSB noise figure, which equals in logarithmic notation: $F_{SSB} = F_{DSB} + 3\,dB$. This is especially valid in the case of low IF and high LO frequency.

Gain Compression

Gain compression is a measure of the maximum RF input signal level for which the mixer provides linear operation. The 1-dB compression point is a measure for the input power level that causes the mixer to deviate from its linear magnitude response by 1 dB. Above this level additional increases in input level do not result in equal increases in output level.

DC Offset

DC offset is a measure of the unbalance of the mixer. For an ideal mixer, no DC offset at the IF output occurs. The DC offset is the DC voltage at the IF output if only the LO signal is applied and the RF input is terminated by 50 Ω.

Port-to-Port Isolation

Isolation is the amount of leakage between the mixer ports. The LO-IF and the RF-IF leakage are the amount the LO and RF input power levels are attenuated towards the IF port. The LO-RF leakage is the attenuation from the LO port towards the RF port. Normally only the LO isolation is specified because the RF power is much lower than the LO power. The required isolation levels depend on the environment in which the mixer is used. LO-IF feedthrough results in LO leakage to the LNA or the antenna. LO-IF and RF-IF feedthrough are critical because these signal levels may saturate the following stage.

4.3 Circuit Design

The mixer presented in this work consists of a mixer core and a microstrip on-chip balun at the RF input in order to provide a single-ended input. In addition, the chip contains LO and IF buffers. A block diagram of the mixer is shown in Fig. 4.7.

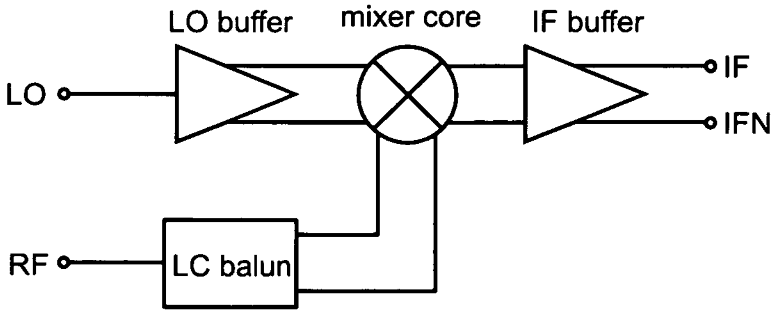


Figure 4.7: Simplified block diagram of the mixer

The mixer core is based on the Gilbert-mixer [Gilbert 00]. It has a double-balanced structure and utilizes differential LO and RF signals. The differential signals required for LO and RF inputs of the mixer core are generated by the LO buffer and the LC balun, respectively. The LO buffer consists of a differential amplifier. The LC balun is based on passive components, converts the balanced to an unbalanced signal and provides an impedance transformation for 50 Ω matching at the RF input. The IF buffer provides impedance matching at the IF output.

4.3.1 LO buffer

The LO buffer (Fig. 4.8) consists of a differential amplifier which provides a differential output signal from the single-ended input. Due to the reduced common-mode rejection ratio (CMRR) of the differential amplifier and the low output resistance of the tail current source in the target frequency range, AC coupling is used in order to prevent a DC offset at the LO input of the mixer core. Emitter followers provide a low impedance interface to the switching quad. Additionally the LO buffer acts as a limiting amplifier to provide a constant LO signal amplitude for the mixer core. A 50 Ω on-chip resistor is used in order to provide matching at the LO input. The LO buffer including the emitter followers draws about 34 mA.

The load resistors of the differential amplifier are 50 Ω. The subsequent high-pass filter is realized with a MIM capacitor of 0.65 pF and a 500 Ω resistor. The tail current of the differential amplifier is 7.5 mA. So the LO swing is limited to a maximum of 680 mV$_{PP}$.

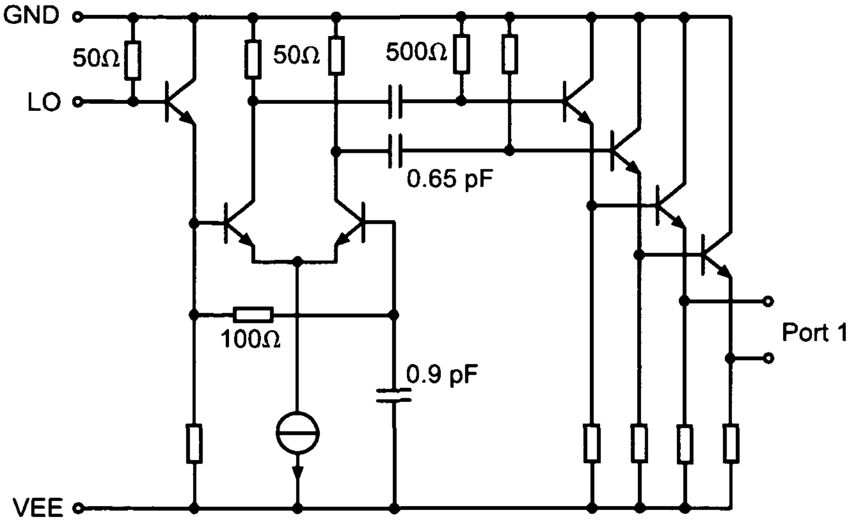


Figure 4.8: Circuit diagram of the LO buffer

4.3.2 Mixer Core

The mixer core is shown in Fig. 4.9. Transistor sizes and bias currents are optimized in order to obtain a good compromise between gain, linearity, and low noise figure. The size of the switching transistors is designed at the current density for maximum f_T. To reduce the noise contribution of the RF transistors, a double base transistor with large emitter contact length is used because of its small base resistance. Shot noise of the base current $\overline{i_B^2}$ and the collector current $\overline{i_C^2}$ as well as thermal noise of the base resistance $\overline{v_B^2}$ of the HBT can be calculated as:

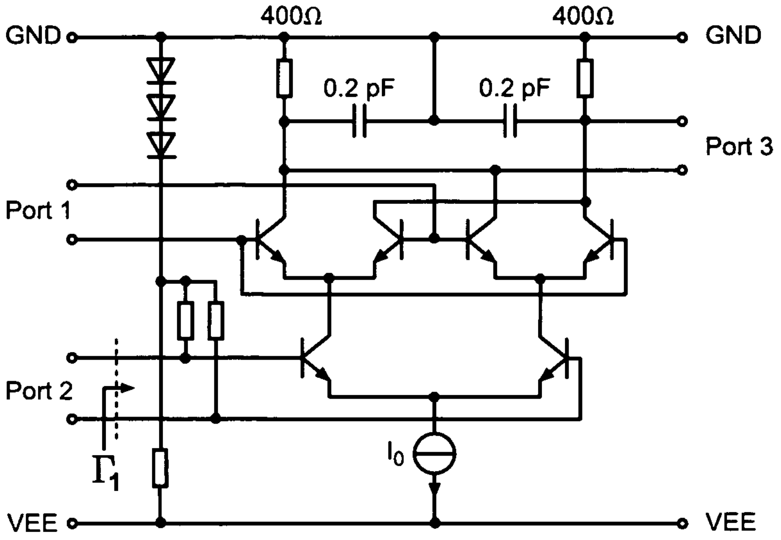


Figure 4.9: Mixer core, based on the Gilbert mixer (GND = 0 V, VEE = −5 V)

$$\overline{i_B^2} = 2qI_B\Delta f \tag{4.7}$$

$$\overline{i_C^2} = 2qI_C\Delta f \tag{4.8}$$

$$\overline{v_B^2} = 4kTr_{bb'}\Delta f \tag{4.9}$$

where q is the electronic charge, Δf is the bandwidth, I_B is the base current, I_C is the collector current, k is Boltzmann's constant, T is the absolute temperature, and $r_{bb'}$ is the base resistance.

The input referred noise of a transistor amplifier in common-emitter configuration due to noise contributions from $\overline{i_B^2}$, $\overline{i_C^2}$, and $\overline{v_B^2}$ is shown in Fig. 4.10. Noise due to the collector

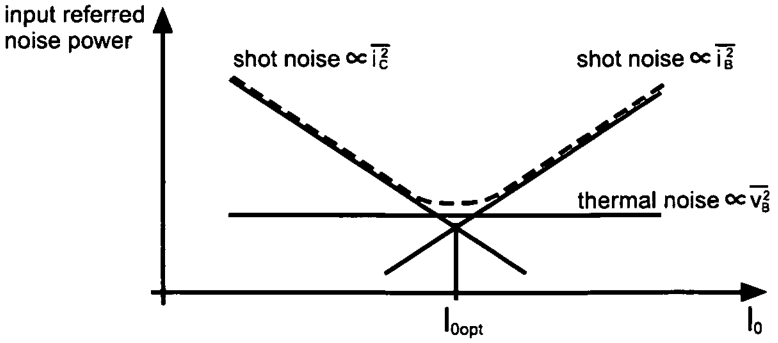


Figure 4.10: Input referred noise power of a transistor amplifier in common-emitter configuration or a differential amplifier depending on the bias current [Gilbert 00]

shot noise $\overline{i_C^2}$ decreases with bias current, while the input referred noise due to the base shot noise $\overline{i_B^2}$ increases with bias current, see Fig. 4.10. The thermal noise due to the base resistance $\overline{v_B^2}$ is constant. The bias current is chosen in order to yield as low noise at the input as possible. So the noise optimum is at the bias current where input referred noise resulting from the base current and collector current are equal.

In order to improve LO-IF isolation and RF-IF isolation an on-chip low-pass filter is used in front of the IF buffer. The load resistors of the Gilbert cell are 400 Ω. The capacitor of the low-pass filter is 0.2 pF, which results in a cutoff frequency of 2 GHz.

DC levels are set by the emitter followers of the LO buffer and the diode bias circuit at the RF input. The Gilbert cell draws only 5 mA and the diode bias circuit draws 4 mA. The differential reflection coefficient at the base of the RF transistors is indicated as Γ_1. This impedance is converted to an unbalanced signal with an input impedance of 50 Ω by the LC LC balun. Due to the load resistors of 400 Ω an LO buffer is required in order to provide a 100 Ω differential output resistance.

4.3.3 LC balun

At the RF input of the mixer, passive components are used for signal conversion in order to keep noise contributions at a minimum. Therefore impedance transformation is done with transmission lines and the balanced to unbalanced transformation is achieved with a passive LC balun [Vizmuller 95]. A general schematic of a lumped-element LC balun is shown in Fig. 4.11.

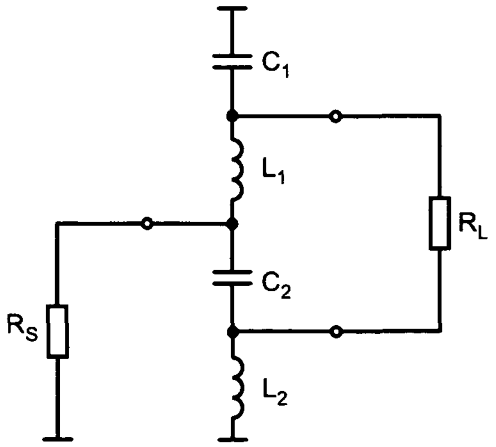


Figure 4.11: General schematic of a lumped-element LC balun

This circuit provides a 180° phase difference and equal amplitude at the two terminals of the symmetrical port. Additionally impedance transformation is performed. R_L is the balanced, symmetrical load resistance and R_S is the grounded, unbalanced source resistance. In order to provide matching at the balanced and the unbalanced port, L

and C values have to be dimensioned as

$$L_1 = L_2 = \frac{Z}{\omega} \tag{4.10}$$

$$C_1 = C_2 = \frac{1}{\omega Z} \tag{4.11}$$

where $Z = \sqrt{R_S \cdot R_L}$ is the characteristic impedance of the balun and ω corresponds to the operation frequency f according to $\omega = 2\pi f$.

For integrated on-chip realization, the inductances can be realized as microstrip lines. Transmission lines with a real or virtual short at the end correspond to an effective inductance according to

$$L = \frac{Z_0}{2\pi f} \tan\left(\frac{2\pi l}{\lambda}\right) \tag{4.12}$$

if $l \leq \lambda/4$. In (4.12), l denotes the length of the line, λ is the wavelength, Z_0 is the characteristic impedance, and f is the frequency. At a given inductance L, a thick dielectric layer between the ground and the signal of the microstrip line, which causes a higher Z_0, is required in order to reduce the line length and so the parasitic series resistance of the line.

In Fig. 4.12 a circuit diagram of the balun integrated in this chip is shown. A detailed view of the balun is depicted in Fig. 4.13.

The LC balun consisting of the transmission lines TRL_1 and TRL_2 and the capacitors C_1 and C_2 converts the balanced to an unbalanced signal and provides an impedance

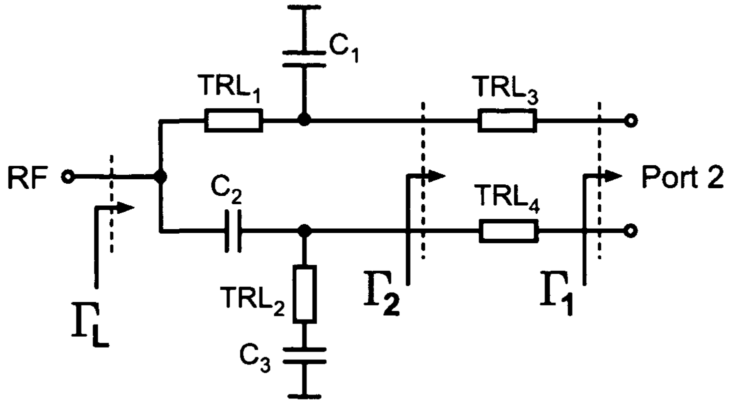


Figure 4.12: Circuit diagram of the LC balun. Transmission lines are drawn as rectangles. TRL_1 and TRL_2 represent inductances L_1 and L_2, TRL_3 and TRL_4 are used for impedance transformation.

Figure 4.13: Detailed view of the LC balun

transformation for 50 Ω matching at the RF input. Capacitor C_3 is required to achieve an RF ground at TRL_2. The balun was designed based on the calculation of a lumped element LC balun. Then the inductances were substituted with transmission lines TRL_1 and TRL_2 [Mongia99]. All transmission lines are realized with the signal line in the fourth and the ground plane in the second metal layer. Capacitances are realized with MIM capacitors. Further optimization was done using a field simulator.

The single-ended input impedance of the RF transistors is simulated to $(54 - j49)\,\Omega$. Transmission lines TRL_3 and TRL_4 are designed in order to transform the impedance of the RF transistors, corresponding to Γ_1, into a real-valued resistance of 33 Ω, corresponding to Γ_2, at the target frequency of 78.5 GHz. This transformation is shown in Fig. 4.14.

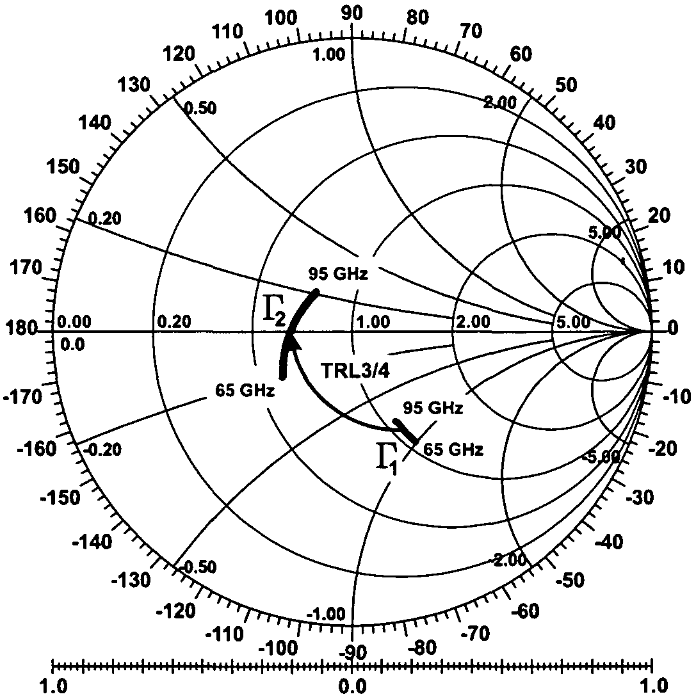


Figure 4.14: Impedance transformation of transmission line TRL_3 and TRL_4. Γ_1 and Γ_2 represent simulated differential reflection coefficients indicated in Fig. 4.9 and Fig. 4.12, normalized to 50 Ω.

4.3.4 IF buffer

The IF buffer, Fig. 4.15, consists of emitter followers and a differential amplifier. The IF buffer is included in order to provide a matched intermediate frequency output and it exhibits a simulated gain of 1.7 dB. So the gain of the complete mixer is dominated by the gain of the mixer core. Due to the high gain of the mixer core the overall noise performance is not affected by the IF buffer. Emitter degeneration is used for linearity improvement. The IF buffer including the emitter followers draws about 17 mA.

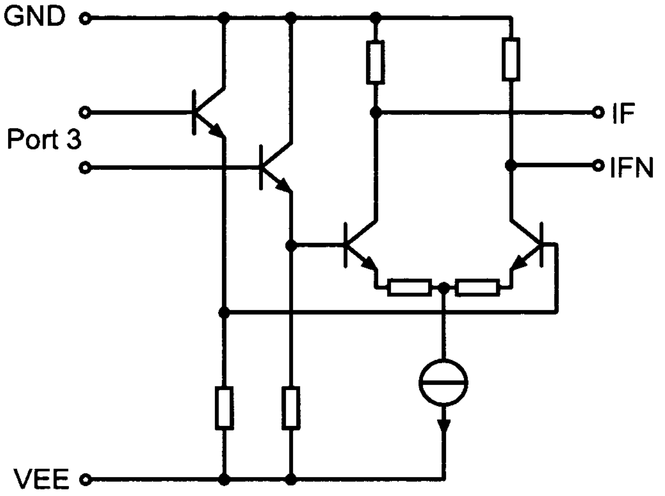


Figure 4.15: IF buffer for providing a 50 Ω match at the IF output

4.4 Layout

Figure 4.16 shows the chip photograph of the mixer. The chip size is 550 μm × 450 μm. Building blocks and important pads are indicated in the photograph. The LC balun is placed directly at the RF input, followed by the mixer core.

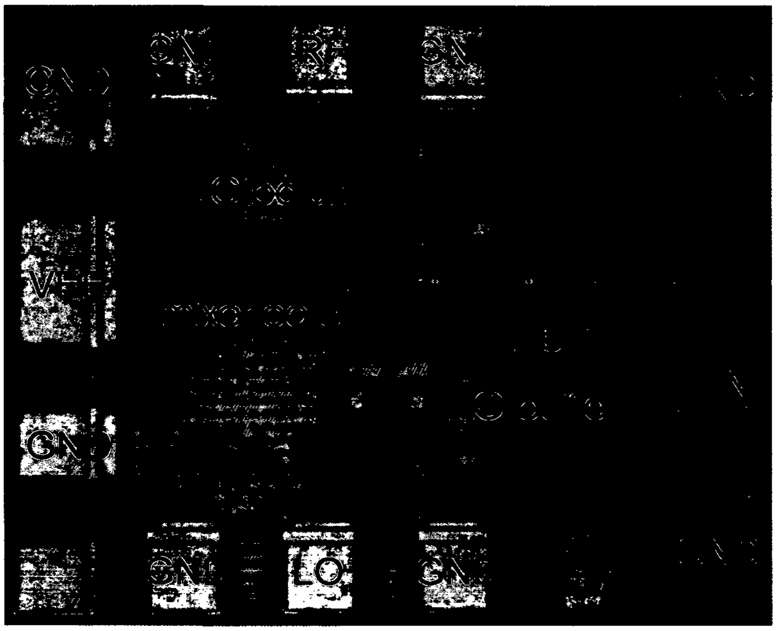


Figure 4.16: Chip photograph of the mixer (chip size: 550 μm × 450 μm)

4.5 Measurement Results

All measurements have been performed on-wafer with an Agilent HP8970 noise figure meter, Agilent mm-wave source modules HP83557A for 50-75 GHz (V-band) and HP83558A for 75-110 GHz (W-band), GGB GS and SG probes for E-band and noise sources from Noisecom for V- and W-band. At the IF output a GGB GSSG probe and a Mini-Circuits power combiner have been used in order to combine the 0°/180° mixer IF outputs to a single unbalanced signal.

The mixer operates at a supply voltage of -5 V with a total current consumption of 60 mA. The mixer core requires only 5 mA.

4.5.1 Y-Factor Method for Noise Figure Measurement

The Y-factor method is a very accurate and common way to measure noise figure and gain of a device concurrently [Agilent 04b]. This measurement method is performed automatically in the noise figure meter HP8970, but it can be performed also manually. A noise source with two different noise power levels is required. Precision noise sources are usually calibrated at a national standards laboratory. Unique calibration information is supplied with noise sources, which is indicated as excess noise ratio (ENR):

$$ENR = \frac{T_h - Tc}{T_0} \tag{4.13}$$

where T_0 is the reference temperature of 290 K and T_h and T_c are calibrated noise levels. The terms "h" and "c" indicate two different noise power levels "hot" and "cold". Usually the ENR is given in decibel, $ENR_{dB} = 10\log(ENR)$. T_c in (4.13) is assumed to be 290 K.

Figure 4.17 shows the noise behavior of a device under test (DUT, either an amplifier or a mixer) in dependence on the noise temperature of the source resistance T_S. N_a is the additional output noise power of the DUT, or in other words, N_a is the output noise power at a source noise temperature of 0 K. N_c is the output noise power at a source noise temperature T_c, and N_h is the output noise power corresponding to a source noise temperature T_h. The output noise power depends linearly on the input noise power or the noise temperature as shown in Fig. 4.17. The slope is kGB, where k is Boltzmann's constant, G is the gain of the system, and B is the noise bandwidth.

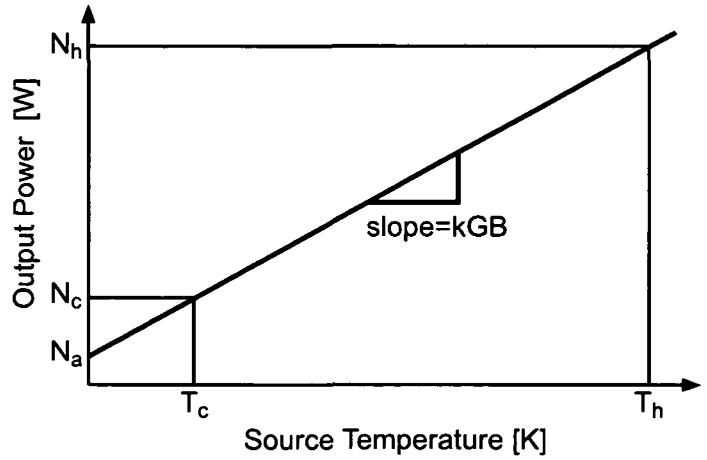


Figure 4.17: Output noise power of an amplifier or a mixer depending on the noise source temperature

The output noise powers N_h and N_c can be calculated as:

$$N_c = kT_cBG + N_a \tag{4.14}$$
$$N_h = kT_hBG + N_a \tag{4.15}$$

The ratio of these two power levels is called the Y-factor:

$$Y = \frac{N_h}{N_c} \tag{4.16}$$

With this, an equation for the internal system noise, N_a can be derived:

$$N_a = kT_0BG\left(\frac{ENR}{Y-1} - 1\right) \tag{4.17}$$

From this the noise figure results in a very simple expression:

$$F_{sys} = 1 + \frac{N_a}{kT_0BG} = \frac{ENR}{Y-1} \tag{4.18}$$

The noise figure F_{sys} from (4.18) includes the noise contribution of the DUT as well as from subsequent systems, e.g. the measurement system. If the gain of the DUT is large ($G_1 \gg F_2$), the noise contribution of the second stage, see Fig. 4.18, can be neglected.

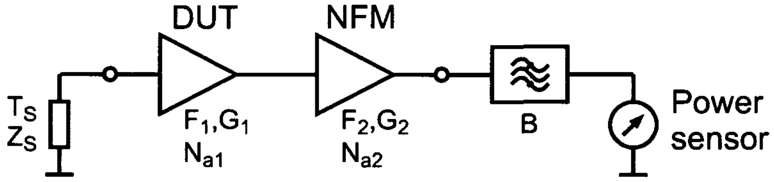


Figure 4.18: General measurement setup for noise figure measurement (DUT=Device Under Test, NFM=Noise Figure Meter)

If the noise figure of the second stage and the gain of the DUT is known the influence of the second stage can be removed, according to [Friis 44]:

$$F_1 = F_{sys} - \frac{F_2 - 1}{G_1} \tag{4.19}$$

The gain of the DUT, G_1, and the measurement system noise figure, F_2, can be determined by system calibration. This is done by connecting at first the noise source directly to the noise figure meter. The measured noise power levels for T_c and T_h result to:

$$N_1 = kT_cG_2B + N_{a2} \tag{4.20}$$
$$N_2 = kT_hG_2B + N_{a2} \tag{4.21}$$

The measurement system noise figure F_2 can be calculated from the noise levels N_2 and N_1 by (4.18). Then the DUT is inserted into the system, like in Fig. 4.18. The noise levels are measured for the noise source temperatures T_c and T_h:

$$\begin{aligned} N_1' &= (kT_cG_1B + N_{a1})G_2 + N_{a2} && (4.22) \\ N_2' &= (kT_hG_1B + N_{a1})G_2 + N_{a2} && (4.23) \end{aligned}$$

The gain of the DUT can be calculated from the noise levels (4.20) to (4.23) as:

$$G_1 = \frac{N_2' - N_1'}{N_2 - N_1} \tag{4.24}$$

The system noise figure F_{sys} can be determined from N_1' and N_2' by applying the Y-factor method. So the noise figure of the DUT, F_1, can be calculated with (4.19).

To achieve accurate and repeatable results with this measurement approach, several sources of error should be prohibited [Agilent 01]:

- A deviation of the actual ENR to the ENR table of the noise source affects directly the measurement result. Therefore the noise source must be calibrated regularly.
- An attenuation before the DUT must be characterized very precisely because every deviation affects directly the measurement result.
- For measuring the 50 Ω noise figure the noise source should exhibit good matching at the "cold" as well as the "hot" state. There exist noise sources with a better match but they exhibit a lower ENR since matching is improved by applying an attenuator.
- The ambient air temperature should be equal to 290 K, otherwise the calculation must be performed with different T_0 and T_c. Usually a small deviation can be neglected.
- The Y-factor method is based on a linear transfer characteristic so the gain of the DUT must not vary.
- If the device under test is a mixer, either SSB noise figure or DSB noise figure is measured. SSB and DSB noise figure are defined in (4.4) and (4.5). In SSB measurement setups, an image rejection filter is required for suppressing the noise power of the unwanted sideband. For DSB noise figure measurement the LO frequency should be as close as possible to the RF band. In this case the SSB noise figure can be calculated in a good approximation as $F_{SSB} = F_{DSB} + 3\,dB$.

In [Agilent 04a] an approach for calculating the uncertainty of the Y-factor method is presented.

4.5.2 Gain and Noise Figure versus LO Frequency

In Fig. 4.19 a block diagram of the setup for gain and noise figure measurement is shown. The supply of the chip as well as DC blocks are not depicted. The synthesizer used in this configuration is a HP83650A with a waveguide frequency extender. The waveguide noise source is connected directly to the waveguide probe. The attenuation of the waveguide probe at the RF input must be determined precisely because this affects directly the measurement result. Also the attenuation of the hybrids, the DC blocks, and the RF cables must be determined in the whole frequency range. The hybrid at the IF output is used in order to combine the differential signals of the circuit. The noise source as well as the synthesizer are controlled by the noise figure meter. With this setup the DSB noise figure is measured. Since LO and RF frequency are very close, the SSB noise figure is calculated as $F_{SSB} = F_{DSB} + 3\,dB$.

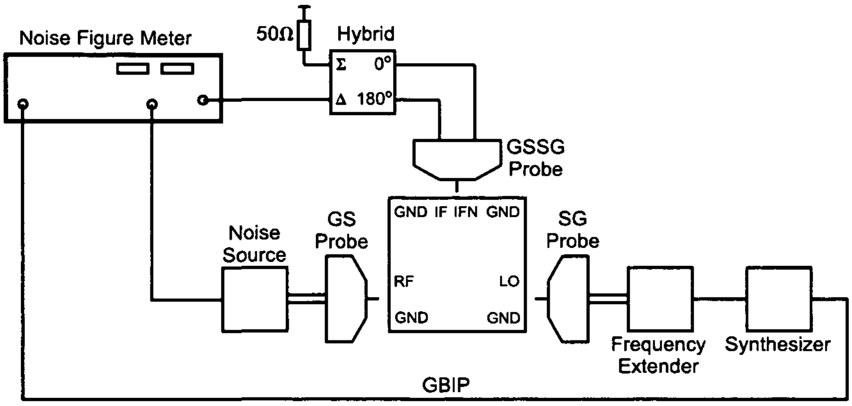


Figure 4.19: Setup for noise figure and gain measurement with the noise figure meter HP8970

In Fig. 4.20 the measured conversion gain and SSB noise figure versus LO frequency of the mixer at a constant IF frequency of 500 MHz are shown. The LO input power is set to 2 dBm at the center frequency. The center frequency of 78.5 GHz is met at the first design. The measured conversion gain is higher than 24 dB and the SSB noise figure is lower than 14 dB in the frequency range from 72.3 GHz to 82.5 GHz. The mismatch of the noise source output and the mixer RF input result in a ripple seen in the measurement plot. The V-band noise source (frequencies below 75 GHz) exhibits a better match than the W-band noise source (frequencies above 75 GHz) which can be seen in a larger ripple at frequencies > 75 GHz. Additionally the return loss at the RF input is shown. At the target frequency the circuit exhibits a return loss of about −9 dB.

4.5.3 Gain and Noise Figure versus LO Power

The setup for this measurement is the same as for the previous measurement, see Fig. 4.19. In this case, a sweep of the LO power at a constant LO frequency is performed.

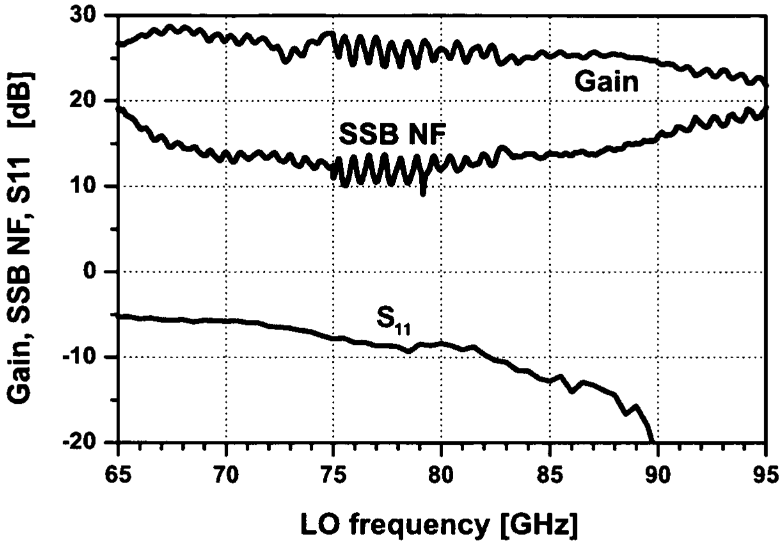


Figure 4.20: Measured conversion gain, SSB noise figure and RF input return loss versus LO frequency. IF frequency is 500 MHz, LO power is 2 dBm.

Figure 4.21 shows the measured conversion gain and SSB noise figure at a fixed IF frequency of 500 MHz and a constant LO frequency of 78.5 GHz as a function of LO power. At lower LO level (<0 dBm) conversion gain and SSB noise figure degrade with decreasing LO power.

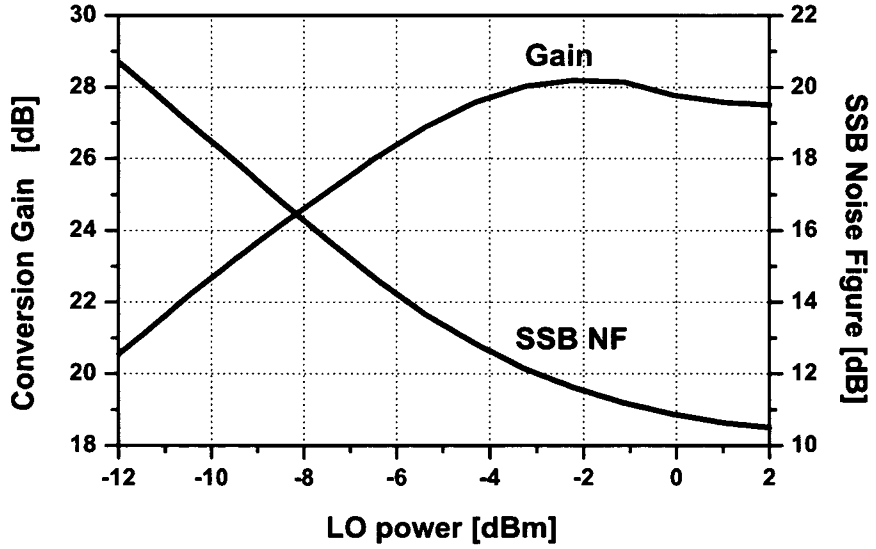


Figure 4.21: Measured conversion gain and SSB noise figure versus LO power. IF frequency is 500 MHz, LO frequency is 78.5 GHz.

4.5.4 Gain and Noise Figure versus IF Frequency

Because of the limited frequency range of the noise figure meter, for low IF frequencies the Y-factor method must be performed manually. The measurement setup is shown in Fig. 4.22. The noise power levels of the "hot" and "cold" noise source are measured with an Agilent spectrum analyzer HP8565EC with appropriate resolution and video bandwidth settings. A low noise amplifier is used in order to improve the measurement system performance.

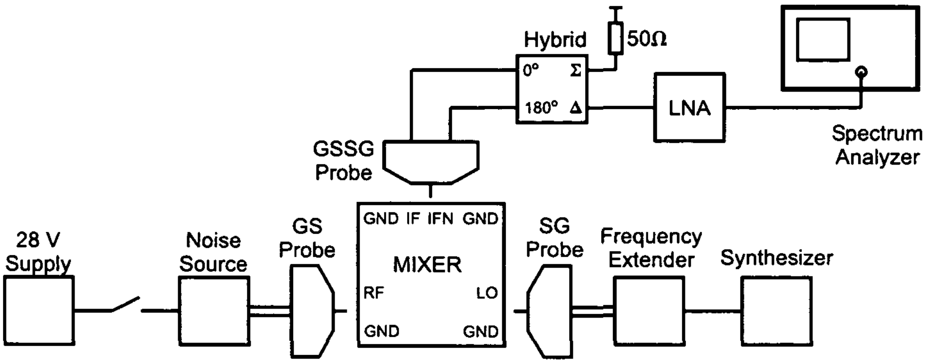


Figure 4.22: Setup for manual noise figure and gain measurement

Figure 4.23 shows the measured conversion gain and SSB noise figure versus IF frequency at a constant LO frequency of 78.5 GHz. The SSB noise figure exhibits a 10 dB per decade slope for frequencies below 10 kHz which results from 1/f noise and the phase noise of the LO signal. For IF frequencies above 10 kHz the SSB noise figure is almost constant. The conversion gain is only a weak function of the IF frequency. Especially for homodyne automotive radar systems, the performance at low intermediate frequencies is of particular importance.

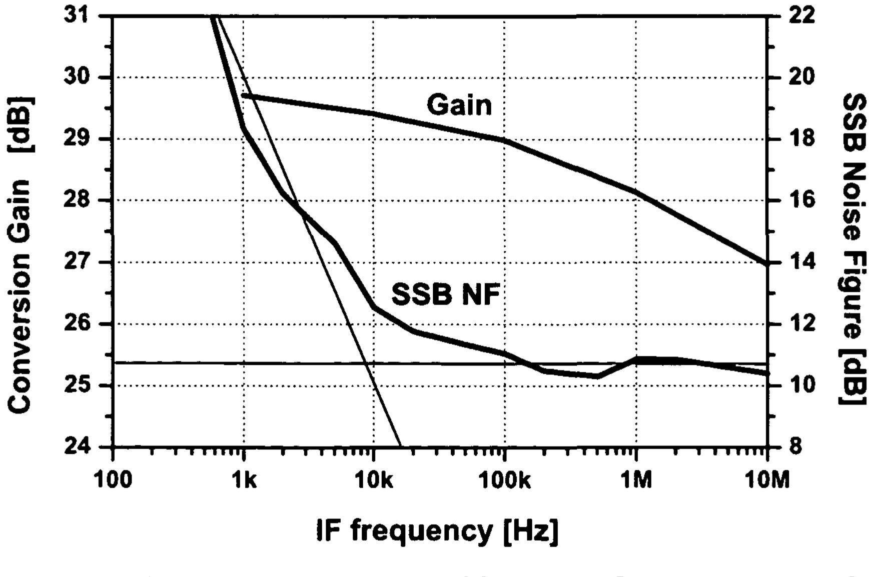


Figure 4.23: Measured conversion gain and SSB noise figure versus IF frequency. LO frequency is 78.5 GHz, LO power is 2 dBm.

4.5.5 Single-Tone Compression Point

Figure 4.24 shows the setup for the 1-dB compression point measurement. Both LO and RF signal are generated by a waveguide frequency extender. The synthesizers use the same reference in order to provide a constant IF. Prior to the measurement, the RF power has been calibrated. The IF power is combined by the hybrid and measured by the spectrum analyzer.

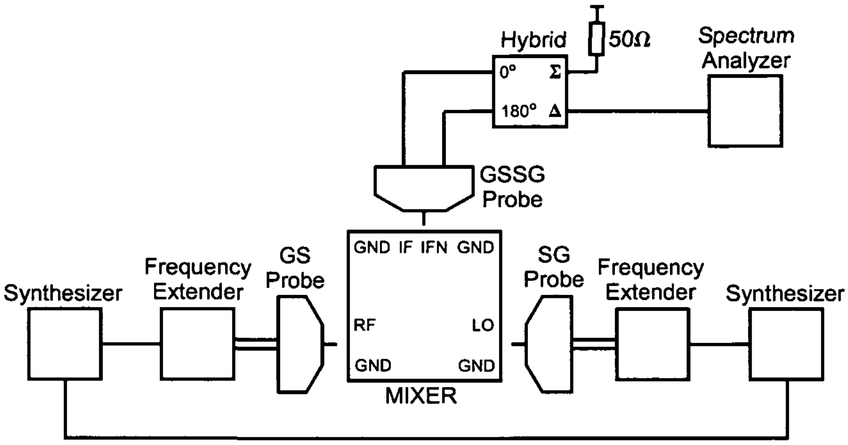


Figure 4.24: Setup for 1-dB compression point measurement

In Fig. 4.25 the measured output power versus input power is shown. The IF frequency is 500 MHz, the LO frequency is 78.5 GHz and the LO power is 2 dBm. The 1 dB compression point is −30 dBm referred to the input and −4 dBm referred to the output. The compression point is dominated by the IF buffer.

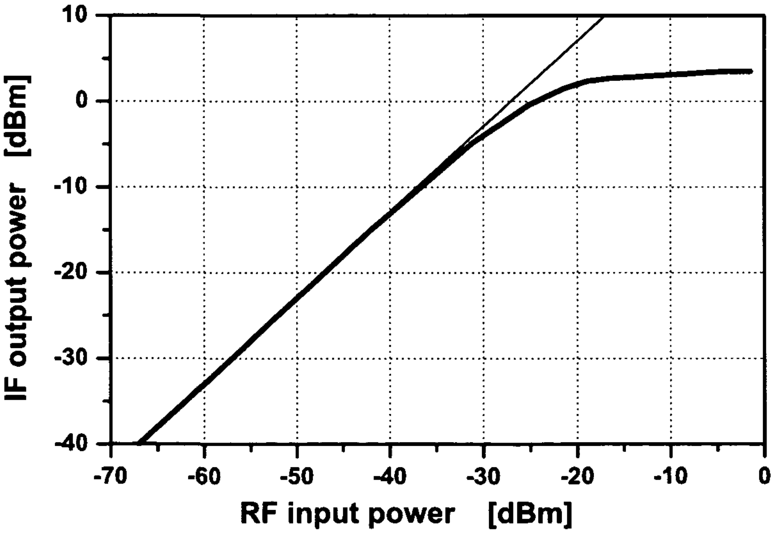


Figure 4.25: Measured IF output power versus RF input power. LO frequency is 78.5 GHz, RF frequency is 79 GHz, IF frequency is 500 MHz, LO power is 2 dBm.

4.5.6 Time-Domain Signal

In this measurement, the IF signal at a frequency of 100 kHz is measured with a digital storage oscilloscope. The setup for this measurement is shown in Fig. 4.26. The outputs were terminated by 50 Ω resistors and the corresponding waveforms were measured with a digital storage oscilloscope.

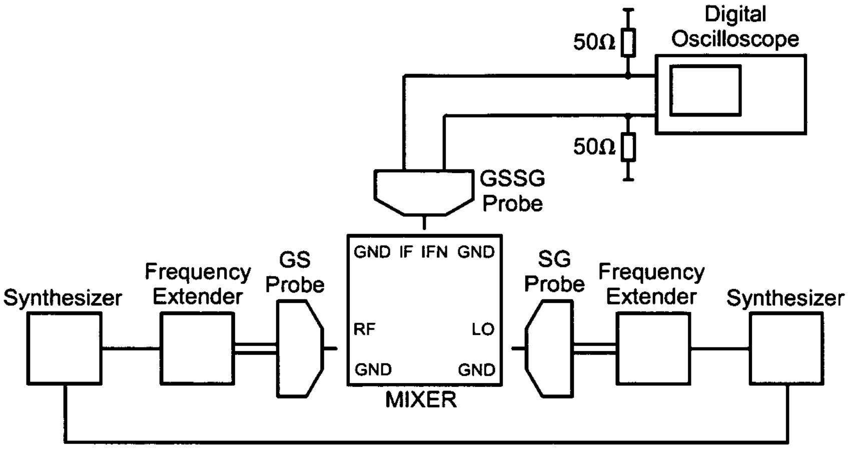


Figure 4.26: Setup for time-domain measurement of the IF output signals

In Fig. 4.27 the oscilloscope display of the measured IF outputs IF and IFN is shown. The IF signals show almost equal amplitudes and near 180 ° phase difference.

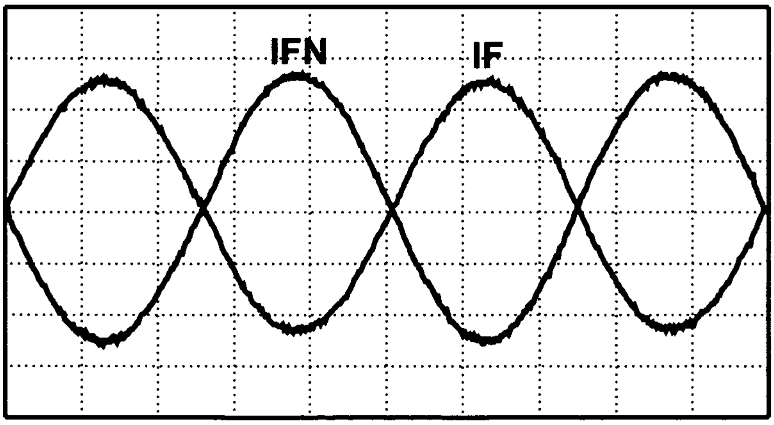


Figure 4.27: Measured waveforms of the IF output IF and IFN. LO frequency is 78.5 GHz, RF frequency is 78.5001 GHz, LO power is 2 dBm, IF frequency is 100 kHz, (10 mV/div, 2 μs/div).

4.5.7 RF Input Reflection

S-parameter measurements have been performed on-wafer using an Anritsu 360B vector network analyzer with frequency extension modules for E-band measurements. In Fig. 4.28 the measured reflection coefficient at the RF input port is shown. The LO port is terminated with 50 Ω during this measurement.

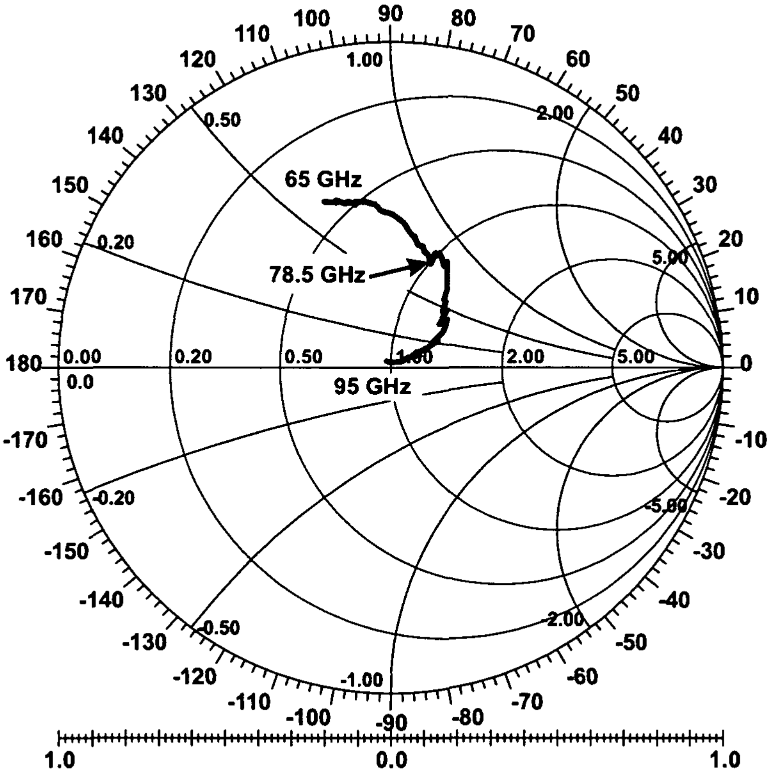


Figure 4.28: Measured reflection coefficient at the RF input port normalized to 50 Ω

4.6 Summary

Table 4.2 summarizes the technical data of the mixer. With this circuit a monolithically integrated active down-conversion mixer for the frequency range from 76 GHz to 81 GHz is demonstrated. The mixer exhibits a gain of more than 24 dB and a low SSB noise figure of less than 14 dB in a frequency range much larger than the target frequency range. In comparison with active state-of-the-art mixers in Table 4.1 fabricated in silicon-based technologies it can be seen that the mixer of this work exhibits the highest RF frequency range and the highest gain at a very low SSB noise figure. A careful optimization of the mixer core as well as the monolithic integration of an LC balun, which is presented the first time in silicon-based technologies, enable such high performance.

Further development of the circuit could be an increase of the 1-dB compression point. This can be done by a redesign of the IF buffer. Because the IF of the intended application is below 1 MHz, the on-chip IF buffer can be omitted and an external IF buffer for enabling measurements can be used. Moreover, the input reflection should be further optimized in order to diminish the dependency of gain and noise figure on the input frequency.

Supply voltage	−5.0 V
Supply current	60 mA
Conversion gain	>24 dB (65.0 GHz - 90.8 GHz) >22 dB (65.0 GHz - 94.9 GHz)
SSB noise figure	<14 dB (72.3 GHz - 82.5 GHz) <16 dB (66.5 GHz - 90.0 GHz)
1 dB comp. point (input/output)	−30 dBm / −4 dBm
Technology	0.18 μm / 200 GHz f_T SiGe bipolar
Chip size	550 μm × 450 μm

Table 4.2: Summary of technical data

Chapter 5

A 98 GHz Voltage Controlled Oscillator

In this chapter a monolithic integrated voltage controlled oscillator (VCO) manufactured in a silicon germanium bipolar technology is presented. The oscillator is optimized for maximum oscillation frequency without neglecting phase noise and output power. At first a short introduction and an overview of state-of-the-art oscillators and VCOs is given. Then the circuit concept, based on the common collector Colpitts oscillator, is presented. Design aspects of the oscillator core and the resonator are discussed. The circuit of this work includes a quarter-wave transformer at the output for impedance transformation, which is a novelty for silicon-based technologies. Furthermore, the layout of the VCO, the measurement procedure, and measurement results are presented.

5.1 Introduction

Voltage-controlled oscillators are key components in almost all communication systems. Already in Chapter 4 applications like distance sensors for automotive and industrial systems are introduced. For these applications frequency bands at 77 GHz and 94 GHz are designated. Up to now, VCOs which operate at these high frequencies are built either with discrete components or they are manufactured in III-V semiconductors. There are several disadvantages of these existing solutions. Discrete oscillators require much space and are expensive to manufacture in mass production. In addition, discrete oscillators usually must be tuned after fabrication to their target frequency. Fully monolithic integrated oscillators, which also include the resonator on chip, are required in order to get around these problems. Up to now, fully integrated oscillators at microwave frequencies are fabricated in III-V semiconductors, due to the much higher intrinsic speed of these materials compared to silicon. Recent advances in the development of SiGe:C technologies enable research of circuits for microwave frequencies in a low-cost silicon-based technology in a highly integrated manner.

5.1.1 State-of-the-Art

The highest frequency fundamental-mode oscillator reported so far operates up to 146 GHz and is fabricated in an InGaP/InGaAs technology with an f_{max} of 170 GHz [Uchida 01]. In silicon-based technologies, VCOs with operation frequencies up to 60 GHz [Winkler 03], 88 GHz [Li 03b], and recently 100 GHz [Franca-Neto 04] and 112 GHz [Steinhauer 04] have been shown so far. An oscillator design up to 50 GHz which exhibits a very low phase noise of −110 dBc/Hz at an offset frequency of 1 MHz has been presented in [Li 03a]. In Tab. 5.1 published fundamental-mode, state-of-the-art, fully integrated oscillators and VCOs are compared. In the upper part of the table, VCOs fabricated in III-V semiconductors are listed. The oscillator in [Uchida 01] is a fixed frequency oscillator. In the lower part of the table, there are silicon-based oscillators.

Reference	measured frequency range [GHz]	measured output power [dBm]	measured SSB noise 1 MHz [dBc/Hz]	Technology
[Bangert 96]	86 - 94	+7.8	−67	GaAs HFET
[Wang 97]	94.5 - 95.0	−3.5	—	InP HBT
[Siweris 99]	75.3 - 77.8	+7.8	−75	GaAs HEMT
[Uchida 01]	147.6	−18.4	−65	GaAs HBT
[Tiebout 02]	50.9 - 51.6	−30	−85	120 nm CMOS
[Shaeffer 03]	40.8 - 45.9	—	−96	SiGe BiCMOS
[Winkler 03]	76.1	−7	−91	SiGe:C BiCMOS
[Winkler 03]	58.7 - 68.5	−17	−84	SiGe:C BiCMOS
[Li 03a]	36 - 46.9	+9	−110	SiGe HBT
[Li 03b]	75.3 - 79.6	+14	−94	SiGe HBT
[Li 03b]	84.3 - 88.4	+10	−90	SiGe HBT
[Franca-Neto 04]	103.9	−65 [a]	−94 [b]	90 nm CMOS
[Steinhauer 04]	104 - 112	0	—	SiGe HBT

[a] including 35 dB conversion loss
[b] at 10 MHz offset frequency

Table 5.1: Comparison of state-of-the-art oscillators and VCOs

5.1.2 Specification of VCO Properties

The aim of this work is to design a voltage-controlled oscillator with an output frequency as high as possible at practically reasonable values of phase noise and output power. This circuit is intended for investigation of oscillator concepts adapted for monolithic integration. The following parameters of the VCO are evaluated during circuit design:

1. Center frequency $>94\,\mathrm{GHz}$:
   The frequency range around 77 GHz and 94 GHz is provided for distance sensor applications. Due to the increasing importance of these systems, it is intended to achieve an output frequency of at least 94 GHz.

2. Tuning range:
   Conventional distance sensor systems are narrow band applications. So the tuning range required for proper operation is usually very small. But in order to compensate for fabrication tolerances, a higher tuning range is required. This design is not optimized in order to obtain a very high tuning range.

3. Output power $>-10\,\mathrm{dBm}$:
   High output power is required for VCOs in a transmitter without power amplifier. In this design an output power of more than $-10\,\mathrm{dBm}$ is the target.

4. Phase noise $<-75\,\mathrm{dBc/Hz}$ at 1 MHz offset:
   Phase noise is a very important parameter especially for VCOs in transmitter and receiver systems. For this VCO, a single-side-band (SSB) phase noise of $-75\,\mathrm{dBc/Hz}$ or less at 1 MHz offset frequency is desired.

5. Supply voltage, tuning voltage:
   A supply voltage of $-5\,\mathrm{V}$ is chosen. The tuning voltage is required to be within ground and the supply voltage.

6. Power consumption:
   Especially for mobile systems, power consumption is an important concern. A low power consumption is desirable.

The VCO of this work is manufactured in a wafer run prior to the technology development stage described in Chapter 2. The transistors offer similar performance: f_T=206 GHz and f_{max}=197 GHz. However the metallization stack of this technology is different. It consists of four aluminium layers with heights of $400\,\mu\mathrm{m}$ at the bottom, two layers with $800\,\mu\mathrm{m}$ in the middle, and $1200\,\mu\mathrm{m}$ at the top layer. Aluminium exhibits a lower conductivity than copper, so there are slightly higher losses in the wiring of this technology. Further, there is no MIM capacitor and no TaN resistor.

5.2 Fundamentals of Oscillator Design

The first step in the design process is to evaluate the most appropriate circuit structure. In integrated high-frequency circuit design predominantly LC oscillators are used for signal generation. Comprehensive classification of LC oscillators can be found in literature [Matthys 83, Zinke 95]. In this work, a Colpitts oscillator is investigated. This circuit is especially suitable for fully integrated circuits because only one inductor is required. Integrated inductors occupy much chip area and they exhibit only moderate quality factors.

Then the circuit structure is analyzed by linear, small signal models before nonlinear simulation tools are applied. With small signal analysis the frequencies which satisfy the oscillation condition are indicated. So the maximum possible oscillation frequency, the desired oscillation signal as well as potential spurious frequencies are determined. With the means of nonlinear, large signal simulation tools the accurate oscillation frequency, phase noise and output power can be evaluated.

5.2.1 Oscillator Model

Oscillators can be analyzed as either an amplifier with positive feedback or as a negative resistance circuit.

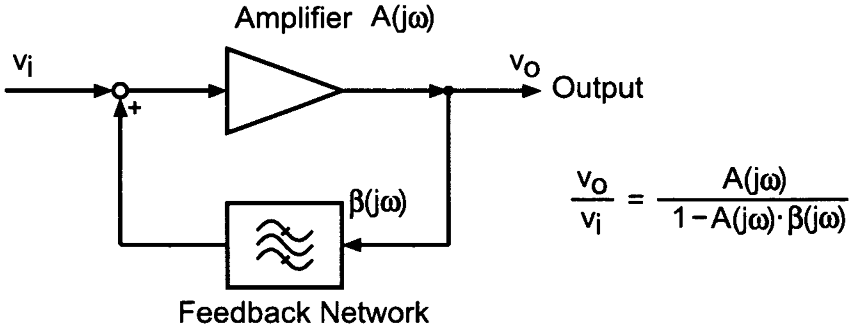


Figure 5.1: Block diagram of a feedback oscillator

Figure 5.1 shows a feedback oscillator model consisting of an amplifier and a feedback network. If the phase shift of the loop is 0, 2π, ... and the open-loop gain equals unity, oscillation is possible. This condition for oscillation is often referred to as Barkhausen criterion:

$$|A(\omega)\cdot\beta(\omega)| = 1 \text{ and } \varphi_A(\omega) + \varphi_\beta(\omega) = 0, 2\pi, \dots , \tag{5.1}$$

where $A(\omega)$ and $\beta(\omega)$ denote the transfer functions of the amplifier and the feedback network, respectively, and φ_A and φ_B give the phases of A and β. In order to guarantee the onset of oscillation the small signal open-loop (voltage) gain of the circuit $|A(\omega)\cdot\beta(\omega)|$ must be greater than unity. In typical RF oscillators a value of 1.4 to 2 (3 dB to 6 dB) is chosen [Rogers 03]. Due to nonlinearities of the amplifier, the gain $A(\omega)$ decreases for higher signal amplitudes, which results in $|A(\omega)\cdot\beta(\omega)| = 1$ for steady-state oscillation.

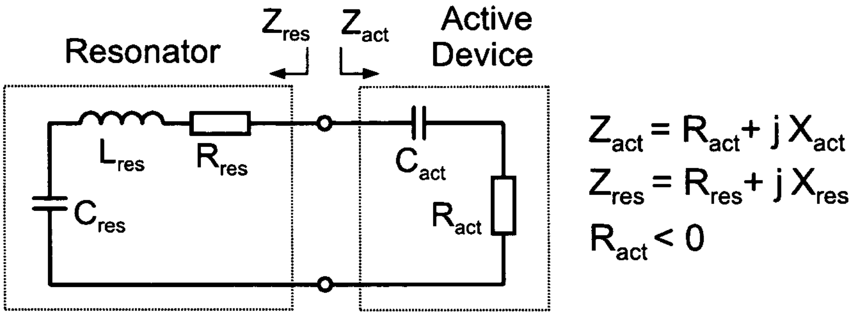


Figure 5.2: Negative impedance model for analyzing oscillators

The linear analysis of the oscillator presented in this work is done using the negative resistance model, shown in Fig. 5.2. This model consists of an active device represented by a negative resistance with a series capacitance. The series-resonator consists of L_{res} and C_{res}. R_{res} models the loss of the resonator. Figure 5.2 equals a series resonant circuit with an exponential decaying oscillation if $R_{act} + R_{res} > 0$ and an exponential growing oscillation if $R_{act}+R_{res} < 0$. The oscillation frequency f_{osc} is set by the resonant frequency of this circuit according to

$$\frac{1}{j\omega_{osc}}\frac{C_{act}+C_{res}}{C_{act}\,C_{res}} + j\omega_{osc}L_{res} = 0\ ,\ f_{osc} = \frac{\omega_{osc}}{2\pi}\,. \tag{5.2}$$

The condition for oscillation is that the negative differential input resistance at least compensates the resonator losses at the oscillation frequency

$$R_{act} + R_{res} < 0 \quad @ \quad f_{osc}\,. \tag{5.3}$$

At start-up of oscillation, the negative resistance of the active device must exceed the resonator losses by about 20% [Vendelin 82]. When steady-state oscillation has built up, large signal effects cause an increase of the negative resistance and the active device exactly compensates the resonator losses, $R_{act} + R_{res} = 0$.

The linear analysis is done by investigation of the impedance $Z = Z_{act} + Z_{res}$. The real part of Z, $Re(Z)$, gives those frequency ranges where oscillation is possible. The zero-crossings of the imaginary part of Z, $Im(Z)$, give the actual oscillation frequencies unless $Re(Z) > 0$ at these frequencies.

5.2.2 Colpitts Oscillator

A simple schematic for realizing negative resistances is given in Fig. 5.3, which represents the active unit of a common-collector Colpitts oscillator. The feedback of the circuit which develops the negative resistance is done by the capacitances C_1 and C_2.

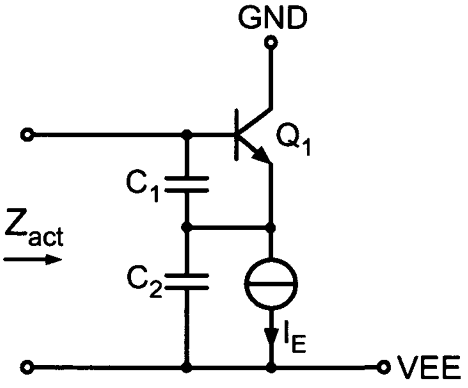


Figure 5.3: Common-collector Colpitts oscillator (active device)

With the assumption of an ideal transistor Q_1 the impedance of the active device Z_{act} in Fig. 5.3 can be calculated as

$$Z_{act} = -\frac{g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}. \tag{5.4}$$

In this calculation, contact resistances $r_{bb'}$, $r_{ee'}$, and $r_{cc'}$ as well as the capacitances c_π and c_μ of the small signal equivalent circuit in Fig. 2.7 are neglected. Additionally $\beta_0 \to \infty$ is assumed. In the case of large values for C_1 and C_2 the parasitics of the transistor are negligible and the approximations are valid. It can be seen that the real part is negative and the reactance equals C_1 and C_2 in series. In order to enable high operation frequencies, C_1 and C_2 must be small. Thus, the oscillation frequency is affected by the parasitics of the transistor. Taking into consideration the parasitics c_π and c_μ of the transistor model, the imaginary part of Z_{act}, which determines the frequency, can be calculated as [Rogers 03]:

$$Im(Z_{act}) \approx \frac{1}{j\omega\left(c_\mu + \frac{(C_1+c_\pi)C_2}{C_1+c_\pi+C_2}\right)}. \tag{5.5}$$

The contact resistances are neglected and $\beta_0 \to \infty$ is assumed in this derivation, again.

5.3 Circuit Design

Figure 5.4 shows the schematic of the voltage controlled oscillator. The VCO is based on the common-collector Colpitts oscillator, as already shown in Fig. 5.3. The active device, on the right hand side, and the resonator, on the left hand side of the figure are indicated. The current source of Fig. 5.3 is replaced by the resistor R_4 and at the collector of Q_1 a low load resistor R_3 and a transmission line TRL_1 towards the output are implemented. The resistors R_1 and R_2 are for biasing.

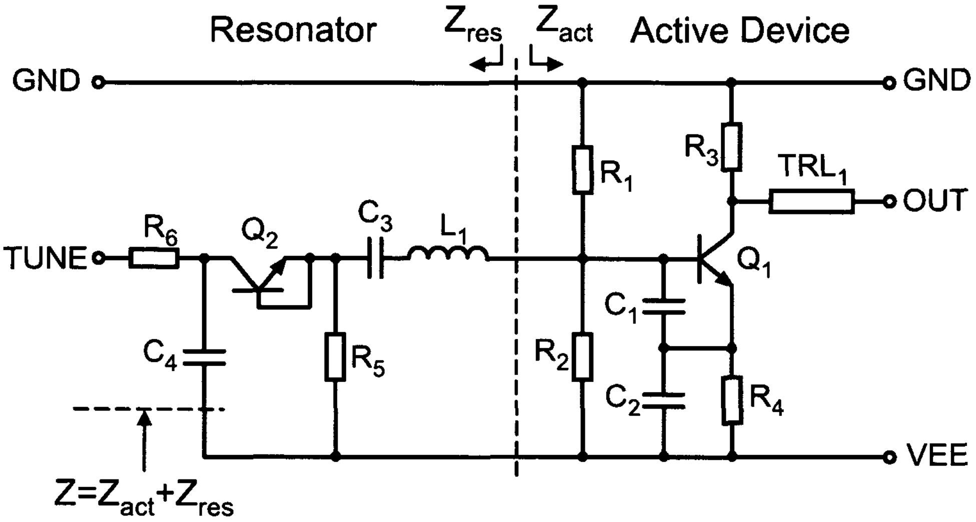


Figure 5.4: Circuit diagram of the 98 GHz VCO

5.3.1 Resonator

The resonator of Fig. 5.4 consists of an inductor L_1, a capacitor C_3 and a diode-connected transistor Q_2. The base-collector capacitance of Q_2 is used as varactor in order to tune the oscillator's frequency. C_4 provides an RF ground at the transistor Q_2. The resistors R_5 and R_6 are for biasing the BC diode.

The inductance of the resonator is designed as a bend in the top metal layer. In Fig. 5.5 a simulation model for monolithic on-chip inductors is shown [Wohlmuth 00]. L_X represents the desired inductance, R_{ALU} characterizes losses in the metallization. Due to the very high frequencies the skin effect is of particular significance for these losses. The skin depth δ is defined as

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{5.6}$$

where ω denotes the angular frequency, μ is the permeability and σ represents the conductivity of the material. The skin depth in aluminium at a frequency of 98 GHz is 0.27 μm.

Further losses result from the conductive silicon substrate. At high frequencies, the substrate acts as a lossy dielectric. This is modeled in the equivalent circuit in Fig. 5.5 as a resistor R_{SUB} and a capacitor C_{SUB} in parallel. The silicon oxide layer which is between the metal layer and the substrate is modeled as capacitance C_{OX}.

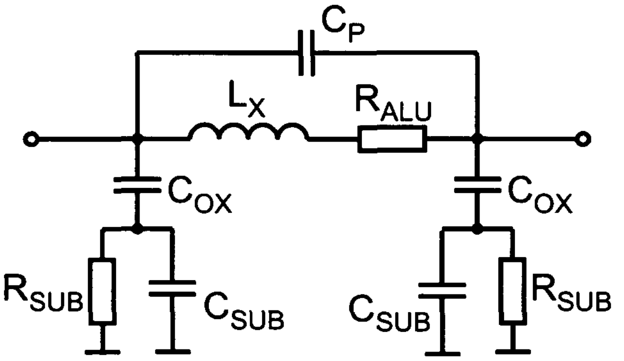


Figure 5.5: Detailed simulation model of monolithic on-chip inductors

The inductor used in this VCO, see Fig. 5.6, consists of half a winding only. This inductor, which looks like a bend, is in total 90 μm long at a width of 7 μm. For an output frequency of 98 GHz the inductance L_1 is modeled as 130 pH.

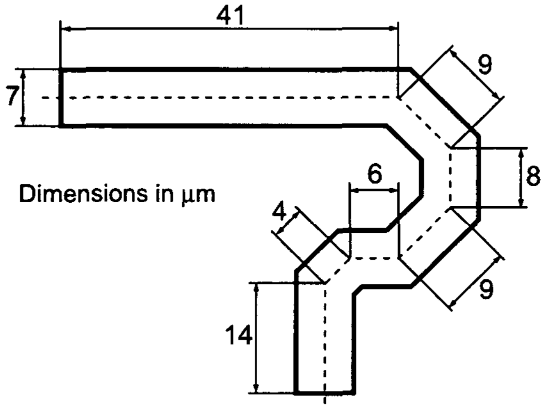


Figure 5.6: Integrated Inductance

The capacitors of the resonator as well as those of the active device, C_1 - C_4, are built of parallel metal layers. The capacitance C of a parallel plate capacitor is calculated by

$$C = \varepsilon \frac{A}{d} \tag{5.7}$$

where ε denotes the permittivity, A is the area of the capacitor, and d is the spacing between the metal layers.

The technology in which this oscillator is manufactured does not provide a varactor. On this account, the depletion capacitance of the BC diode is used in order to tune the frequency of the VCO. The depletion capacitance depends on the forward voltage according to

$$c_j(V) = \frac{C_{J0}}{(1 - V/V_J)^M} , \tag{5.8}$$

see (2.14). The exponent M in this equation depends on the pn-junction. Varactors typically exhibit an M of more than 0.5. But the BC diode is constructed for optimized transistor performance. Therefore the exponent M is about 0.3 which results in a lower capacitance range by variation of the diode voltage. In Fig. 5.7 the capacitance of the BC diode versus tuning voltage is shown. It can be seen that the ratio of the minimum to the maximum capacitance is approximately 1:1.6.

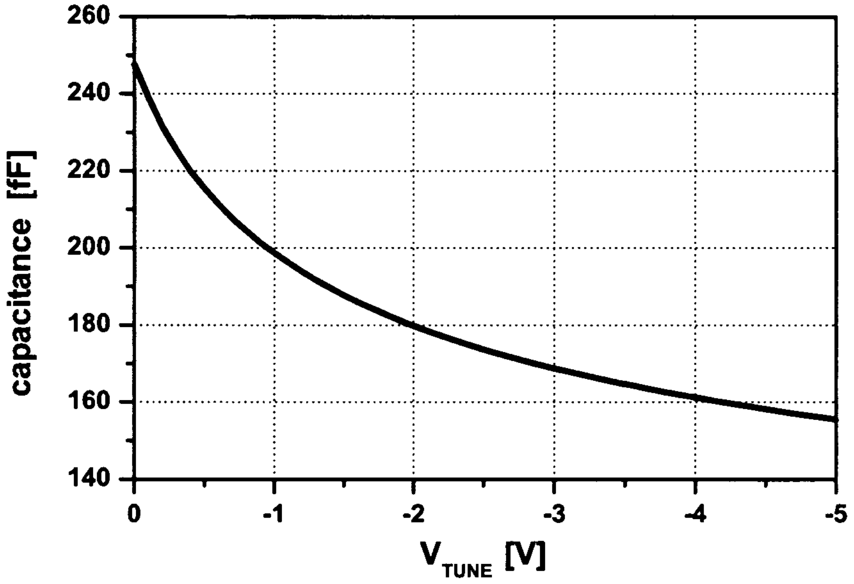


Figure 5.7: Simulated base-collector capacitance C_{BC} of the BC diode of transistor Q_2

5.3.2 Output Matching

A challenge in oscillator design is that the oscillator core must be isolated from the output load. This is important in order to prohibit a decrease of the resonator quality factor due to the output load as well as frequency pulling. Frequency pulling is a measure of the frequency change due to a non-ideal load. Usually a buffer amplifier is used in order to drive the low output impedance. This additional stage adds complexity and increases power consumption. The schematic in Fig. 5.4 gets around this problem by modifying the common-collector Colpitts oscillator in that way that the output is taken from the collector. However the collector should be connected to ground at the operating frequency. Therefore, the transmission line TRL_1 in Fig. 5.4 is used in order to transform the impedance of the output network, comprising the pad capacitance and the 50 Ω impedance of the measurement equipment in parallel, into a low impedance at the collector of Q_1. With this trick, the collector is connected to a reasonable AC ground and the output is taken from the collector, concurrently.

In Fig. 5.8 a cross section of the output transmission line is shown. It is implemented as a grounded coplanar waveguide. The top metal layer is used for the coplanar structure and the second metal layer is used for the ground plane. The simulated characteristic of this structure is an impedance Z_W of 13 Ω, a total attenuation of 0.7 dB and an effective dielectric constant of 3.4 . This transmission line is used as a quarterwave transformer, so the impedance of the measurement system, 50 Ω, is transformed into approximately 4 Ω, according to $Z_W = Z_1 \cdot Z_2$.

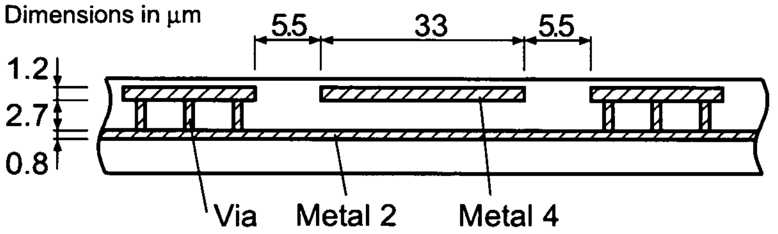


Figure 5.8: Grounded coplanar waveguide at the output of the VCO

5.3.3 Small Signal Design

In this section small signal simulations are used in order to evaluate the impedance of the active device and the resonator $Z = Z_{act} + Z_{res}$ [Rhea 95]. Design tradeoffs and mutual dependencies of circuit parameters are discussed.

C_1 and C_2 constitute the capacitive voltage divider of the Colpitts oscillator. If the capacitors C_1 and C_2 are large, parasitics of the transistor Q_2 will have a negligible effect but the maximum oscillation frequency will be reduced. A high inductance of L_1 results in a better phase noise but also reduces the maximum oscillation frequency. If the capacitor C_3 in the resonator is small, L_1 could be high at a constant resonant frequency, but the tuning range will be narrowed. C_4 should be as large as possible in order to provide an RF ground at the resonator.

Parasitic elements of transistor Q_1 like the base resistance R_B and the base-collector capacitance C_{BC} increase the real part of Z_{act} and therefore reduce the maximum oscillation frequency. Additionally the load of transistor Q_1 increases the negative differential resistance of (5.4). In order to minimize the reduction of the maximum frequency due to the load of Q_1 the grounded coplanar transmission line TRL_1 transforms the impedance of the output network, comprising the pad capacitance and the 50 Ω impedance of the measurement equipment in parallel, into a low impedance at the collector of Q_1. This transformation decreases the negative resistance $Re(Z_{act})$ of the oscillator impedance which enables higher operation frequencies.

In Fig. 5.9 real and imaginary part of the simulated impedance $Z = Z_{act} + Z_{res}$ with and without the transmission line TRL_1 are shown. The maximum possible oscillation frequency is set by the zero-crossing of $Re(Z)$, see (5.3). In Fig. 5.9 it can be seen that oscillation with this configuration is only possible due to the use of transmission line TRL_1. The actual oscillation frequency is set by the zero-crossing of the imaginary part $Im(Z)$, see (5.2). In this frequency range, $Re(Z)$ exhibits a flat minimum.

As an adequate dimensioning, the component parameters result to: $C_1 = 17\,\text{fF}$, $C_2 = 20\,\text{fF}$, $C_3 = 160\,\text{fF}$, $C_4 = 710\,\text{fF}$ and $L_1 = 130\,\text{pH}$. The biasing resistors result to $R_1 = 1.5\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $R_3 = 30\,\Omega$, $R_4 = 400\,\Omega$, $R_5 = 5\,\text{k}\Omega$, and $R_6 = 4\,\text{k}\Omega$. The base-collector capacitance of Q_2 can be set from 155 fF to 250 fF depending on the tuning voltage, see Fig. 5.7. The losses of Q_2 and L_1 are modeled as series resistors with values of $1.7\,\Omega$ and $1.4\,\Omega$, respectively.

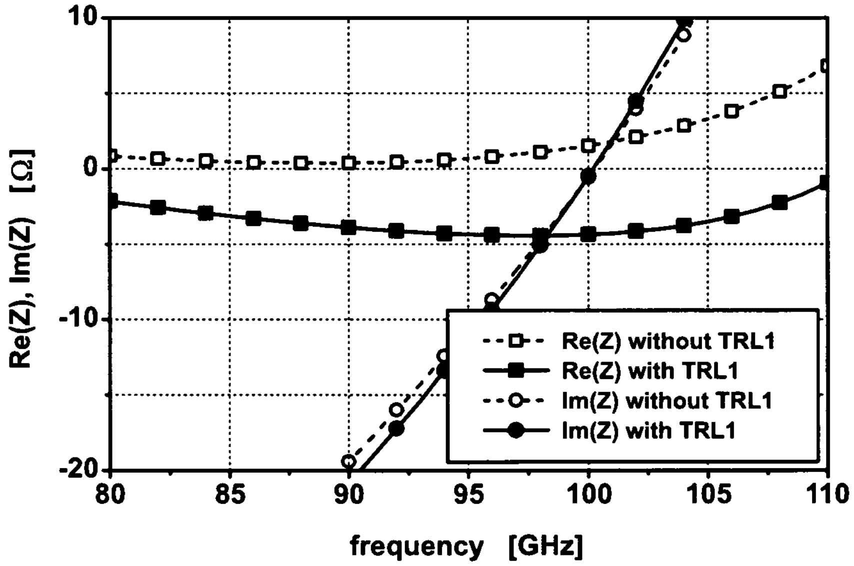


Figure 5.9: Simulated impedance $Z = Z_{act} + Z_{res}$ of the 98 GHz VCO

5.3.4 Large Signal Design

Large signal conditions change the voltage-dependent parameters of the transistor. Therefore the results of the linear approach are used as first design results which have to be further optimized by large signal analysis in order to determine the steady-state frequency of oscillation. As a result of the non-linear simulation, the harmonics of the VCO output signal at a tuning voltage of V_{tune}=0 V are shown in Fig. 5.10. The large signal fundamental frequency of oscillation is simulated to 98.2 GHz, which is in good agreement with the small signal approximation. Further results of the large signal simulation are an output power of −5.1 dBm, and a phase noise performance of −85 dBc/Hz at an offset frequency of 1 MHz from the carrier.

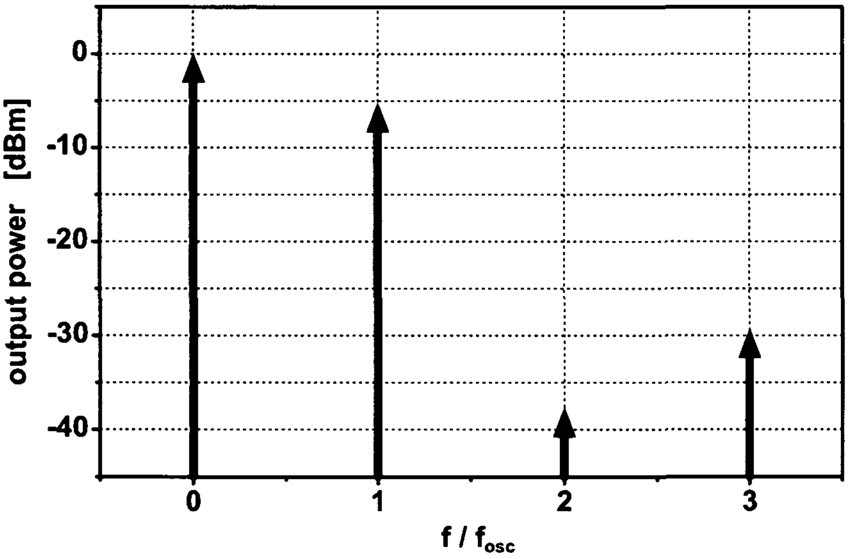


Figure 5.10: Large signal simulation of harmonic content of the VCO output signal (f_{osc}=98.2 GHz)

5.4 Layout

In Fig. 5.11 the chip photograph of VCO is shown. The most important components are indicated in the photograph. The chip size is 550 μm × 450 μm. The components of the active device are placed as close as possible in order to avoid parasitic capacitances and inductances due to complex wiring. The active device of the oscillator requires only a small area of the chip. The resonator, the transmission line at the output TRL_1 as well as the pads consume most of the chip area.

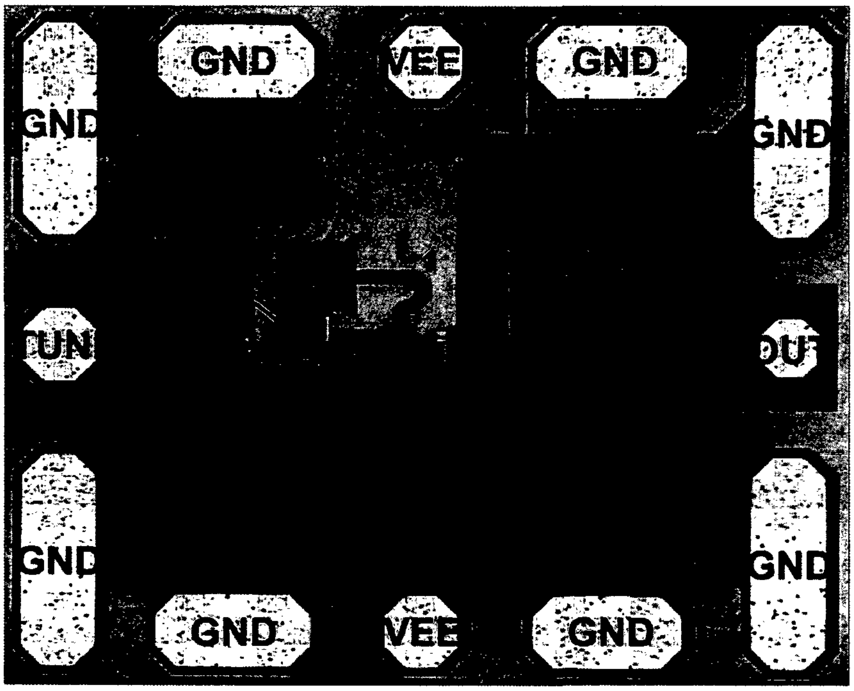


Figure 5.11: Chip photograph of the 98 GHz VCO (chip size: 550 μm × 450 μm)

5.5 Measurement Results

The measurements have been performed on-wafer with an Agilent 8565EC spectrum analyzer, an Agilent 11970W harmonic mixer (75-110 GHz), a GGB 120 GHz GSG microwave probe and a Millitech fullband isolator connected with straight waveguide sections. A photograph and a schematic diagram of the measurement setup are shown in Fig. 5.12. Due to the losses in the microwave probe and the isolator there is an attenuation of at least 3 dB in the considered frequency band.

The oscillators operate with a supply voltage of −5 V. This leads to a total current consumption of 12 mA.

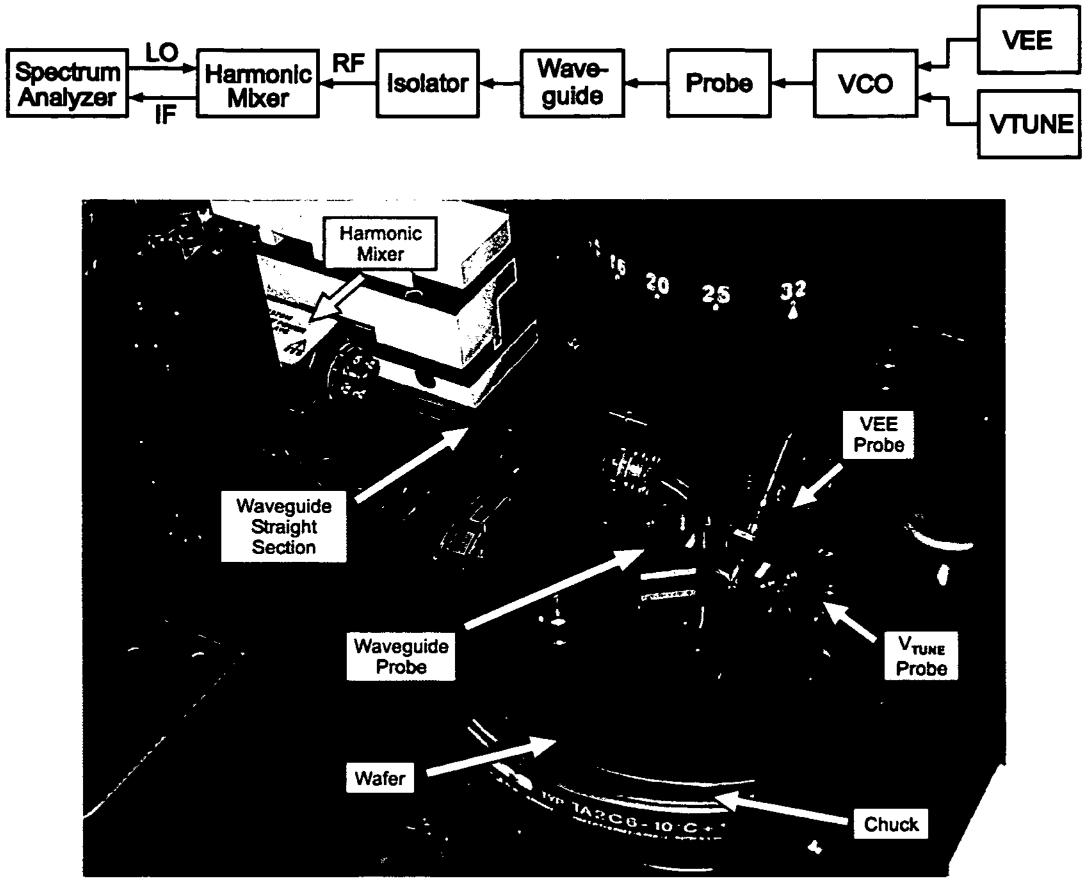


Figure 5.12: Schematic diagram and photograph of the measurement setup

5.5.1 Tuning Characteristic and Output Power

In Fig. 5.13 the measured oscillation frequency and the output power versus the VCO tuning voltage are plotted. The measured output power is about −9 dBm, however due to the losses in the measurement setup, the actual output power is approximately −6 dBm. The output frequency can be tuned from 95.2 GHz to 98.4 GHz. The nonlinear behavior of the tuning characteristic results from the nonlinear dependence of the depletion capacitance on the tuning voltage, see Fig. 5.7. The frequency steps in the tuning behavior in Fig. 5.13 result from influence due to the measurement setup, which is analyzed in this section on page 92.

In Fig. 5.14 the measured output spectrum of the VCO at an oscillation frequency of 98.2 GHz is shown.

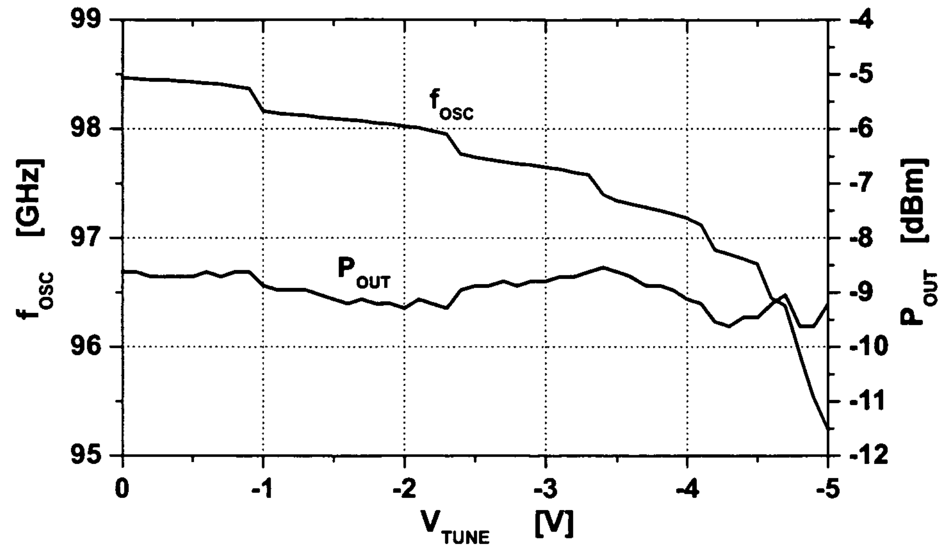


Figure 5.13: Measured oscillation frequency f_{osc} and output power P_{out} vs. tuning voltage of the 98 GHz VCO

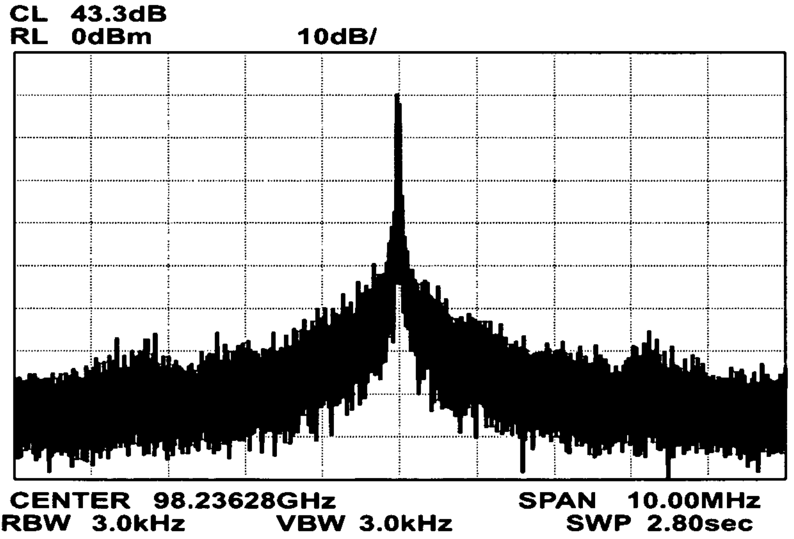


Figure 5.14: Output spectrum at a oscillation frequency of 98.2 GHz

5.5.2 Phase Noise Measurements

Phase noise of oscillators is characterized by statistical, short-term frequency and phase fluctuations of the output signal. A general time-dependent signal, neglecting amplitude deviations[1], can be written as

---

[1] Oscillator limiting mechanisms tend to eliminate amplitude noise. Therefore, oscillator noise near the carrier frequency can be assumed to result exclusively from phase noise.

$$S(t) = A \cdot \cos\left[2\pi f_0 t + \Delta\theta(t)\right] \tag{5.9}$$

where f_0 represents the carrier frequency and $\Delta\theta(t)$ denotes phase fluctuations. The amplitude A is assumed to be constant. Based on the relation between phase fluctuations and instantaneous frequency [Proakis 94], frequency fluctuations $\Delta f(t)$ are defined as

$$\Delta f(t) = \frac{1}{2\pi}\frac{d\Delta\theta(t)}{dt}. \tag{5.10}$$

Due to the statistical behavior of $\Delta\theta(t)$ and $\Delta f(t)$ these variables can be expressed as spectral densities:

$$S_{\Delta\theta}(f_m) = \frac{\Delta\theta^2_{rms}(f_m)}{B}. \tag{5.11}$$

$$S_{\Delta f}(f_m) = \frac{\Delta f^2_{rms}(f_m)}{B} \tag{5.12}$$

The spectral densities $S_{\Delta\theta}(f_m)$ and $S_{\Delta f}(f_m)$ denote the mean-square phase and frequency fluctuations specified as a function of the offset frequency f_m from the carrier frequency f_0 referred to the measurement bandwidth B, which is usually 1 Hz.

Derived from (5.10), $S_{\Delta\theta}(f_m)$ and $S_{\Delta f}(f_m)$ are related as:

$$S_{\Delta\theta}(f_m) = \frac{S_{\Delta f}(f_m)}{f_m^2} \tag{5.13}$$

The most frequently used expression for phase noise specifications is the single-sideband phase noise $L(f)$. It is defined as the noise power in a 1-Hz bandwidth at an offset frequency f_m from the carrier frequency divided by the carrier signal power. Phase noise usually is given in dBc/Hz. In the case of small phase fluctuations (< 0.2 rad), $L(f_m)$ can be calculated as:

$$L(f_m) = \frac{S_{\Delta\theta}(f_m)}{2} = \frac{1}{2f_m^2}S_{\Delta f}(f_m) \tag{5.14}$$

This equation of $L(f_m)$ holds only if it can be assumed that the noise sidebands at $f_0 \pm f_m$ are correlated, i.e., that noise at both frequencies stems from the same noise source.

A linear approach for the calculation of oscillator phase noise has been published by D.B. Leeson in 1966 [Leeson 66]. With this, the single-sideband phase noise at an offset frequency f_m is calculated with the assumption of a constant resonator quality factor. If the signal-to-noise ratio of the active device includes $1/f$-noise, $L(f_m)$ of oscillators can be derived as [Rohde 97]

$$L(f_m) = \frac{1}{2}\frac{kTF}{P}\left(1 + \frac{f_0}{2Qf_m}\right)^2 \left(1 + \frac{f_c}{f_m}\right) \tag{5.15}$$

where k is the Boltzmann constant, T is the absolute temperature, F is an excess noise factor, P is the signal power, f_0 is the oscillation frequency, Q is the loaded quality factor and f_c is the 1/f noise corner frequency. Depending on the relation between f_c and $f_0/2Q$, there are two cases of interest. For the low-Q-case, (5.15) exhibits an $L(f_m)$ which shows a $1/f^3$ and a $1/f^2$ dependence close to the carrier. For the high-Q case, a region of $1/f^3$ and a $1/f$ should be observed near the carrier. The fully-integrated oscillator investigated in this work comprises a low quality factor and therefore the $1/f^3$ and $1/f^2$ dependence is expected.

The phase noise performance of the VCO is measured with the phase noise measurement system Europtest PN-9000. The delay line method, shown in Fig. 5.15, is applied which is also called the autocorrelation method.

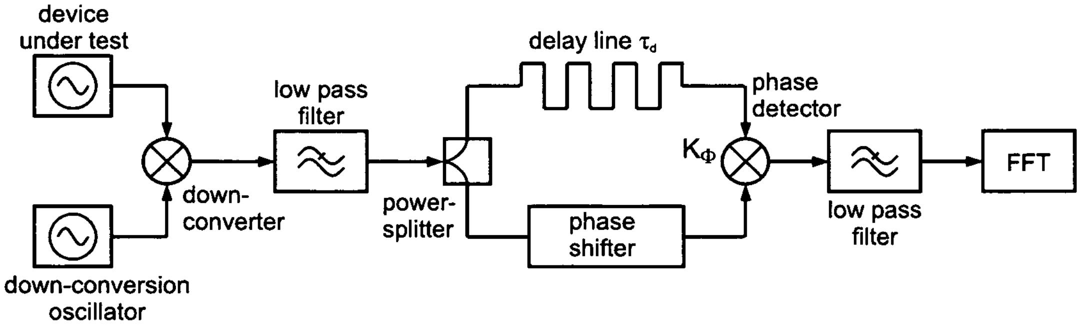


Figure 5.15: Phase noise measurement

In this method a frequency discriminator, composed of a delay line, a phase shifter and a mixer, is used in order to produce a voltage $\Delta V_{rms}(f_m)$ that is proportional to the frequency fluctuation $\Delta f_{rms}(f_m)$:

$$\Delta V_{rms}(f_m) = K_\phi 2\pi\tau_d \Delta f_{rms}(f_m)\frac{\sin(\pi f_m \tau_d)}{\pi f_m \tau_d}. \tag{5.16}$$

In this equation K_ϕ denotes the phase detector constant and τ_d is the delay time. For small offset frequencies $f_m < 1/(2\pi\tau_d)$ the function $\sin(x)/x \approx 1$ and (5.16) simplifies to:

$$\Delta V_{rms}(f_m) = K_\phi 2\pi\tau_d \Delta f_{rms}(f_m). \tag{5.17}$$

Now, using (5.12), (5.14), and (5.17), $L(f_m)$ can be calculated as

$$L(f_m) = 10 \log \left[\frac{\Delta V_{rms}^2(f_m)}{2 f_m^2 B (2\pi K_\phi \tau_d)^2} (1\,\mathrm{Hz}) \right] \quad \mathrm{dBc/Hz}. \tag{5.18}$$

Prior to the measurement, the values for K_ϕ and τ_d must be calibrated. The measurement equipment automatically adjusts the phase difference of the mixer input signals to 90^o so that the mixer acts as phase detector.

The advantages of the frequency discriminator method are:

1. Frequency fluctuations $\Delta f(t)$ are measured directly.
2. There is no reference oscillator required in this setup.
3. Even strongly drifting oscillators can be measured.
4. This method exhibits strong suppression of AM-Noise.

On the other hand, this method has several disadvantages:

1. For measuring $S_{\Delta\theta}(f_m)$ or $L(f_m)$, the sensitivity decreases quadratically for small offset frequencies f_m, see (5.13).
2. The sensitivity also decreases at higher offset frequencies f_m. The limit is $f_m = 1/\tau_d$, see (5.16).
3. The sensitivity is significantly affected by the delay time τ_d. A long delay-time exhibits high sensitivity.

The frequency range of the phase noise measurement system Europtest PN-9000 is restricted from 400 MHz to 1.7 GHz. Therefore the output signal of the VCO at a frequency of about 98 GHz is down-converted using a harmonic mixer from Agilent (11970W) which serves the frequency range from 75-110 GHz and a down-conversion oscillator, see Fig. 5.15. So the sum of the phase noise of the down-conversion oscillator and the device under test is measured. Since the down-conversion oscillator exhibits a much better phase noise, its contribution to the measured phase noise can be neglected. Additionally an Agilent coaxial-to-waveguide adapter V281A is applied. The coaxial system in front of the harmonic mixer exhibits about 20 dB loss in the considered frequency range. Thus, matching is improved and the influence of the measurement equipment is avoided. In Fig. 5.16 the single-sideband phase noise of the VCO versus offset frequency is shown. At an offset frequency of 1 MHz the phase noise is −85 dBc/Hz. According to (5.15) the $1/f^2$ and the $1/f^3$ region can be separated clearly, see Fig. 5.16. The 1/f noise corner frequency of the VCO is about 5 kHz.

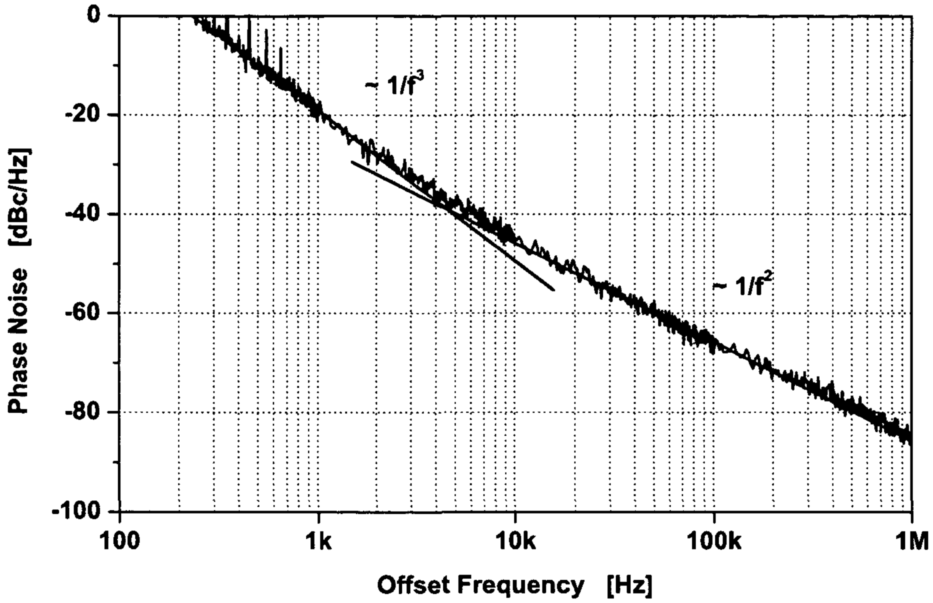


Figure 5.16: Phase noise of the 98 GHz VCO

5.5.3 Influence of the Measurement Equipment

The influence of the waveguide components becomes obvious in the frequency steps of the tuning behavior, see Fig. 5.13. The height of these steps directly corresponds to the length of the waveguide which acts as an additional resonator for the oscillator. This influence is denoted as frequency pulling.

The following derivation gives an accurate approximation for the height of these frequency steps. At first, the wavelength of the TE_{10}-mode in the waveguide has to be calculated:

$$\lambda_{H_1} = \frac{c}{\sqrt{f_1^2 - f_c^2}} \tag{5.19}$$

where c denotes the speed of light in free space, f_1 is the signal frequency and f_c is the cutoff frequency of the waveguide, which is 59.01 GHz for a WR-10 waveguide. This wavelength leads to n half-waves in a resonator with a length l:

$$n = \frac{l}{\lambda_{H_1}} \cdot 2 \tag{5.20}$$

The closest possible resonant frequency to f_1 is either a state with $n+1$ or $n-1$ half-waves in the resonator. In the case of $n+1$ half-waves a wavelength λ_{H_2}, which corresponds to a signal frequency f_2, is obtained:

$$\lambda_{H_2} = \frac{l}{n+1} \cdot 2 \tag{5.21}$$

$$f_2 = \sqrt{\frac{c^2}{\lambda_{H_2}^2} + f_c^2} \tag{5.22}$$

The height of the frequency steps Δf is the difference of f_2 and f_1, $\Delta f = f_2 - f_1$, which leads to:

$$\Delta f = \sqrt{\left(\sqrt{f_1^2 - f_c^2} + \frac{c}{2l}\right)^2 + f_c^2} - f_1 \,. \tag{5.23}$$

The measurements have been performed with a 10 inch waveguide, which results together with the probe and the isolator in a total resonator length of $l = 34\,\text{cm}$. At a signal frequency of $f_1 = 98\,\text{GHz}$, Δf results to approximately 350 MHz, see Fig. 5.13.

The resonator not only influences the tuning characteristic but also improves the phase noise. In Fig. 5.17 the phase noise of the VCO at 1 MHz offset frequency is simulated versus tuning voltage. In this simulation the waveguide at the output is included. The characteristic in this simulation shows a hysteresis, so in Fig. 5.17 the tuning voltage was decreased continuously from 0 V to −5 V. The simulated tuning behavior is almost the same as in the measurements, see Fig. 5.13. It can be seen that the phase noise is subject to strong variations which correspond to the frequency steps. This behavior has been verified by measurements which exhibit a minimum phase noise of −97 dBc/Hz and a maximum phase noise of −85 dBc/Hz, both at 1 MHz offset.

In order to prevent the influence of the waveguide an on-chip output buffer could be used. In the measurements of Fig. 5.18 the resonator was avoided by applying high losses, see Section 5.5.2. This measurement setup enabled smooth tuning curves, Fig. 5.18, and accurate phase noise data at the cost of reduced output power.

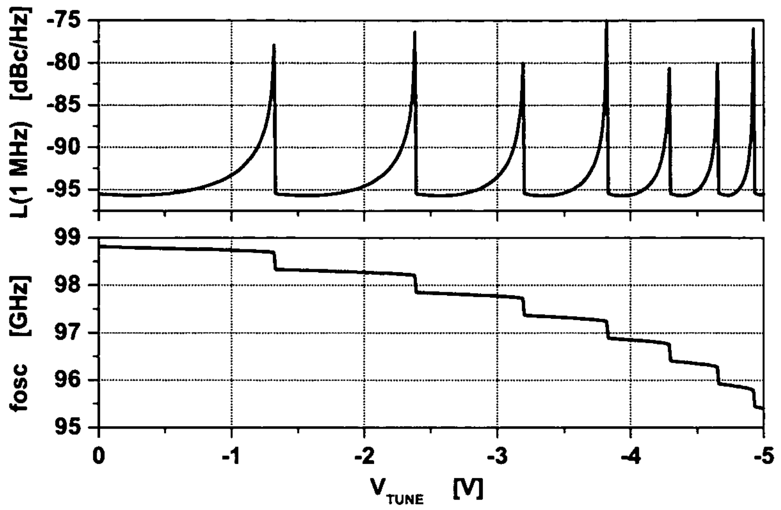


Figure 5.17: Simulated tuning behavior and phase noise at 1 MHz offset frequency of the 98 GHz VCO versus a continuously decreasing tuning voltage including the waveguide at the output

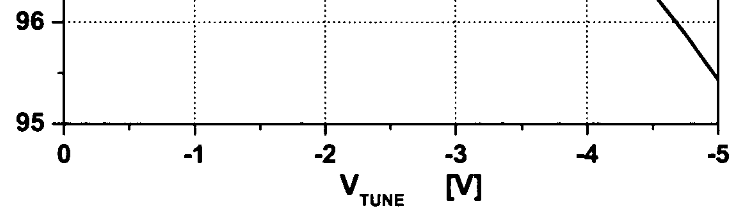


Figure 5.18: Measured oscillation frequency vs. tuning voltage of the 98 GHz VCO. A coaxial measurement equipment is used.

5.6 Summary

The presented voltage-controlled oscillator is the first fundamental mode oscillator fabricated in a silicon-based technology with an oscillation frequency of more than 98 GHz. The output frequency of this circuit is beyond the frequency range of recently emerging high frequency applications like automotive radar systems at 77 GHz and industrial distance sensor systems at 94 GHz. In order to increase the maximum possible oscillation frequency, a transmission line at the output is used.

Further improvements of the circuit performance are possible by a redesign. In order to avoid frequency pulling, isolation between the output and the oscillator core must be guaranteed. This can be done by implementation of an on-chip buffer amplifier realized either by an additional stage or by using a cascode configuration.

With this result it is demonstrated, that voltage controlled oscillators for microwave applications up to 100 GHz are feasible in a low-cost SiGe bipolar technology. Table 5.2 summarizes the technical data of the oscillator.

Technology	0.18 μm / 206 GHz f_T SiGe bipolar
Supply voltage	−5.0 V
Supply current	12.2 mA
Frequency range	95.2 GHz to 98.4 GHz
Measured output power	−9.6 dBm to −8.6 dBm
Phase noise at 1 MHz offset	−85 dBc/Hz (at 98.2 GHz)
Chip size	550 μm × 450 μm

Table 5.2: Technical data of the 98 GHz VCO

Chapter 6

Conclusion and Outlook

In the presented work, monolithic integration of analog building blocks for applications at microwave frequencies in a state-of-the-art low-cost SiGe:C bipolar technology is demonstrated. Due to operation frequencies in the microwave frequency range, the on-chip wavelength is in the range of chip dimensions. So wave-propagation effects must be considered also in integrated circuit design. This fact on the one side brings up difficulties that must be handled with care, but on the other side it enables new approaches. New circuit architectures become possible because components like on-chip transmission lines or on-chip microstrip couplers, for example, are now feasible. By means of these new circuit architectures as well as the improvements of the technology record values for the presented circuits are reached.

Subsequently, the results of the circuits of this work are summarized. At first, the results of a broadband amplifier for high data rate communication systems are presented. Then the results of a down-conversion mixer for distance sensors in automotive and industrial applications are summarized. Finally, a voltage controlled oscillator with an oscillation frequency in the microwave frequency range is demonstrated.

The broadband amplifier of this work is based on a lumped element architecture. The broadband amplifier is based on a fully differential design and consists of two stages. The fabricated circuit exhibits 16 dB gain, a bandwidth of 62 GHz, a 1-dB compression point of -9.5 dBm, and a third-order intercept point of $+2.1$ dBm, both referred to the input. With this chip, clear output eye diagrams at 80 Gbit/s and at 100 Gbit/s with an eye opening of 1 $\mathrm{V_{PP}}$ and 680 $\mathrm{mV_{PP}}$, respectively, are demonstrated. These are the highest data rates for analog building blocks in silicon as well as in III-V semiconductors reported so far.

A fully-integrated down-conversion mixer for automotive radar applications in the frequency range of 77 GHz is presented. The circuit architecture consists of a mixer core based on the Gilbert cell, a new type of LC balun, and an LO buffer for providing differential signals to the mixer core. This circuit exhibits a gain of more than 24 dB and a low SSB noise figure of less than 14 dB in a frequency range much larger than the target frequency range. Conversion gain and SSB noise figure are only a weak function of the IF frequency for intermediate frequencies down to 10 kHz. Especially for homodyne system architectures the performance at low IF is of particular importance. This mixer is the first active down-conversion mixer realized in silicon-based technologies for the frequency range around 77 GHz.

Finally a fundamental-mode voltage-controlled oscillator fabricated in a SiGe:C bipolar technology is presented. The oscillator is based on the common collector Colpitts oscillator. At the output a transmission line is used for impedance transformation in order to increase the maximum possible oscillation frequency. With this circuit, an oscillation frequency of more than 98 GHz at an output power of −6 dBm and a SSB phase noise of −85 dBc/Hz is reached. The presented voltage-controlled oscillator is the first fundamental mode oscillator fabricated in a silicon-based technology with an oscillation frequency of more than 98 GHz.

This work demonstrates outstanding results of monolithically integrated analog building blocks. Applications which could be realized up to now only in III-V semiconductors are now feasible in a low-cost state-of-the-art SiGe:C technology. This is possible due to progress in technology development, new circuit architectures, as well as accurate optimization. Further advances in process technologies and circuit design will result in continuing the upward shift of the frequency limits. A further field of research will be integration of several building blocks onto one substrate in order to realize integrated single-chip solutions. Therefore, interactions between building blocks must be taken into account and the characteristics of the respective blocks must be adjusted to the system specification. A further very challenging task towards microwave semiconductor applications is the packaging of the chips. A promising packaging technology for microwave frequency interconnects seems to be flip-chip packaging.

List of Abbreviations

α_F	forward common-base current gain
α_R	inverse common-base current gain
A	voltage gain
AC	alternating current
As	arsenide
β_F	forward current gain
β_R	inverse current gain
B	bandwidth
B	boron / base
BC	base-collector
BE	base-emitter
BiCMOS	bipolar-CMOS
C	capacitance
C	collector
CE	collector-emitter
CMOS	complementary metal oxide semiconductor
CMRR	common mode rejection ratio
CP	compression point
CS	collector-substrate
δ	skin depth
DC	direct current
DEMUX	demultiplexer
DSB	double-sideband
DT	deep trench
DUT	device under test
ε	permittivity
E	emitter
ENR	excess noise ratio
f	frequency
f_{dop}	doppler frequency
f_T	cutoff frequency
f_β	3-dB cutoff frequency

f_{max}	maximum oscillation frequency
F	noise figure
FET	field effect transistor
FMCW	frequency modulated continuous wave
G	power gain
GaAs	gallium arsenide
GBIP	general purpose interface bus
Ge	germanium
GND	ground
GPS	global positioning system
GS	ground-signal
GSM	global system for mobile communications
GSSG	ground-signal-signal-ground
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
HFET	heterostructure field effect transistor
I	current
I_{BCS}	BC diode saturation current
I_{BES}	BE diode saturation current
I_S	transfer saturation current
I_T	transfer current
IF	intermediate frequency
Im()	imaginary part
InP	indium phosphide
IP3	third-order intercept point
k	Boltzmann constant
K_ϕ	phase detector constant
λ	wavelength
L	inductance
$L(f_m)$	SSB phase noise
LAN	local area network
LC	inductor-capacitor
LNA	low noise amplifier
LO	local oscillator
μ	permeability
MESFET	metal semiconductor field effect transistor
MIM	metal insulator metal
MUX	multiplexer
N	noise power
ω	angular frequency
OFDM	orthogonal frequency division multiplex
P	phosphor / signal power
PLL	phase locked loop

PRBS	pseudo random bit sequence
Q	quality factor
q_b	normalized majority base charge
R	resistance
Re()	real part
RF	radio frequency
RX	receive
SG	signal-ground
Si	silicon
SiGe	silicon germanium
SiGe:C	silicon germanium, carbon
SNR	signal-to-noise ratio
SSB	single-sideband
STI	shallow trench isolation
τ_d	delay time
τ_F	forward transit time
t	time
T	absolute temperature
TaN	tantalum nitride
TEM	transmission electron microscopy
TRL	transmission line
TV	television
TX	transmit
UMTS	universal mobile telephone standard
UWB	ultra wideband
V	voltage
V_{AF}	Early voltage
V_T	thermal voltage
VCO	voltage-controlled oscillator
VEE	negative supply voltage
WLAN	wireless local area network
Z	impedance

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