Technische Universität Wien

DIPLOMARBEIT

BURST MODE RECEIVER FOR PASSIVE OPTICAL NETWORKS

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines Diplom-Ingenieurs

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Abstract

A Burst Mode Receiver chip for Passive Optical Networks is presented. The chip is produced in a standard digital 120 nm CMOS process. High gain and high sensitivity are achieved. This diploma thesis describes basics of optical receivers and the circuit design. The development of the test chip is presented in thorough detail including schematics, simulation graphs and the layout. Two evaluation PCBs were designed and are described too. The measurement results are then presented and followed by a comparison to the simulation results and to other published works.

The incident light wavelength is $\lambda = 1300\,\text{nm}$. For this wavelength an external photodiode is necessary because (integrated) silicon photodiodes only receive $\lambda < 1140\,\text{nm}$. An external photodiode implies a high input capacity. This lowers the total bandwidth and increases the input referred current noise.

The receiver has a single supply with 1.5 V where the transimpedance amplifier alone only consumes 100 mW. The chip area of the TIA is 18,840 μm^2. Control circuits (with large capacitors) add an area of 36,120 μm^2. The total area is 55,000 μm^2. The chip area itself is 1.5 mm^2 containing the pad frame and supply stabilizing capacitors.

The chip achieves a sensitivity of -27.6 dBm at 1.25 GBit/s for a BER = 10^{-10}. At 2.5 GBit/s the sensitivity is -20.4 dBm at the same BER. The value was determined with a bad laser which emits at 2.5 GBit/s an eye not allowing for reliable measurements. The results at the highest bit rate are thus expected to be better when a higher-quality laser source is used.

The chip utilizes a special circuit named “Prepare and Hold” for rapid changes of its gain. The gain can be switched within 800 ps from maximum to minimum and within 2.3 ns in the reverse direction. This values are better by a factor of 10 or more compared to any published works which, by the way, operate at only 1.25 GBit/s.

Zusammenfassung

In dieser Diplomarbeit wird ein Burst Mode Empfänger Chip für Passive Optische Netze präsentiert. Der Chip wurde in einem digitalen Standard-120 nm-CMOS Prozess gefertigt. Hohe Verstärkung und hohe Empfindlichkeit wurden erreicht. In dieser Arbeit werden die Grundlagen und die Schaltungstechnik von optischen Empfängern beschrieben. Die Entwicklung des Test-Chips mit Schaltplänen, Simulationsergebnissen und den Layouts wird besonders genau ausgeführt. Zum Test des Chips wurden zwei Platinen entwickelt, die ebenfalls erklärt werden. Am Ende werden die Messergebnisse präsentiert und mit den Simulations-Ergebnissen und anderen publizierten Ergebnissen verglichen.

Die Wellenlänge des empfangenen Lichts beträgt $\lambda = 1300\,\text{nm}$. Dafür ist eine externe Photodiode notwendig, da (integrierte) Silizium-Photodioden nur für $\lambda < 1140\,\text{nm}$ geeignet sind. Eine externe Photodiode bedeutet jedoch eine hohe Eingangsknotenkapazität wodurch die Bandbreite der Schaltung verringert und das Rauschen erhöht wird.

Der Empfänger wird mit 1,5 V versorgt wobei der Transimpedanzverstärker selbst eine Leistung von nur 100 mW benötigt. Die Chip-Fläche des TIAs alleine beträgt $18.840\,\mu\text{m}^2$. Die Steuerschaltung mit großen Kondensatoren erhöht die Fläche um $36.120\,\mu\text{m}^2$ auf $55.000\,\mu\text{m}^2$. Die Fläche des gesamten Chips ist $1{,}5\,\text{mm}^2$ wobei die restliche Fläche vom Pad-Frame und den Kondensatoren zur Stabilisierung der Versorgung verbraucht wird.

Der Chip erreicht eine Empfindlichkeit von -27,6 dBm bei 1,25 GBit/s für ein BER $= 10^{-10}$. Bei 2,5 GBit/s ist die Empfindlichkeit -20,4 dBm bei gleichem BER. Dieser Wert wurde mit einem schlechten Laser gemessen, der bei 2,5 GBit/s ein Auge abstrahlt, das keine zuverlässige Messung erlaubt. Die Messergebnisse sollten bei Verwendung eines passenden Lasers besser sein.

Am Chip wird eine spezielle Schaltung namens “Prepare and Hold” eingesetzt mit der eine sehr schnelle Änderung der Verstärkung erzielt wird. Die Verstärkung kann innerhalb von nur 800 ps vom höchsten auf den geringsten Wert und innerhalb von 2,3 ns in umgekehrter Richtung eingestellt werden. Diese Werte sind um mindestens einen Faktor 10 besser als in aktuell publizierten Arbeiten, die übrigens alle bei nur 1,25 GBit/s arbeiten.

Acknowledgment

I want to thank Prof. Horst Zimmermann and Kerstin Schneider from the *Institut für elektrische Mess- und Schaltungstechnik* who supervised this diploma thesis. Kerstin advised me in the usage of the chip design software and the laboratory equipment. She gave me countless good hints and stimulated me to creative ideas.

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Kudos go to the worldwide *open source community* which develops numerous highly professional tools. The tools I used most during my diploma thesis are: LaTeX, BibTeX, XFig, GNU Make, GVim, lots of other powerful GNU tools (sed, awk, octave, ...), Netpbm, Linux, GhostScript, GV and many others. Thanks go to their authors, maintainers, documentors, translators and all others who are involved to provide these programs.

Finally I want to thank Infineon `http://www.infineon.com/` for making all this possible. Infineon produced the test chip and provided a friendly place to work.

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Introduction

BROADBAND internet access is currently one of the fastest growing markets in telecommunication. Common technologies are "x Digital Subscriber Line (xDSL)" and cable TV. The most promising future technology is *Passive Optical Network (PON)*. The catch word "*Fiber To The x (FTTx)*" is used. Examples include

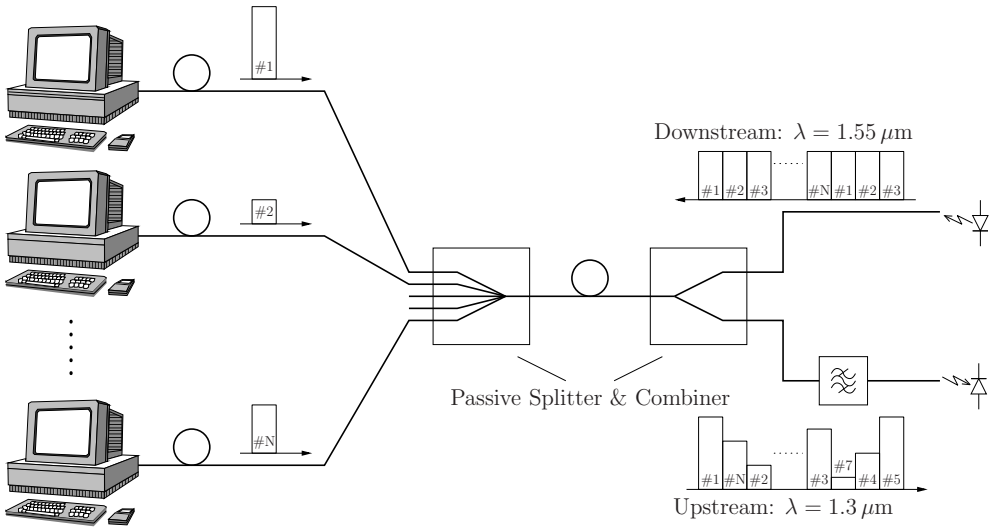
- Fiber To The Home (FTTH),
- Fiber To The Desk (FTTD),
- Fiber To The Office (FTTO),
- Fiber To The Curb (FTTC),
- Fiber To The Building (FTTB).

A fiber cable is directly available at the host.

1.1 Overview

In PONs (see Fig. 1.1) there is a single fiber to every end station. Full duplex transmission is realized with different wavelengths for upstream ($\lambda = 1.3\,\mu$m) and downstream ($\lambda = 1.55\,\mu$m) communication. At the central station all fibers are joined with a *passive* star coupler. There is a single laser and a single *Photodiode (PD)*. Data for the various end stations is sent and received in *Time Division Multiplex (TDM)*. This means that the data packets are sent as bursts via the fiber. Every burst is dedicated to one end station. A single burst only contains a few bits (approx. 400, compare [Säc01]).

Figure 1.1: Schematic setup of a Passive Optical Network (PON)

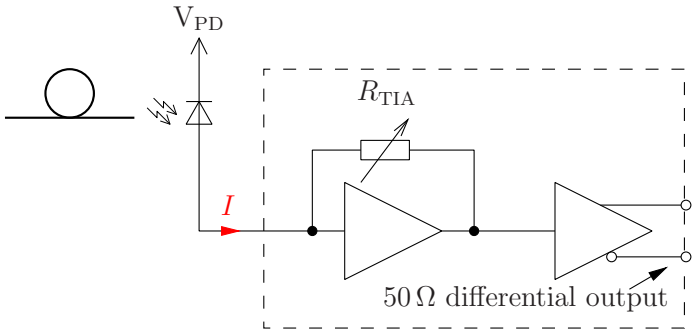


This diploma thesis deals with the development and test of a *Burst Mode Receiver (BMR)* chip for PONs (see Fig. 1.1). The various end stations may have different distance to the central office. This results in different optical power received in the central office because of the fiber attenuation. A BMR has to adapt its *gain* according to the incoming intensity. Higher level protocols provide the control signals to the optical receiver.

The intensity of incident light can vary by 20 dB which means 40 dB input current variation because the photodiode linearly converts the optical power to electrical current (see (1.3)). To avoid a loss of data transfer rate, the change of gain must be settled quickly. Only a few bits are allowed to be lost. In Fig. 4.12 the simulation result of this process is shown.

In Fig. 1.2 the principal structure of the optical receiver is depicted. The light is received by the PD. It converts the optical power to electrical current. This enters the BMR chip via a bond wire. The first stage is implemented as a so called

Figure 1.2: Rough schematic of the optical receiver



Trans-impedance Amplifier (TIA). This converts the current from the photodiode to a voltage. The TIA is followed by the 50 Ω output driver. It has a built-in conversion from the single ended signal to a differential signal.

For cost effective central office equipment, the BMR is included in the digital receiver chip. This combination of an analog amplifier and a digital receiver and control unit is called a *System on Chip (SoC).*

Including an analog front end onto a mostly digital chip has several advantages. Apparently there is only one chip instead of two. This saves packaging cost and board space. The signal line from the analog amplifier to the digital decision device doesn't have to leave a chip package, go via the PCB board and enter another chip. This increases the bandwidth. Finally there is only one chip to produce which decreases costs additionally.

The disadvantage of this combinations is that the digital part will introduce substrate noise to the analog part. Both parts have to be isolated carefully.

An on-chip PD would even more increase the bandwidth and decrease the noise. Unfortunately silicon photodiodes are only able to detect light up to wavelengths $\lambda < 1140\,\text{nm}$ (see [Lee01]). For the employed wavelength of $\lambda = 1300\,\text{nm}$ an external PD is necessary. For more details refer to Sec. 2.2.4.

However, this diploma thesis is about the development of the analog part only. There is no digital part available. For *characterization and measurement* of the TIA, its output has to be fed into measurement equipment. For high frequencies these are only available as 50 Ω devices. Therefore a strong output amplifier is included at the test chip. This will not be necessary in the final product.

The gain of the TIA can be adjusted by several *control voltages*. These have to change very quickly when the next party (with different distance and thus attenuation) is to be received. In the final chip the control voltages for the amplifier are provided by Digital to Analog Converters present on the SoC. For the test chip they are fed from external sources via bonding pads. Nevertheless,

both methods are unable to supply these fast and accurate edges. Therefore a special *Prepare and Hold* circuit is introduced to eliminate this problem.

The chip is produced in a purely digital 120 nm CMOS process. This is also destined for the final receiver chip with digital logic. The bit rate is given by BR = 2.5 GBit/sec. The allowed time to switch amplification is limited by $t_{\text{switch}} \leq 1\,\text{ns}$.

1.2 Outline

In this section a short overview of the content of this diploma thesis will be given.

- Chapter 1 contains the specification of the chip. Some derivations to resulting properties are made.
- In chapter 2 some basics of optical receivers are presented. The concept of PONs and burst mode transmission is discussed.
- The basics on circuit design in chapter 3 include analog circuits, CMOS circuits and noise theory.
- Chapter 4 is dedicated to the actual development of the chip. It starts with its structure, this is followed by details of various important parts. Finally the total chip is shown.
- The test PCBs for measurements are discussed in chapter 5. At the beginning the desired measurements are listed. Basing on that the necessary environment for the chip is developed. Finally two different evaluation PCBs are introduced.
- In chapter 6 the measurement results are presented and compared to the simulation results.
- A summary of the results as well as a comparison to other available burst mode receivers is contained in chapter 7.

1.3 Specification

In Tab. 1.1 the *specification of the chip* is given. The surrounding components have their own specification as listed in Tab. 1.2. A few more numbers follow starting from these figures of merit are given in Tab.1.3.

Table 1.1: Specification of the chip

Specification	**Symbol**		**Value**
Supply voltage	V_{DD}	$=$	$1.5\,\mathrm{V}$
Bit Rate	BR	$=$	$2.5\,\mathrm{GBit/s}$
Bit Error Ratio	BER	$=$	10^{-10}
Minimum average optical input power	$\overline{P}_{\mathrm{opt,min}}$	$\ll$	$-23\,\mathrm{dBm}$
Maximum input current (peak)	$I_{1,\mathrm{max}}$	$=$	$300\,\mu\mathrm{A}$
Time to switch gain	t_{switch}	$\leq$	$1\,\mathrm{ns}$
Output voltage of the TIA	$\Delta V_{\mathrm{TIA,out}}$	$\sim$	$40\,\mathrm{mV_{pp}}$ + DC

Table 1.2: Specification of the components around the chip

Specification	**Symbol**		**Value**
Photodiode Responsivity	R	$=$	$0.85\,\mathrm{A/W}$
Laser Extinction Ratio	Ex	$=$	10

Table 1.3: Resulting additional specification of the chip

Specification	**Symbol**		**Value**
Bit duration	t_{Bit}	$=$	$400\,\mathrm{ps}$
Bandwidth of the TIA	$f_{\mathrm{c,TIA}}$	$=$	$1.67\,\mathrm{GHz}$
Minimum input current (peak)	$I_{1,\mathrm{min}}$	$=$	$7.7\,\mu\mathrm{A}$
Maximum average input power	$\overline{P}_{\mathrm{opt,max}}$	$=$	-7 dBm
Argument of $\mathcal{Q}$-Function	Q	$=$	6.3
maximum RMS noise current	$\sqrt{\overline{i^2_{\mathrm{n,in}}}}$	$=$	$550\,\mathrm{nA}$
Minimum Transimpedance of the TIA	$R_{\mathrm{TIA,min}}$	$\sim$	$100\,\Omega$
Maximum Transimpedance of the TIA	$R_{\mathrm{TIA,max}}$	$\sim$	$6\,\mathrm{k}\Omega$

1.3.1 Bit Duration and Bandwidth

The bit duration is given by

$$t_{\mathrm{Bit}} = \frac{1}{\mathrm{BR}}. \tag{1.1}$$

The 3 dB cutoff bandwidth of the TIA is given by 2/3 of the bit rate BR:

$$f_{\mathrm{c,TIA}} = \frac{2}{3}\mathrm{BR} \tag{1.2}$$

This is a tradeoff between signal distortion and noise transferred via the low pass characteristic (see Sec. 4.1.1.1). As we will see later (Sec. 4.2.4 and Chap. 6) the bandwidth of the TIA is above $f_{\mathrm{c,TIA}}$. Unfortunately the on chip output amplifier (50 Ω driver) decreases the total bandwidth. This necessitates a higher bandwidth of the TIA.

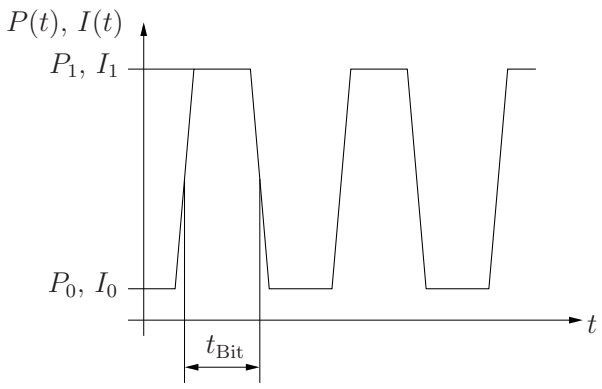
1.3.2 Input Power and PD-Current

The input current to the TIA is provided by the PD. It is given by

$$I(t) = R \cdot P(t). \tag{1.3}$$

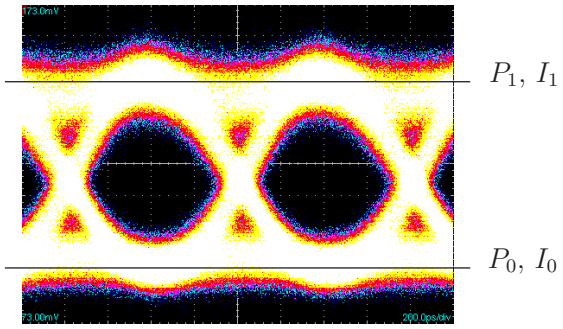
where $P(t)$ is the optical power of the received light (see Sec. 2.2.4). This equation holds for the instantaneous value as well as for average values. The shape of the input current is depicted in Fig. 1.3. In the following derivation we use the symbols I_0, I_1, P_0 and P_1 as mean values averaged over all "1"s or all "0"s for their own. This is illustrated in Fig. 1.4.

Figure 1.3: Optical power and input current for a hypothetical 010101 bit sequence



It is worth to mention that the incident optical power is linearly converted to electrical current (see (1.3)). If the optical power varies by 20 dB (which is a

Figure 1.4: Average input current for "0"s I_0 and "1"s I_1



factor of 100), the electrical current varies by a factor of 100 too. But for a current this means 40 dB level variation.

The *Extinction Ratio*

$$\mathrm{Ex} = \frac{P_1}{P_0} = \frac{I_1}{I_0} \tag{1.4}$$

specifies the ratio of received signal power for a logic "1" P_1 to the power for a logic "0" P_0. The transmitting laserdiode must be kept above its threshold current for fast modulation (see Sec. 2.2.1). This results in a non-zero P_0.

The power P, the current I and its values for "1"s and "0"s — P_1, I_1 and P_0, I_0 respectively — scale linearly with the attenuation of the fiber, i.e. Ex is only destined by the laser.

When receiving maximum power (i.e. the shortest cable) the logic "1" current is $I_{1,\max}$. For minimum received power (i.e. the longest possible cable) this is $I_{1,\min}$.

Assuming that "0"s and "1"s are transmitted equally likely, the mean value of the optical power is given by

$$\overline{P}_{\mathrm{opt}} = \frac{P_0 + P_1}{2} = P_1 \frac{1 + \mathrm{Ex}}{2\,\mathrm{Ex}} = \frac{I_1}{R} \frac{1 + \mathrm{Ex}}{2\,\mathrm{Ex}}. \tag{1.5}$$

We get P_1 by reversing (1.5) being

$$P_1 = \overline{P}_{\mathrm{opt}} \frac{2\,\mathrm{Ex}}{1 + \mathrm{Ex}} \tag{1.6}$$

and I_1 by substituting (1.6) in (1.3)

$$I_1 = R\,P_1 = R\,\overline{P}_{\mathrm{opt}} \frac{2\,\mathrm{Ex}}{1 + \mathrm{Ex}}. \tag{1.7}$$

The input current amplitude is

$$\Delta I = I_1 - I_0 = I_1 \frac{\mathrm{Ex} - 1}{\mathrm{Ex}}. \tag{1.8}$$

It is related to $\overline{P}_{\text{opt}}$ as

$$\Delta I = R\,P_1\frac{\text{Ex}-1}{\text{Ex}} = R\,\overline{P}_{\text{opt}}\frac{2\,\text{Ex}}{1+\text{Ex}}\frac{\text{Ex}-1}{\text{Ex}} = 2\,R\,\overline{P}_{\text{opt}}\frac{\text{Ex}-1}{\text{Ex}+1} \tag{1.9}$$

1.3.3 Bit Error Ratio and Noise Current

At a demanded *Bit Error Ratio (BER)* the required minimum optical power $\overline{P}_{\text{opt,min}}$ is defined by the input referred current noise. We will now derive the relation between BER, $\overline{P}_{\text{opt,min}} \sim I_{1,\text{min}}$ and $\sqrt{\overline{i^2_{\text{n,in}}}}$.

In [Hla01] the exact *bit error probability* for an ML receiver with binary symbols for an AWGN channel[1] is given by

$$\text{P}_{\text{ML}}\{\mathcal{E}\} = \mathcal{Q}\left(\frac{d}{2\sqrt{N_0}}\right) \tag{1.10}$$

where d is the distance of the signal vectors (in signal space) and N_0 is the noise level.

The "*maximum likelihood*" (*ML*) receiver realizes a symbol by symbol decision. Every decision is made by choosing the minimum distance between the received symbol and the (two) possible symbols out of the symbol alphabet. Its symbol error probability $\text{P}_{\text{ML}}\{\mathcal{E}\}$ given in (1.10) is the same as the BER.

Equation (1.10) uses the so called $\mathcal{Q}$-function. This is defined by

$$P\{Z > z\} = \mathcal{Q}\left(\frac{z-\mu_Z}{\sigma_Z}\right) \tag{1.11}$$

where Z is a Gaussian random variable with mean μ_Z and variance σ_Z^2 and $P\{Z > z\}$ denotes the probability that Z is above z. Evidently the $\mathcal{Q}$ function is an integral of the Gaussian distribution and thus defined by

$$\mathcal{Q}(z) = \frac{1}{\sqrt{2\pi}}\int_z^\infty e^{\frac{1}{2}\zeta^2}d\zeta, \quad z \in \mathbb{R}. \tag{1.12}$$

For more details see [Hla01].

In our case the distance of both signal values (considered with real physical units, here we have current in Ampere) is $d = \Delta I$. The input referred current noise level as mentioned above is $N_0 = \overline{i^2_{\text{n,in}}}$. This gives the final value for the bit error ratio

$$\text{BER} = \text{P}_{\text{ML}}\{\mathcal{E}\} = \mathcal{Q}\left(\frac{\Delta I}{2\sqrt{\overline{i^2_{\text{n,in}}}}}\right). \tag{1.13}$$

[1] additive white Gaussian noise

For a given BER the argument of the $\mathcal{Q}$-function ($\mathcal{Q}(Q)$) $Q = \frac{\Delta I}{2\sqrt{\overline{i^2_{\mathrm{n,in}}}}}$ can be determined either graphically or by reversing the formulas for the upper or lower bounds of the $\mathcal{Q}$-function. Table 1.4 shows typical values of corresponding BER and Q.

Table 1.4: Typical values for BER and Q

BER	$\boldsymbol{Q}$
10^{-9}	6
10^{-10}	6.3
10^{-12}	7

Above ((1.10) and (1.13)) we saw that Q is similar to a Signal to Noise Ratio (SNR). Therefore for a given Q we have a relation between the input signal amplitude and input referred current noise. The input signal ΔI must be twice the RMS noise current $\sqrt{\overline{i^2_{\mathrm{n,in}}}}$ times Q to achieve a certain BER.

$$\Delta I \geq 2\sqrt{\overline{i^2_{\mathrm{n,in}}}} \cdot Q \tag{1.14}$$

In the opposite direction, the (maximum) RMS noise current is determined by a given Q and input signal amplitude

$$\sqrt{\overline{i^2_{\mathrm{n,in}}}} \leq \frac{\Delta I}{2Q} = \frac{R\,\overline{P}_{\mathrm{opt}}}{Q}\frac{\mathrm{Ex}-1}{\mathrm{Ex}+1}. \tag{1.15}$$

For a given minimum optical power $\overline{P}_{\mathrm{opt,min}} = -23\,\mathrm{dBm}$ and thus a given current swing of $\Delta I = 7\,\mu\mathrm{A}$ as well as $Q = 6.3$ for BER $= 10^{-10}$ the maximum RMS noise current is $\sqrt{\overline{i^2_{\mathrm{n,in}}}} = 550\,\mathrm{nA}$.

1.3.4 TIA specifications

The output voltage swing of the TIA $\Delta V_{\mathrm{TIA,out}}$ determines its transimpedance

$$R_{\mathrm{TIA}} = \frac{\Delta V_{\mathrm{TIA,out}}}{\Delta I} = \frac{\Delta V_{\mathrm{TIA,out}}}{I_1}\frac{\mathrm{Ex}}{\mathrm{Ex}-1}. \tag{1.16}$$

This yields the minimum and maximum transimpedance as

$$R_{\mathrm{TIA,min}} = \frac{\Delta V_{\mathrm{TIA,out}}}{I_{1,\mathrm{max}}}\frac{\mathrm{Ex}}{\mathrm{Ex}-1} \tag{1.17}$$

$$R_{\mathrm{TIA,max}} = \frac{\Delta V_{\mathrm{TIA,out}}}{I_{1,\mathrm{min}}}\frac{\mathrm{Ex}}{\mathrm{Ex}-1} \tag{1.18}$$

The $50\,\Omega$ output driver further amplifies the output of the TIA which yields higher transimpedance for the total chip.

2

Optical Receivers

THIS chapter is structured in three parts. At the beginning some theory of communication techniques is presented. This consists of important concepts like multiple access and duplex methods. The second part concentrates on the structure of optical transmission systems. Facts and figures for the stations on the journey of a data bit from the sender to the receiver are brought. Finally an eye is put on the specific properties of PONs.

2.1 Communication Techniques

2.1.1 Multiplex and Multiple Access

In many cases more than one communication is conducted via a single physical channel. The transmission signals of all senders are superposed. Thus the channel is a so called "shared medium". The receivers have to pick up their particular signal out of the mixture of signals on the channel. Concurrent use of a single channel by multiple communications is called *Multiplex*.

For the separation of different communications several methods are commonly used.

- Space Division Multiplex
- Time Division Multiplex
- Frequency Division Multiplex
- Wavelength Division Multiplex
- Code Division Multiplex

If multiple parties are competing to *send* via a single channel this is called *Multiple Access*. Several different *Medium Access Control (MAC)* methods are used. These are basically the same as used for multiplex. E.g. for Ethernet *Carrier Sense Multiple Access with Collision Detection (CSMA/CD)* is used. This is a variant of Time Division Multiple Access (TDMA).

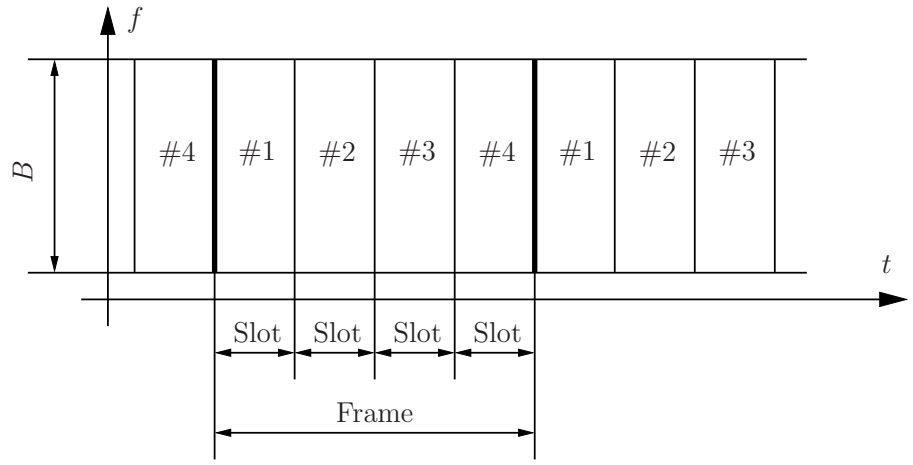
2.1.1.1 Time Division Multiplex

If the channel has enough bandwidth the different signals can be transmitted one after another. This is called *Time Division Multiplex (TDM)*. To conduct several signals (virtually) concurrently, they have to be alternated. Therefore a so called *Frame* with fixed duration is repeated in short intervals. Each frame is split into a constant number of *Time Slots*. Every signal is then assigned to one particular time slot. This is depicted in Fig. 2.1.

2.1.1.2 High Bit Rate

Multiplex is not only used to conduct several competing transmissions via a single channel. We can think of high bit rates as a lot of superposed low bit rate communications. The previously described multiplex methods are all together used to utilize the high bit rate of modern communication channels.

Figure 2.1: Time Division Multiplex



2.2 Fiber Communication

A typical optical data transmission line is built up of the following parts (see Fig. 2.2):

1. Laser Driver (optional)
2. Laser
3. Optical modulator (optional)
4. Fiber
5. Fiber amplifier
6. Photodiode
7. Electrical amplifier
8. Slicer

For more details refer to [Lee01] and [Lee02].

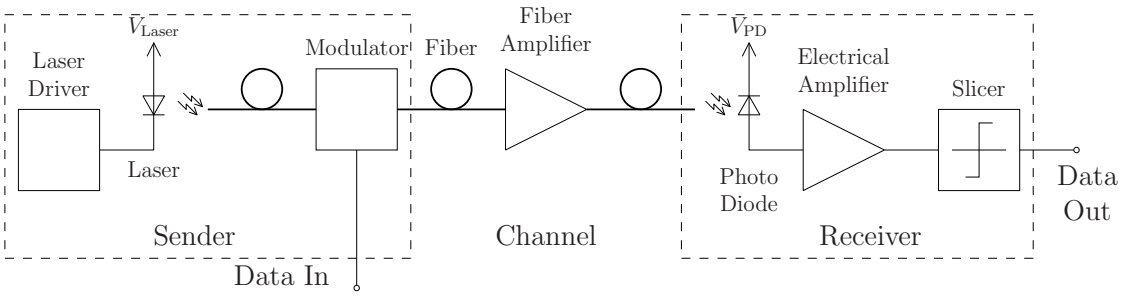
2.2.1 Laser

In fiber optics every transmitted bit is represented by a light pulse. Usually this light is emitted by a *Laser*. It is (almost) monochromatic[1] and coherent[2].

[1] the frequency spectrum is very narrow

[2] the emitted electromagnetic wave has a constant phase instead of a mixture of superposed phases

Figure 2.2: Overview of a typical optical transmission line. Only one of the laser driver *or* the optical modulator are present.



In Fig. 2.3 the P/I characteristic (optical output power depending on electrical current) of a laser is shown. There are two major areas. The left part with a very flat curve is below *threshold*. The laser acts as a (very expensive) *Light Emitting Diode (LED)*. The emitted optical power is very low because no inversion, only spontaneous emission takes place. Above threshold the net gain (stimulated emission minus absorption) is positive and the laser effect occurs. ([Lee01]) Typical values are: threshold current $I_{\text{thres}} = 30 - 50\,\text{mA}$, peak current $I_{\text{peak}} = 60 - 100\,\text{mA}$, peak output power $P_{\text{peak}} = 15\,\text{mW}$.

Typical wavelengths are $\lambda = 890\,\text{nm}$, $\lambda = 1300\,\text{nm}$ and $\lambda = 1550\,\text{nm}$. These wavelengths are chosen to utilize special properties of the fibers. See Sec. 2.2.3 for a discussion of the effects.

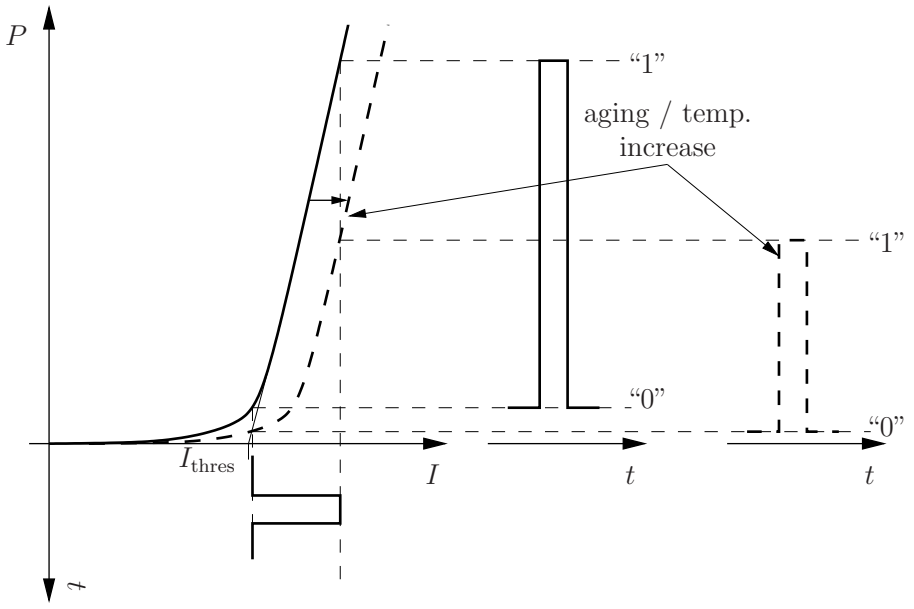
The characteristic strongly depends on temperature. The steep part is shifted horizontally. At a constant drive current I the output power P varies greatly. Usually there are taken two counter measures.

1. cooling
2. monitor

More expensive laser diodes are built in a package with a *Peltier cooling unit* and temperature measurement. Some electronics around the laser controls its temperature at a constant level. This is especially important for lasers with a very narrow spectrum.

Each laser has two mirrors. Between these the light is reflected back and forth. Since *both* mirrors are partially transparent (reflection coefficient $r \approx 99.9\,\%$) the output of the laser is at both sides. Only half of the output power is coupled into the fiber. At the other side a *monitor diode* is mounted to receive the other half of the output power. A low pass filter selects its DC part. The control circuit uses this to keep the mean output power of the laser constant.

Figure 2.3: Laser P/I characteristic



When the laser diode gets older (*aging*), its characteristic also shifts horizontally to the right. Its steepness decreases too. The monitor diode and surrounding control circuit keeps the mean and peak output power constant.

2.2.2 Optical modulator

For data transmission up to 2.5GBit/sec *direct modulation* is used. Therefore the laser current is modulated according to the transmitted bit at the bit rate. As depicted in Fig. 2.3 the current[3] for a logical "0" I_0 is above the threshold current I_{thres}. This is necessary for fast modulation because the transit from and to inversion is time consuming. Evidently the laser emits light even when transmitting a logical "0". The ratio of output power for "1" to output power for "0" is called *Extinction Ratio* Ex. Usually Ex $\approx$ 10. (see Sec. 1.3.2). A *laser driver* is used to generate the high current with fast edges.

For higher bit rates the laser is operated in continuous mode and no laser driver is used. Directly after the laser a dedicated *modulator* (e.g. Electro-optical Absorption Modulator (EAM), Mach Zehnder Modulator (MZM)) is used to modulate the light with the bit stream. Thus the laser driver and the modulator in Fig. 2.2 are mutualy exclusive depending on the application.

[3]As an abuse of notation for laser currents we use the same symbols as for photo diode currents I_0 and I_1.

2.2.3 Fiber

Optical fibers are used as a wave guide for frequencies at several 100 THz. In vacuum this means a wavelength of e.g. 1300 nm or 1550 nm. Their main advantages are the extremely low attenuation (down to 0.18 dB/km), high immunity against interference and you get potential separation for free.

2.2.3.1 Types of fibers

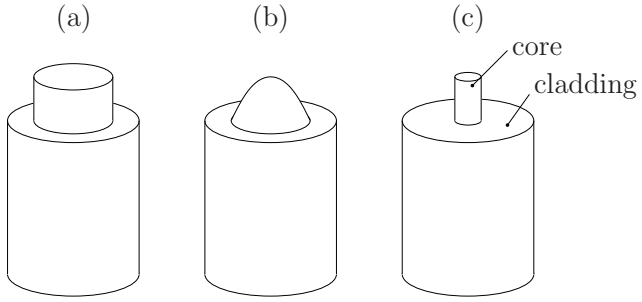
Cheap Fibers for short range communication (e.g. inside of cars or houses) are made of plastic (*Plastic Optical Fiber (POF)*). They have a core diameter of approximately 0.9 mm [Lee01]. Since they have bad properties, we will not consider them here. For professional optical communication the fibers are made of fused silica *Silicon dioxide (SiO_2)*.

There are three base types of fibers:

1. Step Index Multimode Fiber
2. Gradient Index Multimode Fiber
3. Singlemode Fiber

These types differ in their core diameters and the profiles of the *optical refraction index*. In Fig. 2.4 the index profiles are sketched. The fiber itself (as shown in the picture) is additionally covered in a plastic coating. In a *Multi Mode Fiber (MMF)*

Figure 2.4: Types of fibers. (a) Multimode Fiber; (b) Gradient Index Fiber; (c) Monomode Fiber



(with step index profile as well as gradient index profile) the electromagnetic wave can propagate inside the core with several modes. In a *Single Mode Fiber (SMF)* (also called a *Monomode Fiber*)[4] the propagation is only possible in a single mode. See Tab.2.1 for some representative data of these fibers. [Lee01]

[4]We use the abbreviation MMF for "multimode fiber" and SMF for "single mode fiber" here. Using "monomode fiber" would lead to undistinguishable abbreviations.

The index profile of the fiber produces *total internal reflection*. The light is reflected from one wall to the other and thus going zigzag through the fiber.

2.2.3.2 Applications

For very short range data transmission with low bit rates (up to 155 MBit/s) cheap MMFs with step index profile are used. Bit rates up to approximately 2.5 GBit/s are usually achieved with gradient index fibers. Distances of a few kilometers are possible. For high data rates (1 GBit/s and more) and very long distances (a few to thousands of kilometers) SMF are used.

2.2.3.3 Attenuation

The *attenuation* of an SiO_2 fiber is caused by loss of optical power in the material. There are three so called windows where absorption is at a minimum. These windows are at

850 nm ≈ 1 dB/km, cheap lasers available

1300 nm ≈ 0.3 dB/km, lowest dispersion

1550 nm ≈ 0.2 dB/km, lowest attenuation

The best fibers available have attenuation of 0.18 dB/km at 1550 nm. [Lee01], [Lee02] Fiber communication over very long distance (e.g. between two continents) uses fiber amplifiers. They directly amplify the optical power instead of digitally receiving bits and sending them again.

2.2.3.4 Data Rate

Today the maximum possible data rate to transmit via a fiber is only limited by the sender and receiver. This is true for very short distance transmission. For long fibers there are two possible effects limiting the data rate. In *attenuation*

Table 2.1: Types of fibers

	Unit	Multi Mode	Gradient Index	Single Mode
core diameter	μm	$50 \div 600$	50, 62.5	$4 \div 10$
cladding diameter	μm	$150 \div 1000$	$100 \div 200$	$100 \div 200$
bandwidth	GHz km	< 0.05	$0.2 \div 3$	$\gg 1$

limited systems the received signal power is very weak compared to the receiver noise. This SNR determines the BER. In *dispersion limited systems* the pulse deformation due to dispersion limits the maximum data rate.

The effects of dispersion and attenuation (measured in dB) linearly depend on the length of the fiber. Therefore the so called *bitrate-length product* is used. Typical values are noted in Tab. 2.1. Since the attenuation measured in dB depends linearly on the fiber length, the attenuation measured in linear units depends *exponentially* on the fiber length.

2.2.4 Photodiode

At the receiver the light pulses have to be transformed to electrical pulses. Therefore *photodiodes (PD)* are used. They convert the optical power to electrical current.

$$I(t) = R \cdot P(t) \tag{2.1}$$

The current is proportional to the incident optical power (=intensity). The *responsivity* R depends on the semiconductor material and the wavelength.

$$R = \frac{I}{P} = \eta \frac{e}{h\,f} = \eta \frac{e\,\lambda}{h\,c_0} \tag{2.2}$$

where $e = 1.602 \cdot 10^{-19}\,\mathrm{As}$ is the charge of a single electron, $h = 6.626 \cdot 10^{-34}\,\mathrm{Js}$ is Planck's constant and $c_0 = 300,000\,\mathrm{km/s}$ is light speed in vacuum, λ is the wavelength and η is the external quantum efficiency (see [Zim04b] and [Lee01]).

PDs utilize the *inner photo effect*. An absorbed photon with the energy $E = h\,f = \hbar\,\omega$ raises an electron from the valence band into the conduction band. This generates an electron–hole pair. To avoid recombination a high electric field is applied to the depletion layer. The generated electron-hole pair is seperated by the field and thus results in a current through the PD.

Figure 2.5: Electrical circuit with a photodiode

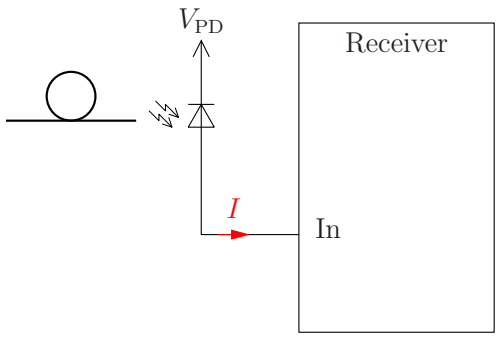


Figure 2.5 shows an electrical schematic. Photo diodes are operated with reverse bias. This means that the photo current is a reverse current through the diode.

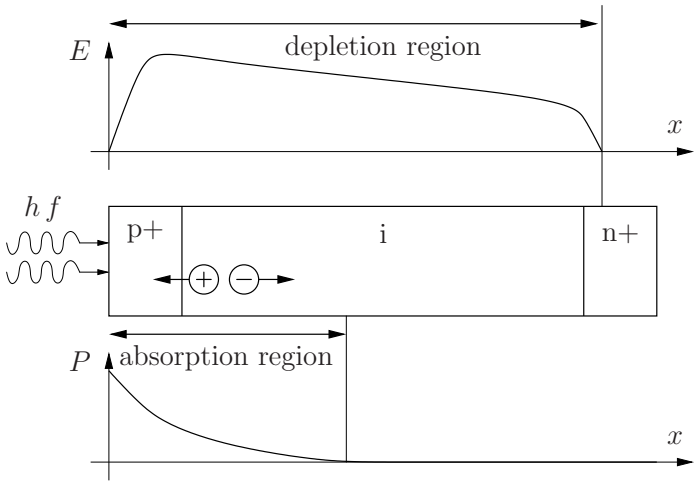
Typical materials for photodiodes are GaAs, InGaAs and Si. Unfortunately the band gap of Si limits its use to wavelengths below 1140 nm. Therefore ternary or quaternary PDs are used for wavelengths 1300 nm and 1550 nm (GaAs, InP, InGaAs [Zim04b]).

There are two basic types of photodiodes:

- PIN photodiodes
- Avalanche photodiodes (APD).

PIN photodiodes have an intrinsic region between the p- and n-doped regions. They are available for very high bit rates (40 GBit/s and more). In Fig. 2.6 the structure of a PIN PD is drawn. The electric field E is depicted at the top of the picture. It determines the position and extent of the *depletion region*, i.e. where no free electrons are available.

Figure 2.6: Structure of a PIN photodiode



The optical power P enters the PD at the left and is absorbed by the semiconductor because *photo generation* takes place. P's exponential decrease is shown in the bottom part of the picture. The region where photo generation takes place is denoted as *absorption region*.

In the depletion region a photo generated electron-hole-pair is instantly separated due to the high electric field. Both drift with high velocity (usually the saturation velocity is desired). If a pair was generated outside the depletion region it had to diffuse through the semiconductor. Since diffusion is a very slow process compared

to drift, this has to be avoided. Therefore the "i" region is used to extend the depletion region over the absorption region.

The bandwidth of a PIN-PD is determined by

1. electrical circuit (RC lowpass)
2. transit time in the depletion region
3. diffusion of the electron-hole-pairs generated outside the depletion region

The design of a photodiode has to find a tradeoff between the transit time through a long depletion region and the increased capacity of a short depletion region. [Lee01]

In the *Avalanche Photo Diode (APD)* the photo current is amplified by the avalanche effect. This is an internal low noise effect. The photo generated electrons are accelerated by the high electric field in the multiplication zone. Due to impact ionization additional electron-hole pairs are generated. Multiplication factors m of $4 - 10$ are achievable depending on the diode an the reverse bias vortage. The avalanche effect requires high supply voltage for the PD. APDs can be used with very low input power. Unfortunately they are only available for bit rates up to 2.5 GBit/s. [Lee01] and [Zim04b]

2.2.5 Amplifier

The (reverse) current from the photodiode is then fed into the electrical amplifier. The weak current (microampere) with very high bandwidth needs to be "boosted" to a level where the digital receiver can decide "0"s and "1"s.

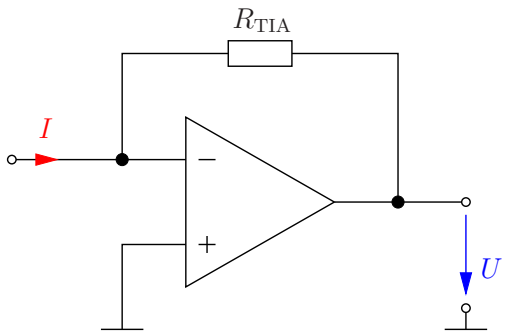
Amplifiers with an input current and an output voltage are called *Transimpedance Amplifiers (TIA)*. The most widely known example circuit is the inverting opamp circuit without the input resistor (see Fig. 2.7).

The most important properties of the input amplifier are *high bandwidth* and *low noise*. The input signal is the weakest signal in the amplifier chain. Thus the added noise has the largest impact on the signal quality. See als Sec. 3.3.4.

2.2.6 Slicer

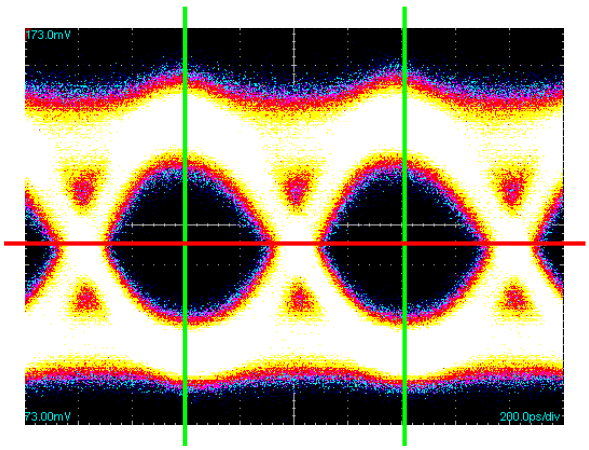
At the slicer the clock rate and phase as well as the data bits have to be recovered. This is called *Clock/Data Recovery (CDR)*. A discussion of clock recovery is out of the scope of this diploma thesis. For further discussion we assume the knowledge of the clock and phase at the receiver.

Figure 2.7: Opamp circuit as TIA



The slicer itself considers the received signal at clocked moments (see Fig. 2.8). Depending on the value whether it is above or below a certain threshold, the bit is decided to be a “0” or a “1”.

Figure 2.8: Slicer in the eye diagram. The sampling instants are marked with green lines. The threshold is shown with the red line.



If the noise floor of the signal causes the value to be at the other side of the threshold, a bit error has occurred. For optical data transmission bit error ratios (BER) as low as 10^{-9}, 10^{-10} or even 10^{-12} are desired (see Sec. 1.3.3).

2.3 Burst Mode

In *Passive Optical Networks (PONs)* between the sender and receiver there are only passive optical components. No active components (e.g. amplifiers, multiplexers, ...) are used. PONs are therefore cheap compared to other approaches.

This is especially interesting for consumer market and where many stations have to be connected via fiber optics (e.g. in a company's office).

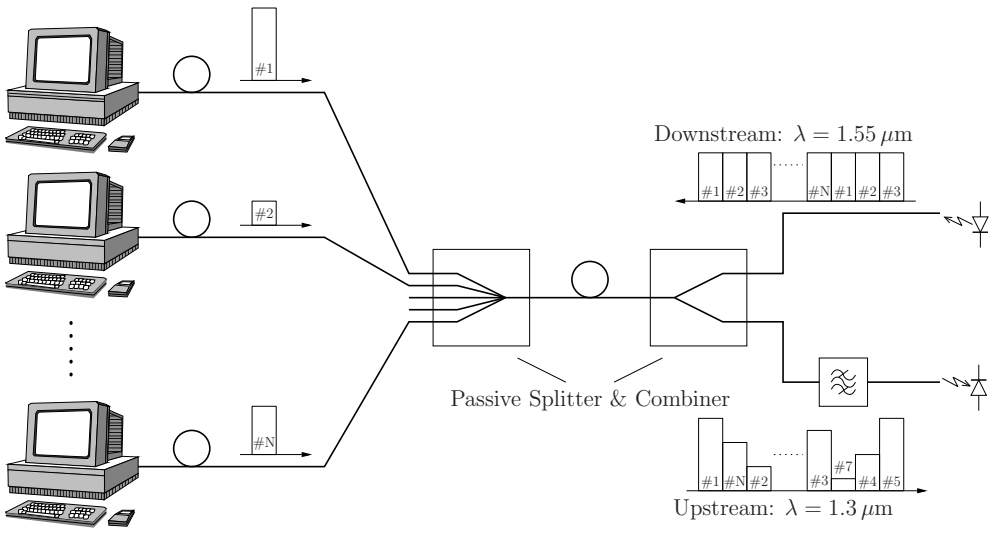
Think of a village where e.g. 1000 households have their PON connection. Using a bit rate of 2.5 GBit/s this is divided by the count of end stations. In our example every household gets a net bit rate of 2.5 MBit/sec. This is by far more than any Asymmetric Digital Subscriber Line (ADSL) or cable TV provider currently offers.

As drawn in Fig. 2.9 every computer is connected to the central office via a *single* fiber. Full duplex communication is accomplished by Wavelength Division Duplex (WDD). *Download* (referred to the end station, so data from the central station to the end station) utilizes $\lambda = 1.55\,\mu$m. *Upload* is done using $\lambda = 1.3\,\mu$m.

Before payload data is transmitted a higher level protocol assigns a time slot to each party. The central station continuously sends data. This is concurrently received by every end station. Every end station will only pick up data depending on its assigned time slot.

For the opposite direction of data (end station to central office) a *Medium Access Control (MAC)* mechanism is necessary. The "shared medium" is the (common) fiber in the central office and the receiver photodiode. The MAC is organized by TDMA. Every party is only allowed to send in its slot, all others have to switch off their lasers.

Figure 2.9: Schematic setup of a Passive Optical Network (PON).



One time slot (i.e. the time one station is allowed to talk) is only a few bits (approx. 400). To avoid too much overhead between two consecutive time slots, the time to switch off the laser of station #n and to switch on the laser of station #n+1 is limited to a short time.

The end stations might be spread within a little city. Therefore cable lengths to the central office may vary greatly. As discussed in Sec. 2.2.3.3 the signal attenuation measured in dB linearly depends on the fiber length. This means that the received signal power measured in Watt *exponentially* depends on the length.

To get high bit rate and high sensitivity the receiver in the central office has to adapt its gain depending on the input signal amplitude. Since a higher level protocol negotiates the order of the different end stations and their time slots, the central office already knows which party will send at a particular time slot. Therefore it easily can control the input amplifier's gain depending on the party.

The receiver's gain has to be switched very quickly. Only a few bits are allowed to be lost. Special circuits are necessary to accomplish this demanding task.

Note that a near station being quiet by sending "0"s would bias the weak signal from a far station due to the "dark" optical power P_0 more than the far station's signal amplitude!

3

Circuit Design

ANALOG circuit design is the main task of this diploma thesis. This chapter describes the employed components, some basic circuits, noise theory and properties of the semiconductor process. The information in this chapter is largely based on [GHLM01], [Zim04b], [Säc01] and [TS02].

3.1 Transistors

Transistors are the core components on semiconductors. They are mostly used as switches (especially in digital circuits) and as amplifiers. There are two types of transistors:

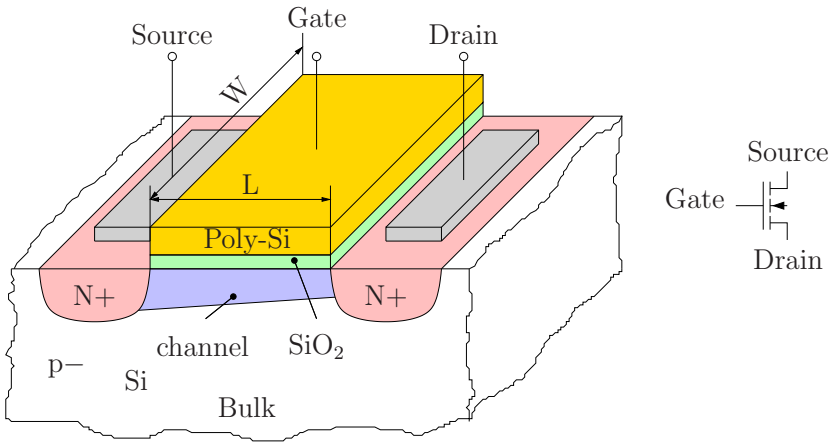
- bipolar junction transistors
- field effect transistors.

Both have specific properties and characteristics. Note that not necessarily all types are available in a particular semiconductor process. In this chapter we will only consider the field effect transistor because no Bipolar Junction Transistor (BJT) is used in the developed chip.

3.1.1 Field Effect Transistors

Field Effect Transistor (FET) conduct the current through a so called *channel* between the two connections "Source" and "Drain". The channel is controlled by an electric field applied with the "Gate". Figure 3.1 shows the profile of an N-MOS FET and its circuit symbol [TS02].

Figure 3.1: Profile of a FET



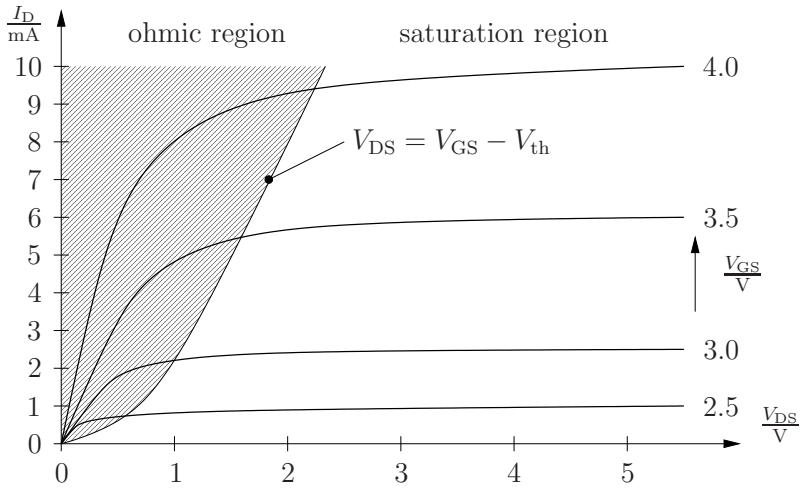
In the lightly P-doped silicon two N+ wells are doped for S and D. These are connected with metal layers. At the surface of the semiconductor between these wells a very thin so called *gate oxide* (SiO_2) is deposited. The gate contact itself is made out of a poly-silicon layer.

Two FET types are available: N-channel FETs and P-channel FETs. For the latter all N and P regions are exchanged. Besides this types there are *Metal Oxide Semiconductor Field Effect Transistor (MOSFET)* (with an insulated gate) as seen in Fig. 3.1 and *Junction Field Effect Transistor (JFET)*. For the latter there is no gate oxide, the (metal) gate is directly deposited to the channel so that a Schottky contact is formed. This Schottky diode is reverse biased and will deplete the available electrons from the surface. The channel between S and D is narrowed and separated for high (negative) gate voltages. Finally there are *enhancement mode* and *depletion mode* FETs. JFETs are only available in depletion mode whereas MOSFETs are available in both modes.

3.1.1.1 Characteristic

For further discussion we will use the NMOS FET. Figure 3.2 shows the output characteristic of a typical N-channel FET. The gate-source voltage V_{GS} controls the channel. Depending on the drain-source voltage V_{DS} the drain current I_D is conducted. Two regions are distinguishable. When $V_{DS} \leq (V_{GS} - V_{th})$ the FET

Figure 3.2: Output characteristic of an N-channel FET



is in the "*ohmic region*". The channel extends from source to drain and the FET behaves like a controllable ohmic resistor.

With increasing V_{DS} the voltage drop from D to S increases too. The local difference of the channel potential to the gate potential varies due to this voltage drop. This results in a non-equal depth of the channel (see Fig. 3.1). For $V_{DS} = (V_{GS} - V_{th})$ the channel depth at the drain approaches zero. This is the threshold to the "*saturation region*". For higher V_{DS} the channel does not extend over the full gate length. In this region the FET behaves as a current source.

3.1.1.2 Model

The output characteristic of a FET can be described by

$$I_D = \begin{cases} 0 & \text{for } V_{GS} < V_{th} \\ K\,V_{DS}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)\left(1 + \frac{V_{DS}}{V_A}\right) & \text{for } V_{GS} \geq V_{th},\ 0 \leq V_{DS} < V_{GS} - V_{th} \\ \frac{K}{2}\left(V_{GS} - V_{th}\right)^2\left(1 + \frac{V_{DS}}{V_A}\right) & \text{for } V_{GS} \geq V_{th},\ V_{DS} \geq V_{GS} - V_{th} \end{cases} \tag{3.1}$$

where

$$K = \mu\, C'_{ox}\, \frac{W}{L} \tag{3.2}$$

is the *transconductance coefficient* of the particular FET, μ is the *carrier mobility* in the channel and C'_{ox} is the *gate capacity* normalized to area. W and L are the channel dimensions as shown in Fig. 3.1. [TS02]

The first line of (3.1) reflects the cutoff region where the gate-source voltage is below the threshold voltage V_{th}. The second line models the ohmic region, when

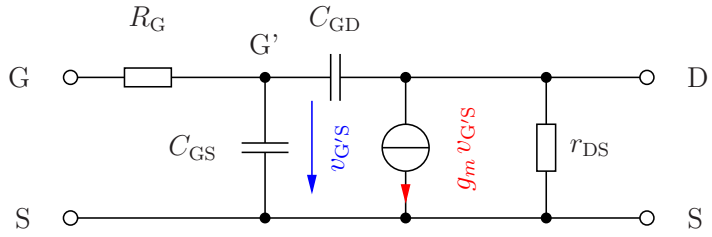
$V_{DS} \ll (V_{GS} - V_{th})$ its is approximately linear. In the third line the saturation region is described. The last term in parenthesis reflects the channel length modulation. For a continuous curve it also has to be considered in the ohmic region. The parameter V_A is called *Early voltage* and references the virtual intersection of the slopes in the saturation region at $-V_A$.

For MOSFETs the gate current I_G is zero because the insulating gate oxide prevents any (notable) current. For fast changing gate voltages (when used as AC amplifier) the gate capacity has to be charged or uncharged which nevertheless will require notable currents. The DC gate current of JFETs is given by the Shockley equation

$$I_{G,JFET} = I_{G,S}\left(e^{\frac{V_{GS}}{V_T}} - 1\right). \tag{3.3}$$

3.1.1.3 Small signal equivalent circuit

Figure 3.3: FET dynamic small-signal equivalent circuit



The dynamic small signal equivalent circuit is shown in Fig. 3.3. R_G denotes the gate connection resistance. The values for the transconductance g_m and for the output resistance R_{DS} in the saturation region are given by

$$g_m = \left.\frac{\partial I_D}{\partial V_{G'S}}\right|_O = \sqrt{2\,K\,I_{D,O}} \tag{3.4}$$

$$r_{DS} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_O = \frac{V_A}{I_{D,O}}. \tag{3.5}$$

Note that these equations are rough approximations. In the simulations of the developed chip BSIM[1] 3.3 and BSIM 4 MOSFET models where used.

The gate-source capacitance C_{GS} is mainly destined by the gate oxide material and thickness as well as the gate dimensions. The gate-drain capacitance C_{GD} results from the overlap between gate electrode and the drain well. Both capacities don't depend on the operating point.

[1] BSIM = Berkeley short-channel IGFET model

3.2 Amplifiers

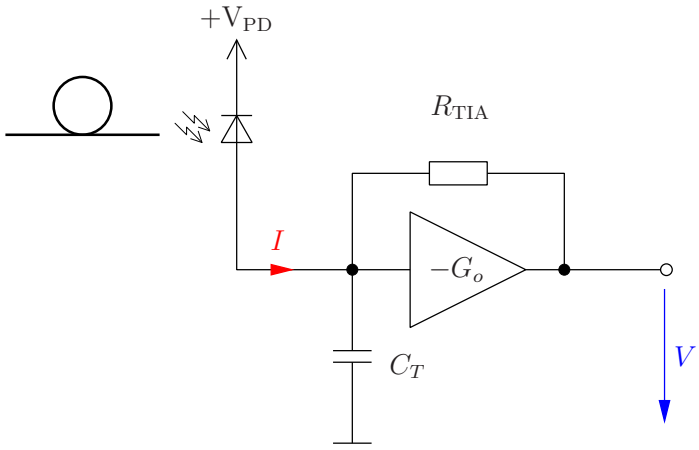
In the developed chip several amplifier circuits are employed. This section describes the basics of them. Most formulas here use small signal voltages and currents as opposed to the total values. Therefore they are written with lower case letters (e.g. i_C). Operating point (DC) values are written with an upper case letter and with an additional index "O" like $I_\mathrm{C,O}$. The total value (DC + small signal offset) is written with upper case letter and without the additional index "O" like I_C.

3.2.1 Transimpedance amplifier analysis

The (small signal) transfer function of a TIA with an ideal amplifier with gain $-G_o$ and a feedback resistor R_TIA (see Fig. 3.4) is given by

$$\frac{v}{i} = -\frac{G_o}{1+G_o}\frac{R_\mathrm{TIA}}{1+j\omega\frac{C_T R_\mathrm{TIA}}{1+G_o}}. \tag{3.6}$$

Figure 3.4: Transimpedance amplifier principal circuit



The total input capacitance $C_T = C_\mathrm{PD} + C_\mathrm{para} + C_\mathrm{in}$ sums up from the photodiode depletion capacity, parasitic capacities (e.g. bond pads, package, ...) and the amplifier input capacity. R_TIA and C_T form a first order low pass which limit the bandwidth of this circuit to

$$f_\mathrm{c,3dB} = \frac{1+G_o}{2\pi\, R_\mathrm{TIA}\, C_T}. \tag{3.7}$$

The circuit topology with the amplifier reduces the input impedance by a factor of $1+G_o$ compared to a passive RC low pass and thus increases the bandwidth by the same amount.

In the above consideration an ideal amplifier with infinite bandwidth or at least a bandwidth much larger than given by (3.7) was assumed. If $G_o(j\omega)$ starts to decrease at frequencies below $\omega_{\mathrm{c,3dB}} = 2\pi f_{\mathrm{c,3dB}}$ the total circuit bandwidth also decreases. Assuming an amplifier with the transfer function of a first order low pass

$$G(j\omega) = \frac{G_o}{1 + jG_o\frac{\omega}{\omega_T}} \tag{3.8}$$

with a very high low frequency open loop gain $G_o \gg 1$ and transit frequency ω_T the transfer function of the total TIA is given by

$$\frac{v}{i} = -\frac{R_{\mathrm{TIA}}}{1 + j\omega\left(\frac{C_T R_{\mathrm{TIA}}}{G_o} + \frac{1}{\omega_T}\right) - \omega^2 \frac{C_T R_{\mathrm{TIA}}}{\omega_T}}. \tag{3.9}$$

This second order low pass function can lead to ringing and gain-peaking especially when photodiodes high capacity are used (see curves A ($C_T = 0.5\,\mathrm{pF}$) and B ($C_T = 2\,\mathrm{pF}$) in Fig. 3.5). This effect can be abandoned by adding a feedback capacitor C_{TIA} in parallel to R_{TIA}. Two values of this capacitor are evaluated in Fig. 3.5 as curves C ($C_T = 2\,\mathrm{pF}$, $C_{\mathrm{TIA}} = 10\,\mathrm{fF}$) and D ($C_T = 2\,\mathrm{pF}$, $C_{\mathrm{TIA}} = 30\,\mathrm{fF}$). In the designed TIA no extra C_{TIA} was inserted because the parasitic capacities are enough.

A typical TIA circuit example is shown in Fig. 3.6. The gain is provided by the transistor T_1 operated in common source configuration (see Sec. 3.2.3). T_2 is used as source follower (Sec. 3.2.5) for high output drive capability. The feedback resistor R_{TIA} is connected between the output and the input. Note the parallels to the circuit in Fig. 3.4.

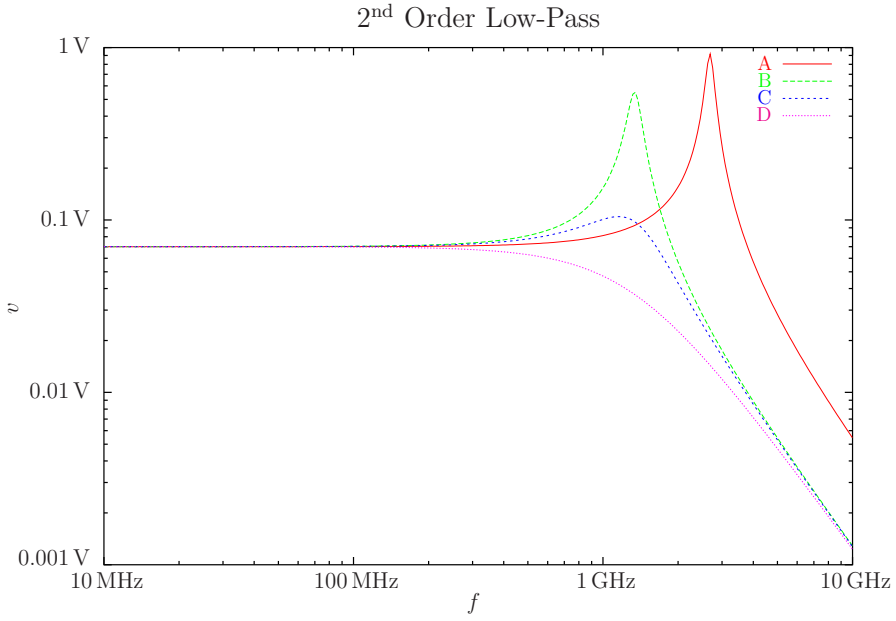
3.2.2 CMOS Inverter

A *CMOS inverter* (Fig. 3.7) has a very steep characteristic when both FETs are conducting. The operating point must be chosen to lie in this region. Very high gain ($\gtrsim 10$) up to high frequencies with very low input current is possible. The disadvantage is the high current from V_{DD} to V_{SS} in this operating point (but this yields low noise and is thus desired). Digital CMOS circuits use the same inverters but strive for a fast transition through the high current region.

3.2.3 Common source

The common source circuit is depicted in Fig. 3.8. The gain is $G = -g_m\left(r_{\mathrm{DS}}||R_{\mathrm{D}}\right)$. [TS02] It is easily visible that it depends on the operating point (g_m) and it is proportional to the drain resistor R_{D} in parallel with the FET output resistance r_{DS}. Replacing R_{D} with a current source (which has infinite small signal resistance) increases the gain to $G = -g_m\, r_{\mathrm{DS}}$.

Figure 3.5: Frequency response of second order lowpass according to (3.9): $R_{\mathrm{TIA}} = 7\,\mathrm{k\Omega}$, $G_o = 1000$, $\omega_T = 1000\,\mathrm{GHz}$, $i = 10\,\mu\mathrm{A}$; (A) $C_T = 0.5\,\mathrm{pF}$; (B) $C_T = 2\,\mathrm{pF}$; (C) $C_T = 2\,\mathrm{pF}$, $C_{\mathrm{TIA}} = 10\,\mathrm{fF}$; (D) $C_T = 2\,\mathrm{pF}$, $C_{\mathrm{TIA}} = 30\,\mathrm{fF}$ where C_{TIA} is in parallel to R_{TIA}.



This current source could be a PMOS FET with adjustable gate voltage. Its output resistance is only limited by the Early effect. Additionally the current and thus the operating point of the common source circuit can be adjusted.

3.2.4 Differential Amplifier

Figure 3.9 shows the schematic of a simple *differential amplifier*. The basic principle is the common source of both FETs and the current summation point $I_0 = I_1 + I_2$. The differential amplifier amplifies the *difference* between its input voltages $V_{\mathrm{in}} = V_{\mathrm{in,p}} - V_{\mathrm{in,n}}$ independent of the common mode voltage $V_{\mathrm{cm}} = \frac{V_{\mathrm{in,p}}+V_{\mathrm{in,n}}}{2}$ (when V_{cm} is within certain limits).

3.2.5 Source Follower

The *source follower* circuit is the *common drain* base circuit (see Fig. 3.10). It provides low output resistance and is thus used to drive heavy loads. Unfortunately its voltage gain is slightly less than one. It is also used as a level shifter.

Figure 3.6: Example of a FET transimpedance amplifier

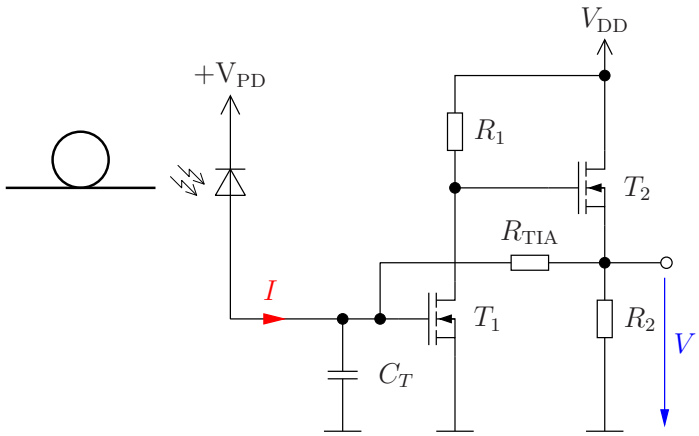
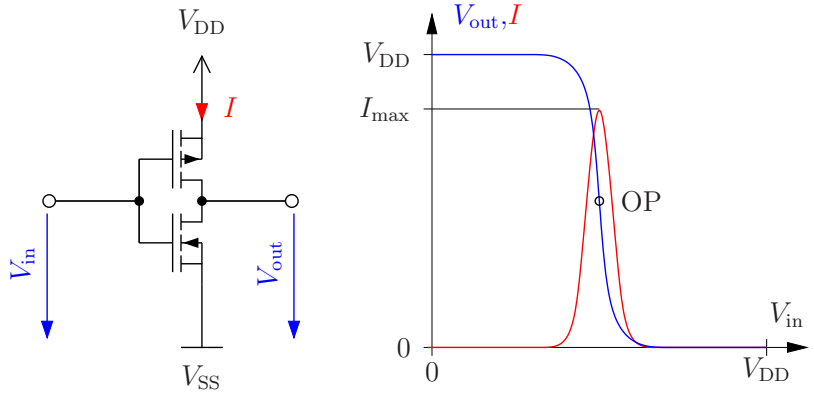


Figure 3.7: CMOS inverter as amplifier



3.3 Noise Theory

Noise is an ubiquitous phenomenon in electrical circuits. It disturbs the wanted signal and thus decreases signal quality. The noise amplitude (or alternatively its power) determines the minimum detectable signal.

3.3.1 Resistor noise source

Integrated and discrete metal-film resistors only display thermal noise. This is generated by random motion of the electrons in the resistor. The noise voltage or current generators for a resistor R are given by

$$\overline{v_{\mathrm{n,R}}^2} = 4\,k\,T\,\Delta f\,R \tag{3.10}$$

Figure 3.8: Common source circuit

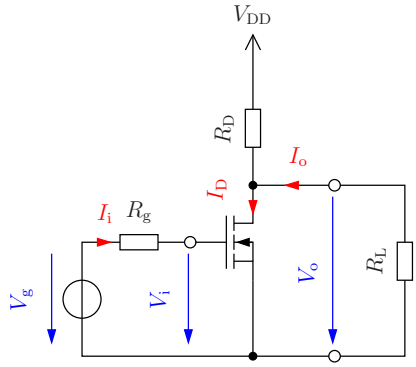
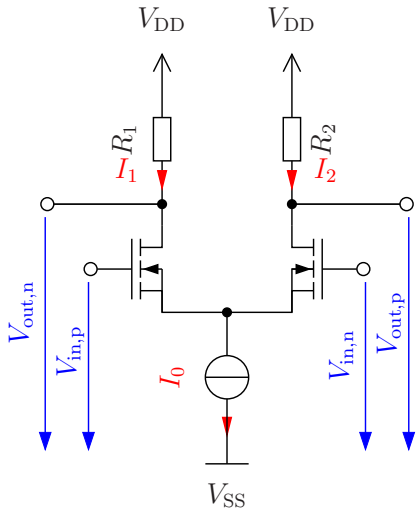


Figure 3.9: Differential amplifier



$$\overline{i^2_{n,R}} = 4\,k\,T\,\Delta f\,\frac{1}{R} \tag{3.11}$$

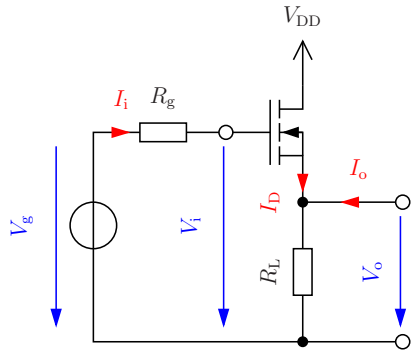
where $k = 1.38 \cdot 10^{-23}$ J/K is Boltzmann's constant and T is the absolute temperature in Kelvin. The noise is represented by either the voltage source $\overline{v^2_{n,R}}$ in series to the resistor *or* the current source $\overline{i^2_{n,R}}$ in parallel to the resistor.

3.3.2 FET noise sources

Field effect transistors reveal three important sources of noise. [TS02], [GHLM01]

1. Thermal noise of the resistive channel. Note that the small signal conductivity g_m is reduced by a factor of 2/3 (valid for Si MOSFETs operated in

Figure 3.10: Common drain circuit



saturation region) because the channel is neither homogeneous nor in thermal equilibrium. This noise contribution is white due to its thermal origin.

$$\overline{i^2_{n,D,1}} = 4\,k\,T\,\Delta f\left(\frac{2}{3}g_m\right) \tag{3.12}$$

2. Flicker noise in the channel. The current through the channel is conducted near the surface where traps can capture and release electrons. Flicker noise is also called $1/f$ noise and is dominant at low frequencies.

$$\overline{i^2_{n,D,2}} = K_{1/f}\frac{I_D^\alpha}{f}\,\Delta f \tag{3.13}$$

The parameters $K_{1/f}$ and α depend on the particular device.

3. Because of the capacitive coupling between the channel and the gate electrode the thermal noise in the channel induces fluctuations of the gate current. This is modeled by

$$\overline{i^2_{n,G}} = \frac{16}{15}k\,T\,\omega^2\,C^2_{GS}\,\Delta f \tag{3.14}$$

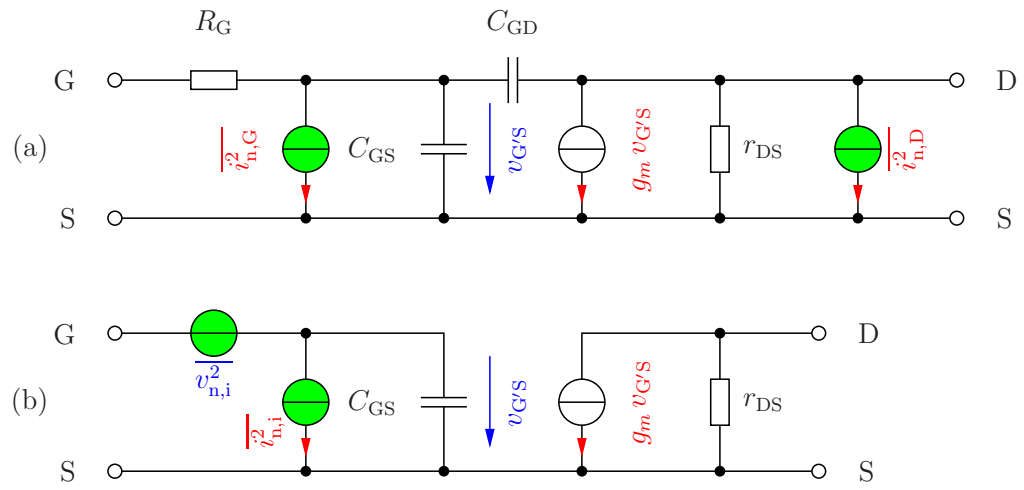
For channel lengths below $1\,\mu$m the factor 16/15 must be chosen higher because of hot electron effects. This noise source is correlated to $\overline{i^2_{n,D,1}}$ because both result from the same thermal noise.

The sources $\overline{i^2_{n,D,1}}$ and $\overline{i^2_{n,D,2}}$ are uncorrelated and therefore can be merged to a single noise source

$$\overline{i^2_{n,D}} = \overline{i^2_{n,D,1}} + \overline{i^2_{n,D,2}}. \tag{3.15}$$

Figure 3.11a shows the dynamic small signal equivalent ciruit of a FET with the noise sources (filled green) as calculated above. These sources can be referred

Figure 3.11: FET dynamic small-signal equivalent circuit with noise sources: (a) with original noise sources; (b) with input referred noise sources.



back to the input as shown in Fig. 3.11b. In the following calculation the gate resistance R_G and the gate drain capacity C_{GD} are negleted.

The input referred noise sources $\overline{v^2_{n,i}}$ and $\overline{i^2_{n,i}}$ are calculated by making circuit (b) equivalent to circuit (a) with their outputs short circuited. For the derivation of $\overline{v^2_{n,i}}$ we short circuit the *input* of both circuits as well and obtain $\overline{i^2_{n,D}} = g_m^2\,\overline{v^2_{n,i}}$. This yields

$$\frac{\overline{v^2_{n,i}}}{\Delta f} = 4\,k\,T\frac{2}{3}\frac{1}{g_m} + K_{1/f}\frac{I_D^\alpha}{g_m^2\,f}. \tag{3.16}$$

To derive $\overline{i^2_{n,i}}$ we open-circuit the input of both circuits in Fig. 3.11. The noise current in the short circuited output of both circuits must be equal $i_{n,i}\frac{g_m}{j\omega C_{GS}} = i_{n,G}\frac{g_m}{j\omega C_{GS}} + i_{n,D}$. The input referred current noise root-mean value is thus $\overline{i^2_{n,i}} = \overline{i^2_{n,G}} + \frac{\omega^2 C_{GS}^2}{g_m^2}\overline{i^2_{n,D}}$. Substituting (3.15), (3.12), (3.13) and (3.14) the input referred current noise is given by

$$\frac{\overline{i^2_{n,i}}}{\Delta f} = \frac{16}{15}k\,T\,\omega^2\,C_{GS}^2 + \frac{\omega^2 C_{GS}^2}{g_m^2}\left(4\,k\,T\frac{2}{3}g_m + K_{1/f}\frac{I_D^\alpha}{f}\right). \tag{3.17}$$

In this derivation we see that the current gain of the FET is given by $G_i = \frac{g_m}{\omega C_{GS}}$. The output noise current source $\overline{i^2_{n,D}}$ is divided by the square of this factor when referred back to the input. This is why for low frequencies the noise is very small and only determined by the (neglected) gate resistor R_G. For high source impedance – where $\overline{v^2_{n,i}}$ can be neglected — the noise performance of MOSFETs is much superior to that of bipolar transistors. Note that for low impedance

sources $\overline{v_{\mathrm{n,i}}^2}$ is dominant and due to the higher g_m BJTs are often superior there. [GHLM01]

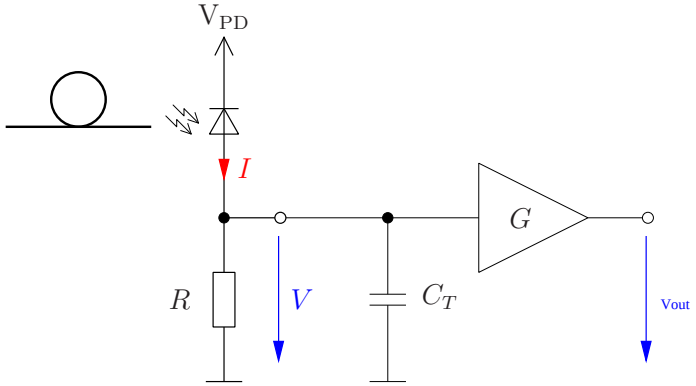
From the second term in (3.17) it is clear that noise can be minimized by maximizing g_m (see (3.4)). This is accomplished by high drain current in the operating point $I_{\mathrm{D,O}}$. Unfortunately $I_{\mathrm{D,O}}$ enters only by the square root into g_m so increasing $I_{\mathrm{D,O}}$ is not very efficient. The input referred noise also has a strong dependency on the frequency ω and the input capacity C_{GS}. This is due to the back-translation of the frequency independent drain noise current $\overline{i_{\mathrm{n,D}}^2}$ to the input via the capacitor C_{GS}.

3.3.3 TIA Noise

3.3.3.1 PIN-FET Amplifier

The output of the PD is a current proportional to the received optical power (see (1.3)) which has to be converted to a voltage. The simplest circuit for this conversion is a resistor R followed by an amplifier G (see Fig. 3.12).

Figure 3.12: Current to voltage conversion with a resistor

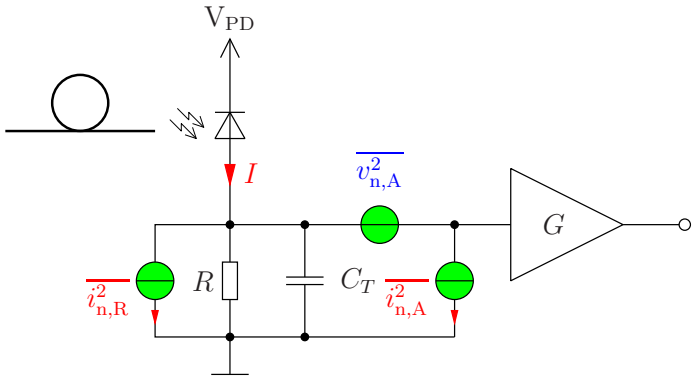


The total input capacitance $C_T = C_{\mathrm{PD}} + C_{\mathrm{para}} + C_{\mathrm{in}}$ is given by the sum of the photodiode depletion capacitance, parasitic capacities (e.g. bond pads, package, ...) and the amplifier input capacity. R and C_T form a first order lowpass which limit the bandwidth of this circuit to

$$f_{\mathrm{c,3dB}} = \frac{1}{2\pi\, R\, C_T}. \tag{3.18}$$

The resistor R can either be chosen rather low or rather high. For the low impedance case we use $R = 50\,\Omega$ as an example which yields a bandwidth of $f_{\mathrm{c,3dB}} = 1.59\,\mathrm{GHz}$ when $C_T = 2\,\mathrm{pF}$. Choosing $R = 7\,\mathrm{k}\Omega$ in the high impedance

Figure 3.13: Noise sources for a resistor with amplifier



case leads to an unusable bandwidth of $f_{\mathrm{c,3dB}} = 11.4\,\mathrm{MHz}$ with the same capacitance.

The noise sources for the amplifier circuit in Fig. 3.12 are shown in Fig. 3.13. $\overline{i_{\mathrm{n,R}}^2}$ is the current noise from the resistor R and $\overline{i_{\mathrm{n,A}}^2}$ and $\overline{v_{\mathrm{n,A}}^2}$ are the noise sources of the amplifier. The shot noise originated from the photodiode is neglected in this examination. The input referred current noise is easily calculated as

$$\overline{i_{\mathrm{n,i}}^2} = \overline{i_{\mathrm{n,R}}^2} + \overline{i_{\mathrm{n,A}}^2} + \frac{1+\omega^2 C_T^2 R^2}{R^2}\,\overline{v_{\mathrm{n,A}}^2}. \tag{3.19}$$

Since the thermal noise generated by the resistor is inversely proportional to the resistance R (see (3.11)) we have to choose a R as high as possible. Unfortunately the bandwidth is inversely proportional to R too resulting in competing design criteria for the resistor.

A very simple amplifier for the above task is the common source circuit shown in Sec. 3.2.3, the so called *PIN-FET amplifier*. The amplifier noise sources are then given by the FET input referred noise sources (3.17) and (3.16) with C_{GS} substituted by the total input node capacity C_T. Neglecting the channel induced gate noise current $\overline{i_{\mathrm{n,G}}^2}$ (see (3.14)) the total input referred noise current is [SZ01]

$$\begin{aligned}
\frac{\overline{i_{\mathrm{n,i}}^2}}{\Delta f} &= \frac{4\,k\,T}{R} + \frac{\omega^2 C_{\mathrm{T}}^2}{g_m^2}\left(4\,k\,T\frac{2}{3}g_m + K_{1/f}\frac{I_{\mathrm{D}}^{\alpha}}{f}\right) \\
&\quad + \frac{1+\omega^2 C_T^2 R^2}{R^2 g_m^2}\left(4\,k\,T\frac{2}{3}g_m + K_{1/f}\frac{I_{\mathrm{D}}^{\alpha}}{f}\right) \\
&= \frac{4\,k\,T}{R} + \left(\frac{\omega^2 C_T^2}{g_m^2} + \frac{1+\omega^2 C_T^2 R^2}{R^2 g_m^2}\right)\left(4\,k\,T\frac{2}{3}g_m + K_{1/f}\frac{I_{\mathrm{D}}^{\alpha}}{f}\right) \\
&\approx 4\,k\,T\left(\frac{1}{R} + \frac{4}{3}\frac{\omega^2 C_T^2}{g_m}\right)
\end{aligned} \tag{3.20}$$

where in the last line $g_m R \gg 1$ was assumed and the channel flicker noise was neglected. Especially for high frequencies the noise current is proportional to $\overline{i_{\mathrm{n,i}}^2} \sim \frac{C_T^2 f^2}{g_m}$. Thus for high sensitivity we have to minimize the input node capacity by shrinking the gate, eliminating parasitic elements and using a photodiode with small capacity i.e. operated at high reverse bias.

Additionally g_m needs to be maximized by increasing the DC drain current. The transconductance g_m of a FET is given by (3.4). Another equation relates it to the transit frequency f_T

$$g_m \approx 2\pi f_T C_{\mathrm{GS}}. \tag{3.21}$$

Thus, maximizing g_m also means increasing C_{GS} which is a contrary requirement to the previous paragraph. The minimum of the term $(C_T^2 f^2)/g_m \sim (C_{\mathrm{PD}} + C_{\mathrm{para}} + C_{\mathrm{GS}})^2/C_{\mathrm{GS}}$ has a minimum when

$$C_{\mathrm{GS}} = C_{\mathrm{PD}} + C_{\mathrm{para}}. \tag{3.22}$$

Therefore the design criteria for the front end FET in the TIA is to match its gate source capacity to the capacity of the photodiode plus the parasitic capacities. [Säc01]

In Fig. 3.14 the current noise spectral density of a TIA is shown. The three section, $\frac{1}{f}$ noise for low frequencies, frequency independent noise in the medium frequency range and f^2 noise for high frequencies are pointed out.

Figure 3.14: TIA noise spectral density

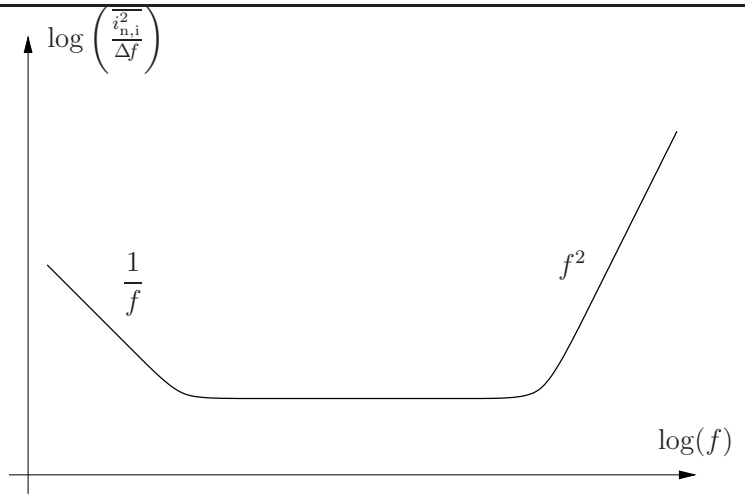
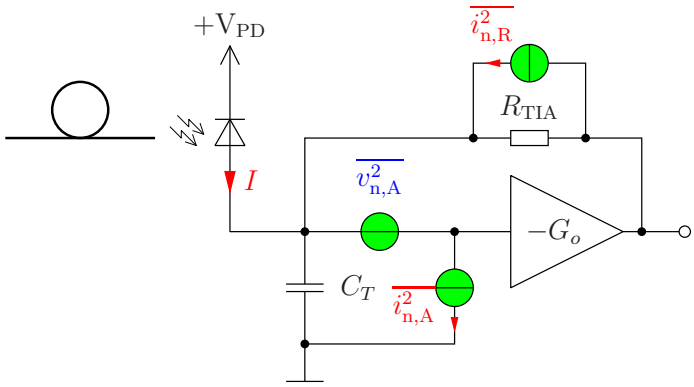


Figure 3.15: Transimpedance amplifier principal circuit with noise sources



3.3.3.2 Transimpedance Amplifier

Next we consider a plain TIA as shown in Sec. 3.2.1. The noise sources for this circuit are depicted in Fig. 3.15. The input referred noise for this circuit is then given by the same formula as for the PIN-FET amplifier

$$\overline{i^2_{\mathrm{n,i}}} = \overline{i^2_{\mathrm{n,R}}} + \overline{i^2_{\mathrm{n,A}}} + \frac{1+\omega^2 C_T^2 R_{\mathrm{TIA}}^2}{R^2}\,\overline{v^2_{\mathrm{n,A}}}. \tag{3.23}$$

From this result no improvement of noise performance is visible but Equ. (3.7) shows that the bandwidth of the TIA circuit is improved by a factor of $1 + G_o$ which allows to increase the feedback resistor by this factor to realize the same bandwidth. The higher feedback resistor will then emit less noise current which is considerable in the medium frequency range.

3.3.3.3 FET Transimpedance Amplifier

The FET-TIA as shown in Fig. 3.6 emits an input referred noise current

$$\begin{aligned}\overline{i^2_{\mathrm{n,i}}} &= \overline{i^2_{\mathrm{n,R}}} + \overline{i^2_{\mathrm{n,A}}} \\ &= 4\,k\,T\frac{1}{R_{\mathrm{TIA}}+R_2}\Delta f + \overline{i^2_{\mathrm{n,A}}}\end{aligned} \tag{3.24}$$

where $\overline{i^2_{\mathrm{n,A}}}$ again is the input referred noise current of the amplifier, i.e. the FET T_1. $\overline{v^2_{\mathrm{n,A}}}$ is negligible because of the high-impedance source. This result is the same as found for the PIN-FET amplifier before (cf. (3.19)) as shown in [Zim04b] and [GHLM01] except that the sum of $R_{\mathrm{TIA}} + R_2$ decreases the thermal noise compared to the PIN-FET amplifier although R_2 is usually much small than R_{TIA}. Because of this similarity the PIN-FET noise analysis can be used as an estimation for the FET TIA.

Using other amplifier topologies the gain can be increased which decreases the input referred noise current. In this work a CMOS inverter with high gain and low noise is utilized.

3.3.3.4 Summary

The most important requirement of an optical receiver is lowest input noise achievable at a the specified bandwidth. The noise sources of FETs have been discussed. Furthermore the input referred noise of the PIN-FET amplifier was calculated and a design criteria to minimize its noise was derived. A general TIA structure was considered and finally the input referred current noise of the FET TIA was found to be approximately equal to the PIN-FET amplifier. The advantage of the FET TIA is the lower input impedance which allows a higher transimpedance at the same bandwidth.

3.3.4 Noise Figure

The *noise figure* is a convenient way to specify the noise performance of amplifiers. It is commonly used in microwave circuit design. The noise figure F is defined as

$$F = \frac{\text{input SNR}}{\text{output SNR}} \tag{3.25}$$

and usually given in decibels. The minimum (i.e. optimum) noise figure is $F = 1 = 0\,\text{dB}$.

The noise figure of a series of amplifiers (and attenuators) can be calculated from their gain (or attenuation) and their input and output resistance. For simplicity we assume that all amplifiers as well as the source and the load are matched. This yields a very simpe result for the total noise figure

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_2} + \cdots \tag{3.26}$$

where F_x and G_x are the noise figure and the gain of the x-th amplifier respectively.

To optimize the total noise figure of a series of amplifiers, the conditions can be derived from the above formula:

- minimize the noise figure of the first amplifier F_1
- maximize the gain of the first amplifier G_1.

This is intuitively clear because the noise generated in a "later" part of the circuit is divided by the gain of the previous amplifiers when referred back to the input. [TS02]

3.4 C11N Process

3.4.1 Process properties

The developed amplifier will be included on a mixed signal transceiver chip as final product. This final chip contains large digital portions. For low costs the final chip will be manufactured in a standard digital CMOS process. The developed analog amplifier has to be built and thus developed and optimized for the same process.

Infineon's "C11N" digital deep sub-μm CMOS process with 120 nm feature size is used. The process has some analog extensions (FETs with higher and lower V_{th}, ...) but these have not been utilized in the developed chip to minimize the cost of the final design.

For metallization 6 *copper* layers are used. The two topmost layers are built thicker for higher currents.

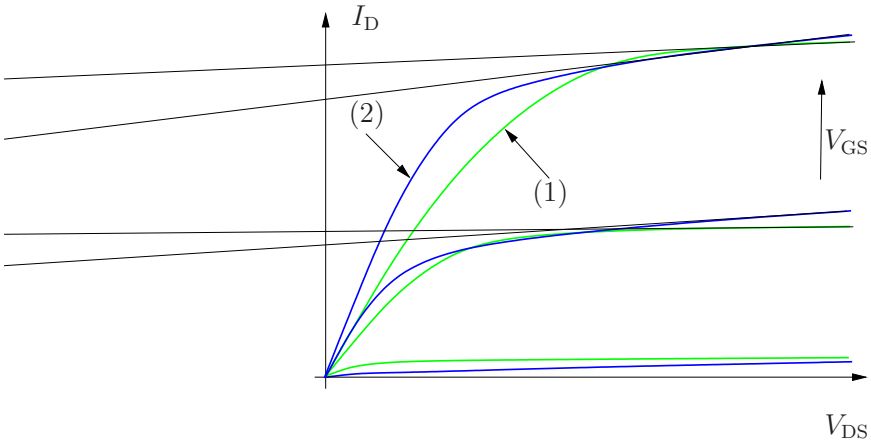
3.4.2 Integrated Components

The process provides enhancement mode NMOS and PMOS transitors. The substrate is slightly P-doped and connected to V_{SS} what enables NMOS FETs being directly implemented. PMOS transistors need an N-well which must be doped additionally. The potential of this N-well can be chosen freely and is usually connected to the source to avoid the *back-gate effect*. This is not possible for NMOS transistors due to the fixed potential of the substrate.

The Early voltage of FETs decreases with the smaller channel length. In Fig. 3.16 two typical NFET characteristics are shown. The green curves (1) show an NFET with $L = 560\,\mathrm{nm}$. Thin black lines extend the slope of the curve in the saturation region towards negative numbers. An NFET with $L = 120\,\mathrm{nm}$ is depicted as blue curves (2) (both characteristics are normalized to approximately constant maximum drain current). From this figure it is clear that short FETs are particularly bad for analog circuits due to their low Early voltage. The usual assumption of a drain current I_{D} approximately independent of V_{DS} is wrong which results in a very low small signal output resistance r_{DS} (see (3.5)).

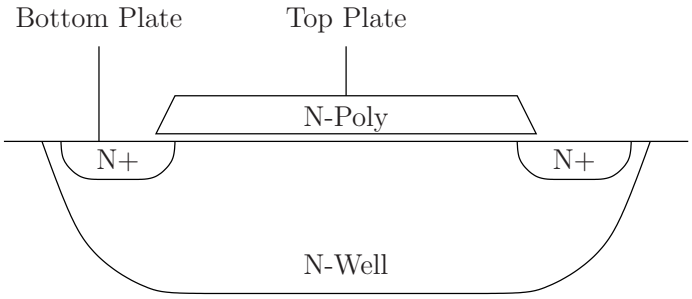
In the semiconductor process ohmic resistors as well as capacitors are available. *Resistors* are implemented as thin and long metal paths or paths of poly-silicon often wound as meander. *Capacitors* are implemented as two parallel metal planes. For very high capacities the gate dielectric is used. Therefore an NMOS FET like structure within an N-well is built. This N-well is one plate of the capacitor and contacted similar to source and drain. The second plate is the (large) polysilicon gate electrode. The waver substrate is slightly P-doped and

Figure 3.16: Early effect of two NMOS FETs with channel length (1) 560 nm and (2) 120 nm



connected to V_{SS} enabling the N-well to have any potential greater 0 V due to the reverse biased PN-junction.

Figure 3.17: NFET-in-N-well Capacitor



Large process variations in this process are no problem for digital circuits. For analog circuits these variations have a bad influence. The saturation current of a FET can vary up to ±24 % between different chips at constant V_{GS} and V_{DS}. Resistor values vary by ±10 % to ±15 % and capacitors vary by ±13 %. This complicates the design of the chip. The high demands outlined in Sec. 1.3 are only achievable with careful and tedious optimization work.

3.4.3 Analog Circuits

In the final mixed signal chip digital *and* analog circuits are used. For high frequency applications a library with specialized components is provided. This "`rfcmos`" library contains NMOS and PMOS transistors with a special layout.

These FETs with their predetermined layout are characterized very carefully and accurate simulation models are provided.

Unfortunately the FETs of the `rfcmos` library can't be scaled as usually done for integrated circuit transistors. There are a few models with 120 nm, 180 nm, ... gate length L and a constant gate width W. For wider transistors multiple standard cells have to be connected in parallel.

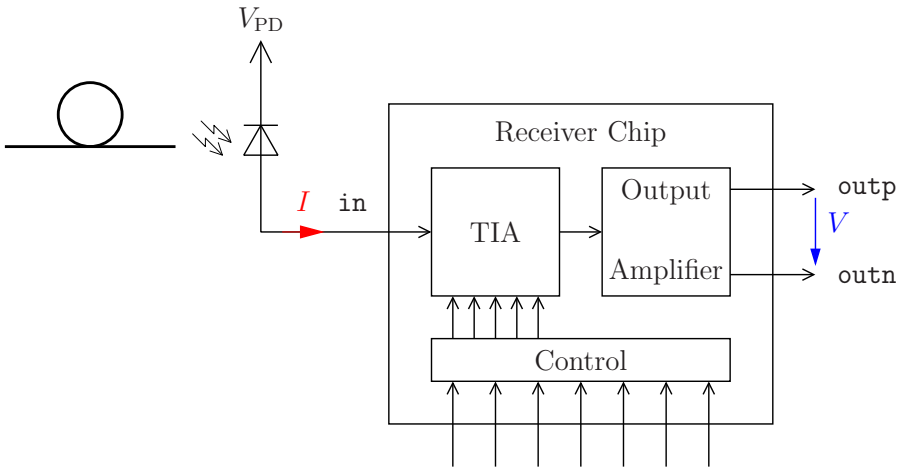
I want to emphasize again, that the designed analog chip is manufactured in a standard digital (deep-sub-μm-) CMOS process. No process options for better analog behaviour are employed. The only improvement is to use a special layout for the FETs.

4

Semiconductor Chip

BURST Mode Receivers for PONs (see Sec. 2.3) require a powerful input amplifier. In this diploma thesis the design of such an amplifier is implemented. The basic structure of the designed chip and its surrounding peripherals is depicted in Fig. 4.1.

Figure 4.1: Basic structure of the chip



The transimpedance amplifier (TIA) is the interesting part. The output amplifier is only necessary for measurement and characterization of the TIA. Control voltages are applied to the TIA by the control block.

This chapter is designated to describe the chip. In the first section the specifications and requirements combined with the demands for the chip circuit are presented. Section two details the central part, the TIA. The third section treats of the Prepare and Hold circuit. In the next section the comparator and output amplifier are described. This is followed by the assembly of all parts to the complete chip. In the end of this chapter the used tools as well as some other approaches are shown.

Whenever “the chip” or “developed chip” is written, the acutally developed and produced chip is meant. “The final chip” refers to the desired end product where parts of the developed chip are included.

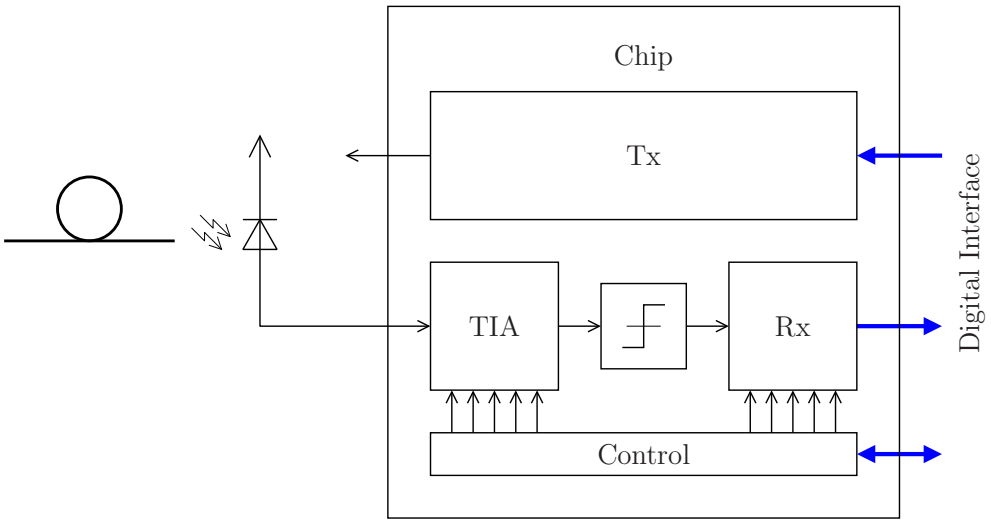
4.1 Structure

The TIA — which was developed within the scope of my diploma thesis — is the main field of interest. It will be embedded on a mixed signal chip. This is used for central office equipment of PON installations. This final mixed signal chip will contain

- the analog front end (TIA),
- a slicer,
- digital receiver,
- a transmitter and
- the control logic.

This structure is summarized in Fig. 4.2. This diploma thesis concentrates on

Figure 4.2: Basic structure of the final chip

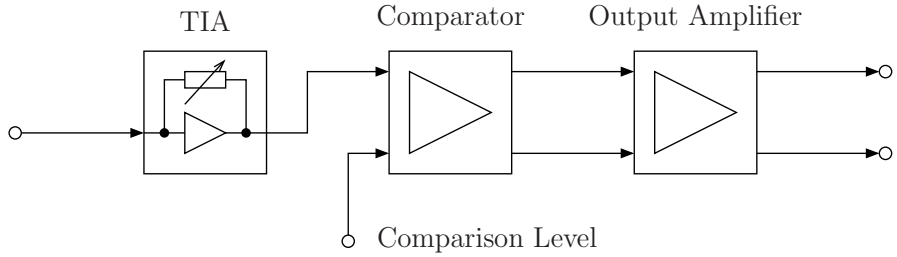


the development of the TIA. Its main function is to amplify the current through the PD and convert it to a voltage.

For its characterization special measurement instruments have to be connected to the outputs of the chip. For the high frequencies the TIA deals with, only 50 Ω interfaces are available. Strong output amplifiers are necessary to drive such a low-impedance load.

To improve substrate interference behavior, the output driver is implemented fully differential. Since the output signal of the TIA is single ended, a comparison with a reference level is built in. Figure 4.3 shows the amplifier chain on the developed chip.

Figure 4.3: Structure of the developed chip



4.1.1 Specification

In Sec. 1.3 the required characteristics of the developed chip are specified. Table 4.1 lists some typical values of $\overline{P}_{\text{opt}}$ and corresponding values of P_1, P_0, I_1 and I_0. (See section 1.3.2 or appendix B for explanations of the symbols.)

Table 4.1: Input power and current for typical values of $\overline{P}_{\text{opt}}$

$\overline{P}_{\text{opt}}$	P_1	P_0	I_1	I_0
194.0 μW = -7.1 dBm	352.7 μW	35.3 μW	300 μA	30.0 μA
5.0 μW = -23.0 dBm	9.1 μW	911.2 nW	7.7 μA	774.6 nA
2.0 μW = -27.0 dBm	3.6 μW	362.8 nW	3.1 μA	308.4 nA

4.1.1.1 Bit rate and Bandwidth

The specified bit rate is BR = 2.5 GBit/s. This implies very high frequency operation of the chip. The highest possible frequency occurs for a "01010101" data bit stream. Its period is $t = 2 \cdot t_{\text{Bit}} = 800\,\text{ps}$ what is equal to a frequency of $f = \frac{1}{t} = 1.25\,\text{GHz}$. For sharp edges of the data signal we need at least the next two harmonics at $3f$ and $5f$. The highest occurring frequency is then $f_{\max} = 5f = 6.25\,\text{GHz}$.

Unfortunately high analog bandwidth also increases the total output noise power. Since noise must be minimized (see the next section), high bit rate and low noise are competing demands. A good tradeoff for best BER is given by [Säc01]

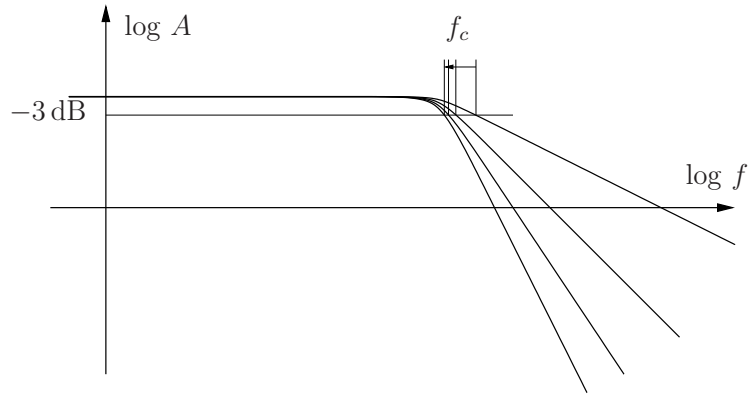
$$f_{\text{c,3dB}} = \frac{2}{3}\text{BR} = 1.67\,\text{GHz}. \tag{4.1}$$

The noise current spectral density $i^2_{\text{n,in}}(f)$ for high frequencies increases proportional to the square of the frequency f^2 as well as the square of the capacity at the TIA input C_T^2: $i^2_{\text{n,in}}(f) \sim f^2\, C_T^2$ (see Equ. (3.20)). Thus a higher bandwidth

will introduce even more noise. Additionally we have to keep the input capacity as low as possible. [Säc01]

Note that this is the bandwidth between the optical photodiode input and the slicer input. On the developed chip there is no slicer but a strong output amplifier. To be able to measure accurate BER the total chip is required to have a bandwidth of 1.67 GHz.

Figure 4.4: Cutoff frequency shift in a Bode plot



Several lowpass systems with equal bandwidth in series decrease the total bandwidth. This is easily understood when looking at the Bode diagram in Fig. 4.4. The −3 dB frequency is shifted to the left due to the overlaid Bode diagrams of the individual lowpass systems. The bend of every single system sums up to a sharper bend.

For a total 3 dB bandwidth of 1.67 GHz the individual parts of the chip need a higher bandwidth of approximately 2.5 GHz each. To achieve these high frequencies, the design of the chip must conform to special conditions, e.g. long paths between the amplifiers in the signal path introduce high ohmic resistivity and high capacity which form a lowpass reducing the total bandwidth aund thus must be avoided.

4.1.1.2 Sensitivity

The *sensitivity* of a receiver is specified as the required minimum average input power for a given BER. Clearly, the sensitivity heavily depends on the noise generated by the receiver itself. The higher the input referred noise current, the more input power is necessary for a given BER. See Sec. 1.3.3 for more explanation.

At the given mean optical input power $\overline{P}_{\mathrm{opt,min}} = -23\,\mathrm{dBm}$ the input current for "1" is 7.7 μA. A "0" is received with 0.7 μA (see Tab. 4.1). In Sec. 1.3.3 the

maximum RMS input referred current noise is calculated as $\sqrt{\overline{i_{\mathrm{n,in}}^2}} = 550\,\mathrm{nA}$ for a BER $= 10^{-10}$.

4.1.1.3 Switch the gain

As mentioned in Section 2.3 the input signal of the chip varies by about 20 dB. This results in a change of the input current of 40 dB or by a factor of 100 from $3\,\mu$A at -27 dBm to $300\,\mu$A at -7 dBm. The BMR has to change its gain according to the input power to avoid blocking.

The numerous parties sending their data to the central BMR alternate very quickly. Therefore the gain has to be switched very quickly too. The specification of the chip requires the gain to settle within $t_{\mathrm{switch}} = 1\,\mathrm{ns}$. Steep edges and high signal amplitudes occur inside the chip to achieve this requirement.

Layout implications to achieve fast switching include low stray capacitance, careful and optimized circuit design and good power supply decoupling.

4.1.1.4 Supply

The chip is supplied with $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$. For FET threshold voltages of $V_{\mathrm{th}} \approx 0.4\,\mathrm{V}$ (and because $V_{\mathrm{DS}} = V_{\mathrm{GS}} - V_{\mathrm{th}}$ is the threshold between ohmic region and saturation region, see Sec. 3.1.1.1) only three FETs between V_{DD} to V_{SS} are possible. Two FETs in series (e.g. for a differential amplifier, common-source circuit with transistor load, ...) are easier and yield better results. This constraint limits the possible circuits to use. For example no normal cascode circuit is possible.

Simulations have shown that gain switching is only fast enough if the supply of the TIA is very stable. This requires careful supply filtering and stabilizing capacitors. As we will see later, the supply capacitors consume most area of the chip.

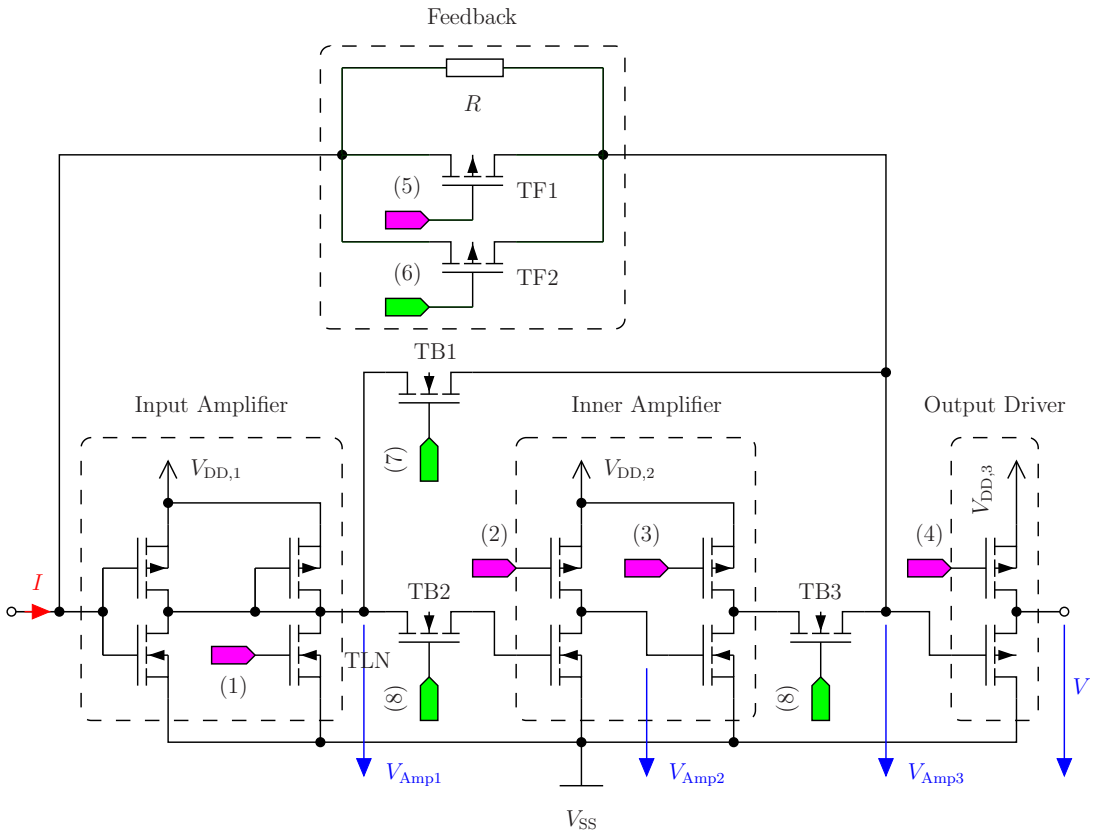
4.2 Transimpedance Amplifier

The *transimpedance amplifier* is the frontend circuit of the chip which is directly connected to the photodiode. For high input dynamic range its transimpedance needs to be adjustable. This is done by changing the feedback resistor R_{TIA}. Unfortunately for low transimpedance values the amplifiers is unstable. Therefore its open loop gain has to be reduced. This is accomplished by bypassing inner amplifier stages.

4.2.1 Schematic

The schematic of the realized TIA is shown in Fig. 4.5. The input current I enters on the left. The output voltage V exits at the right. The bottom parts are the amplifier stages. At the top the feedback network is shown.

Figure 4.5: Schematic of the developed TIA



For some FETs no bulk connection is drawn. All bulks of the NMOS transistors are connected to V_{SS}. This is the substrate contact too. The bulks of all PMOS which are not explicitly drawn are connected to one of the $V_{DD,x}$ supplies.

4.2.2 Control Voltages

Control voltages are applied at the green and magenta markers. Green markers denote *digital* control voltages. Magenta markers show *analog* control voltages. All these voltages are supplied by the Prepare and Hold circuits described in Sec. 4.3. These control voltages are used to adjust the transimpedance and the open loop gain of the TIA. Table 4.2 summarize the drawn control voltages. Detailed descriptions of every control voltage are provided in the next subsections.

4.2.3 Structure and function

In Fig. 4.5 the four main parts are marked with dashed lines. The left most part is the *input amplifier*. This is followed by the *inner amplifier*. The *feedback network* couples its output back to the input. It realizes the transimpedance of the amplifier. To unload the amplifier and drive the following stages the *output amplifier* is present.

Note: When "the TIA" or "the total TIA" is written, the total circuit as shown in Fig. 4.5 is meant. "The TIA itself" or "the actual TIA" always refers to the circuit without the output driver.

4.2.3.1 Feedback Network

The feedback network determines the amplifier's *transimpedance* R_{TIA}. It can be adjusted in a range of approximately $100\,\Omega$ to $7\,\mathrm{k}\Omega$. If both transistors TF1 and TF2 are switched off — that means they are in cut-off region — $R_{\mathrm{TIA}} = R$. The resistor R is produced as a poly-silicon resistor with nominal resistance of $R = 7\,\mathrm{k}\Omega$.

By applying the control voltage `V_C_FB` with values less than V_{DD} the transistor TF1 gets ohmic. Since it is connected in parallel to R the total transimpedance R_{TIA} decreases. To minimize R_{TIA} the second transistor TF2 is in place. It can only be switched on or off but no steps in between are possible.

4.2.3.2 Switches

As already mentioned above the input current varies by a factor of 100 — that are 40 dB. The transimpedance R_{TIA} has to vary for approximately the same order of magnitude for an output amplitude mostly independent of the received power.

Table 4.2: Control voltages as labeled in Fig. 4.5

Label	Name	A/D	Description
1	`V_C_Amp1`	A	Weaken gain of the input amplifier
2	`V_C_Amp2`	A	Adjust operating point of amplifier stage 2
3	`V_C_Amp3`	A	Adjust operating point of amplifier stage 3
4	`V_C_Amp4`	A	Adjust operating point of amplifier stage 4
5	`V_C_FB`	A	Adjust feedback resistor
6	`V_C_FBD`	D	Minimize feedback resistor
7	`V_C_BP`	D	Bypass the inner amplifier
8	$\overline{\texttt{V\_C\_BP}}$	D	Cut off the inner amplifier

The open loop gain of the amplifier must be reduced for lower transimpedance values to guarantee stability.

The approach used in the developed TIA is to bypass the inner amplifier. Only the gain of the input amplifier is left. Transistor TB1 connects the output of the input amplifier to the feedback network. To avoid disturbance from the inner amplifier, it is cut off with TB2 and TB3.

When switching from high transimpedance to minimum transimpedance, the feedback resistance is decreased. The gate voltages of the feedback transistors TF1 and TF2 are set to 0 V. The bypass transistor TB1 is "switched on". Both cut-off transistors TB2 and TB3 are "switched off".

For a change from low to high transimpedance, the opposite actions are taken. The gate voltages of the feedback FETs go high (V_{DD}). TB1 is opened and TB2 and TB3 are closed. In this case stage 3 has to adopt its old (dummy) output voltage to the new feedback situation. This is the major complication to speed up this procedure. Please refer to Sec. 4.2.4 for simulation results.

4.2.3.3 Input Amplifier

The *input amplifier* is a simple inverter. In CMOS circuits inverters have the highest gain. Naturally this gain is only available in a carefully chosen operating point. This inverter is loaded with a PMOS diode load and an adjustable NMOS load. The gain can be lowered by increasing the gate voltage of the FET "TLN" (see Fig. 4.5).

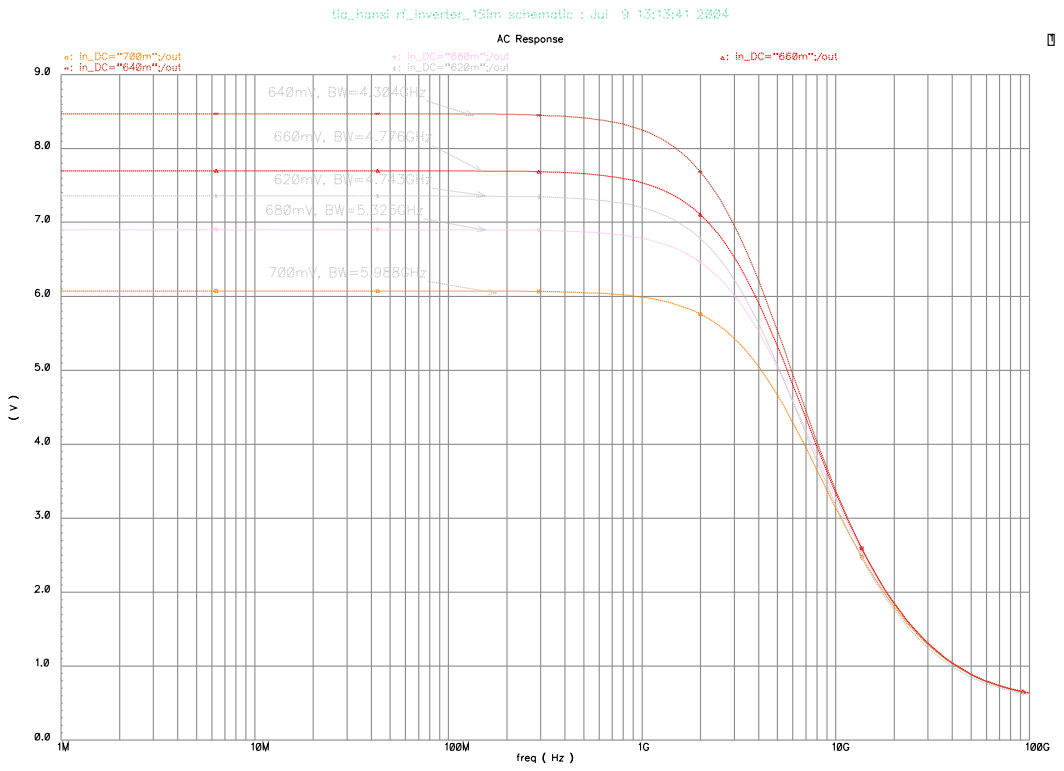
In Fig. 4.6 the simulated AC response of the input amplifier is shown. The curves are simulated with different input operating point. The labels show the operating point voltage and the bandwidth. Values range from 4.3 GHz up to 6 GHz.

The DC transfer characteristic is shwon in Fig. 4.7. At the horizontal axis the operating point voltage is specified and the left scale denotes the output voltage. The orange line is the transfer characteristic. The red line is the differential gain. Its associated vertical scale is labeled at the right. An operating point at 640 mV results in a gain of $-8.5\,\mathrm{V/V}$.

4.2.3.4 Inner Amplifier

The *inner amplifier* increases the open loop gain of the actual TIA. Two common source circuits with adjustable drain resistors are used. By adjusting their operating point their gain can be changed. This is another method to adjust the open loop gain and optimize the bandwidth and noise behavior of the TIA. Each of the two common source circuits adds $180^\circ = \pi$ phase shift. Together with the input amplifier the total phase shift is $540^\circ = 3\pi = \pi$. This is the same as for the input amplifier alone.

Figure 4.6: AC response of the input amplifier



4.2.3.5 Output Amplifier

Behind the TIA another amplifier stage is connected. In the developed chip the comparator with `V_Compare` is there. In the final chip the slicer is there instead. This succeeding circuit will load the output of the TIA. To keep the actual TIA mostly unloaded, the *output driver* is added.

It is a PMOS source follower circuit. The current source can be adjusted with `V_C_Amp4`. By varying this voltage the DC operating point of the output of the total TIA is changed. The comparison voltage `V_Compare` has to be changed accordingly.

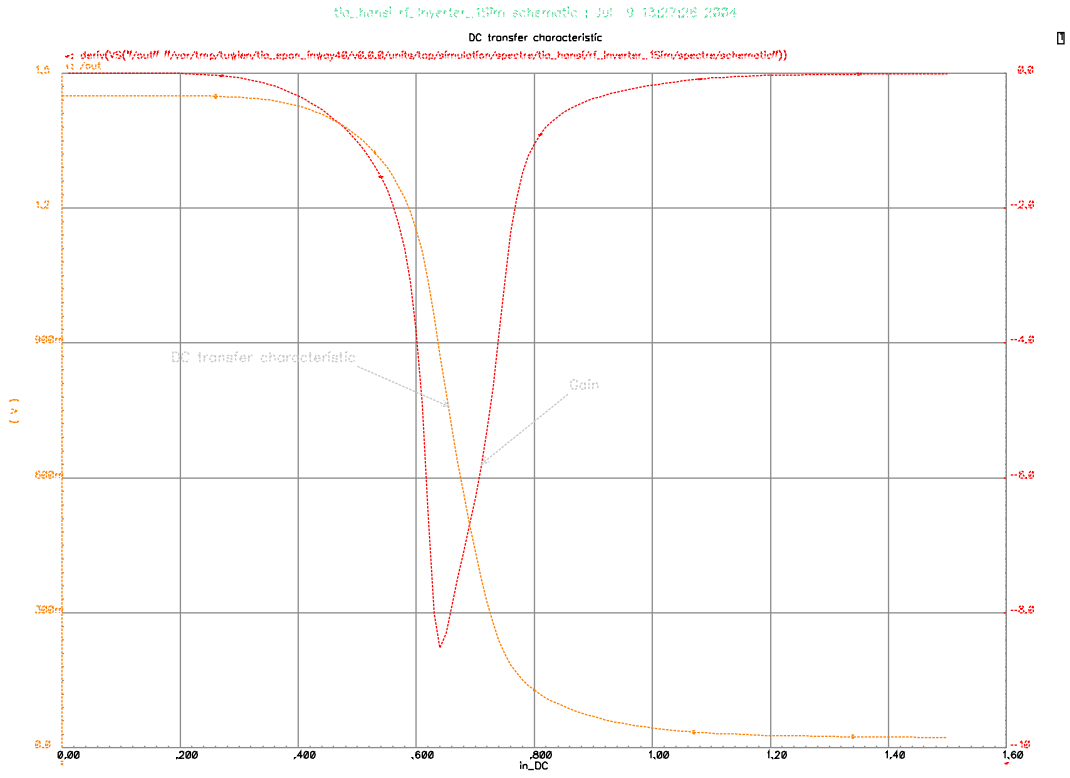
Unfortunately the voltage gain of the output driver is less than one. This is a loss in total gain (i.e. transimpedance) by a factor of approximately $1.2 - 1.4$.

4.2.4 Simulation

4.2.4.1 AC and transient analysis

In Figs. 4.8 to 4.11 simulation results of the TIA are shown. Figures 4.8 and 4.10 show Bode plots of the AC analysis at a given operating point. Note that

Figure 4.7: DC transfer characteristic of the input amplifier



all presented simulations are executed with the nominal process variation setup and at a temperature of 70 °C. During development simulations with all other process variations have been done too.

The first graph shows the transfer characteristic for control voltages adjusted for weak input signal ($I_1 = 3\,\mu\text{A}$). The input AC current is normalized to 1 A. The transimpedance of 7 kΩ of V_{Amp3} is visible. As mentioned in Sec. 4.2.3.5 the output voltage V of the TIA has less transimpedance $R_{\text{TIA}} = 5.3\,\text{k}\Omega$ than V_{Amp3}. The total bandwidth is $f_{\text{c,TIA}} = 2.111\,\text{GHz}$.

The second graph (Fig. 4.9) shows a transient analysis for weak input. Every signal is shown in a separate scale. The signal flow is from top to bottom. A data signal with a bit rate of 2.5 GBit/s is used. The same control voltages have been used for the AC and transient analysis.

The transimpedance for strong input ($I_1 = 300\,\mu\text{A}$) is approximately 92 Ω as depicted in Fig. 4.10. The total gain is 60 Ω. Its bandwidth is $f_{\text{c,TIA}} = 3.41\,\text{GHz}$.

Figure 4.11 shows the result of the transient analysis for strong input signal. Since the inner amplifier is bypassed, V_{Amp2} and V_{Amp3} are omitted.

Figure 4.8: AC transfer characteristic of the total TIA for weak (3 μA) input signal. The total bandwidth is 2.111 GHz at $R_{\mathrm{TIA}} = 5.3\,\mathrm{k\Omega}$.

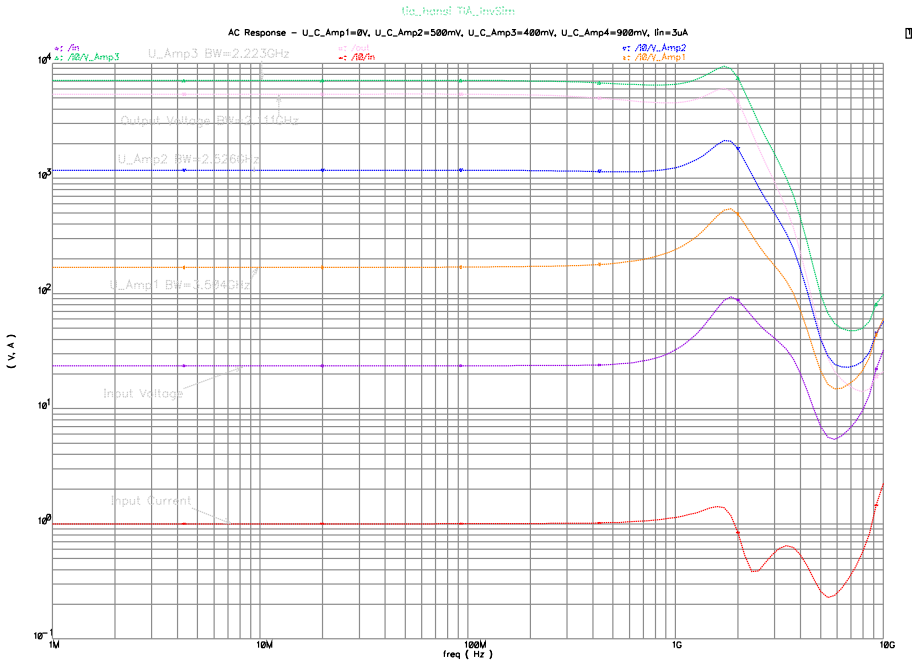


Figure 4.9: Transient analysis of the total TIA for weak input signal (3 μA) at 2.5 GBit for the data signal "000100010010111010111110111".

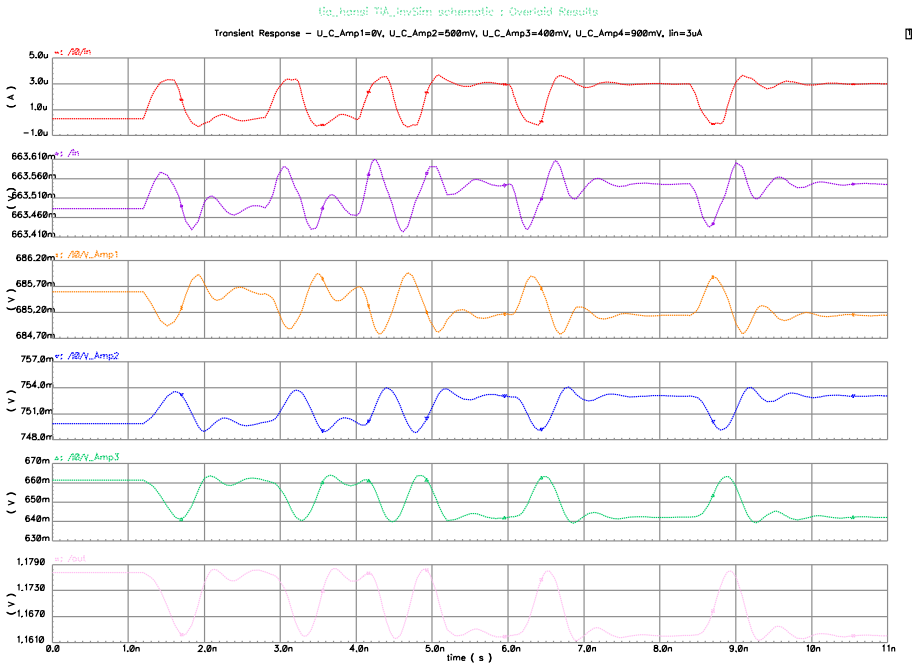


Figure 4.10: AC transfer characteristic of the total TIA for strong (300 μA) input signal. The total bandwidth is 3.42 GHz at $R_{\mathrm{TIA}} = 60\,\Omega$.

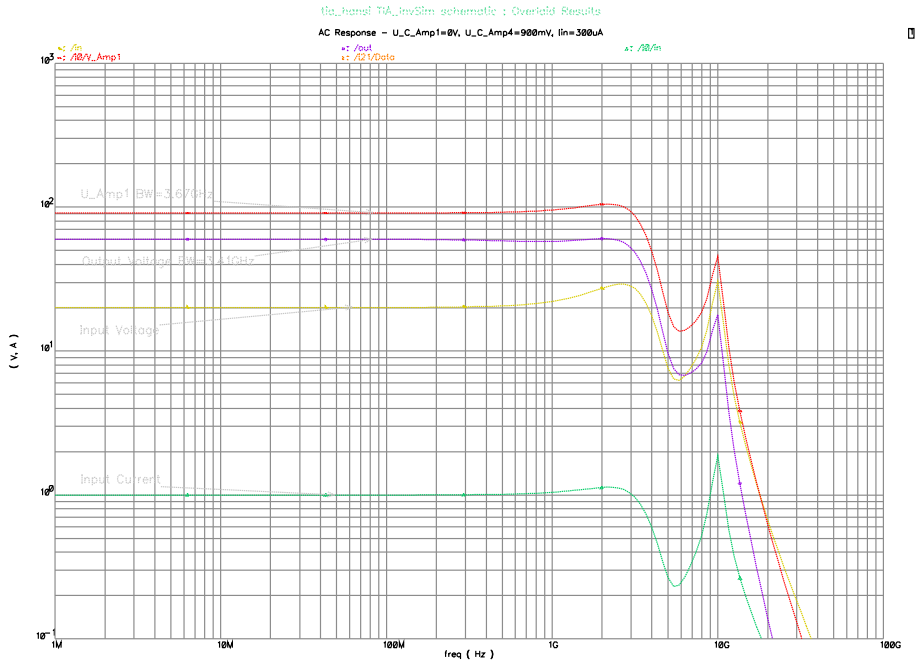
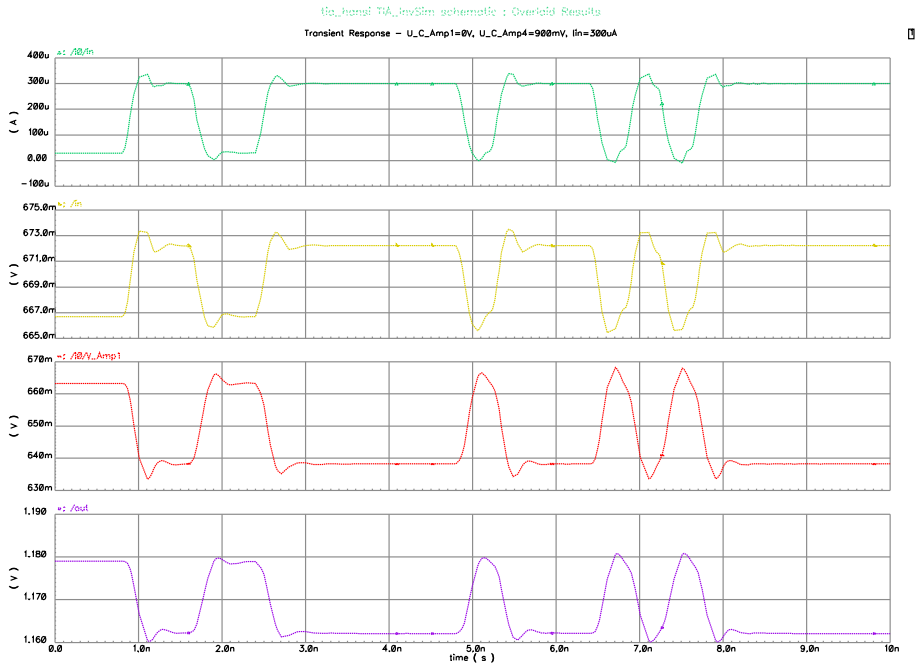


Figure 4.11: Transient analysis for strong input signal (300 μA) at 2.5 GBit for the data signal "00110011111110111010111111"



4.2.4.2 Switch the gain

In Fig. 4.12 a longer transient analysis is shown. It contains three burst periodes, each 10 ns. At 10 ns and 20 ns the gain is switched for the next periode. Marker `M1` and `M2` denote the duration of switching from high gain to low gain. This is accomplished in only 500 ps which is only slightly more than one bit. To switch from low to high gain the markers `M3` and `M4` indicate a duration of 2 ns which is only 5 bits.

Special care was taken to set the control voltages of the inner amplifier for the weak gain period. In principle their values do not matter in this period because the inner amplifier is bypassed. However, the time to switch to high gain can be greatly reduced when keeping the output voltages of both stages V_{Amp2} and V_{Amp3} at the level where they will be in the next high gain period.

4.2.4.3 Noise analysis

Figure 4.13 shows the input referred current noise density plotted versa frequency from 1 kHz to 10 GHz. The simulation was done with an ideal current source with 3 μA peak current emitting pulses with Ex = 10. Parallel to this current source a 1 pF capacitor was appended to simulate the capacity of the real photodiode.

Note that the simulation yields the pure noise current. Measurements will show distortion due to noise *and* limited signal bandwidth. The total bandwidth of the chip is approximately 2 GHz. The current noise density is integrated from 1 kHz to 2.2 GHz. The upper frequency is higher than the chip's bandwidth by a factor of 1.1 because it takes into account that the low-pass characteristic of the chip is not ideal.

The total input referred current noise is $\sqrt{\overline{i_{\mathrm{n,in}}^2}} = 403\,\mathrm{nA}$. This is better than the required 550 nA as stated in Tab. 1.3.

The 50 Ω output driver on the chip doesn't introduce a noticeable noise contribution. For simulation simplification the noise analysis is only accomplished for the TIA and not repeated for the total chip.

4.2.5 Layout

The layout-plot of the TIA is shown in Fig. 4.14. Figure 4.15 describes the colors and patterns used for the metal layers. In the layout there are four large areas of transistor arrays.

Figure 4.12: Transient analysis with switch of gain

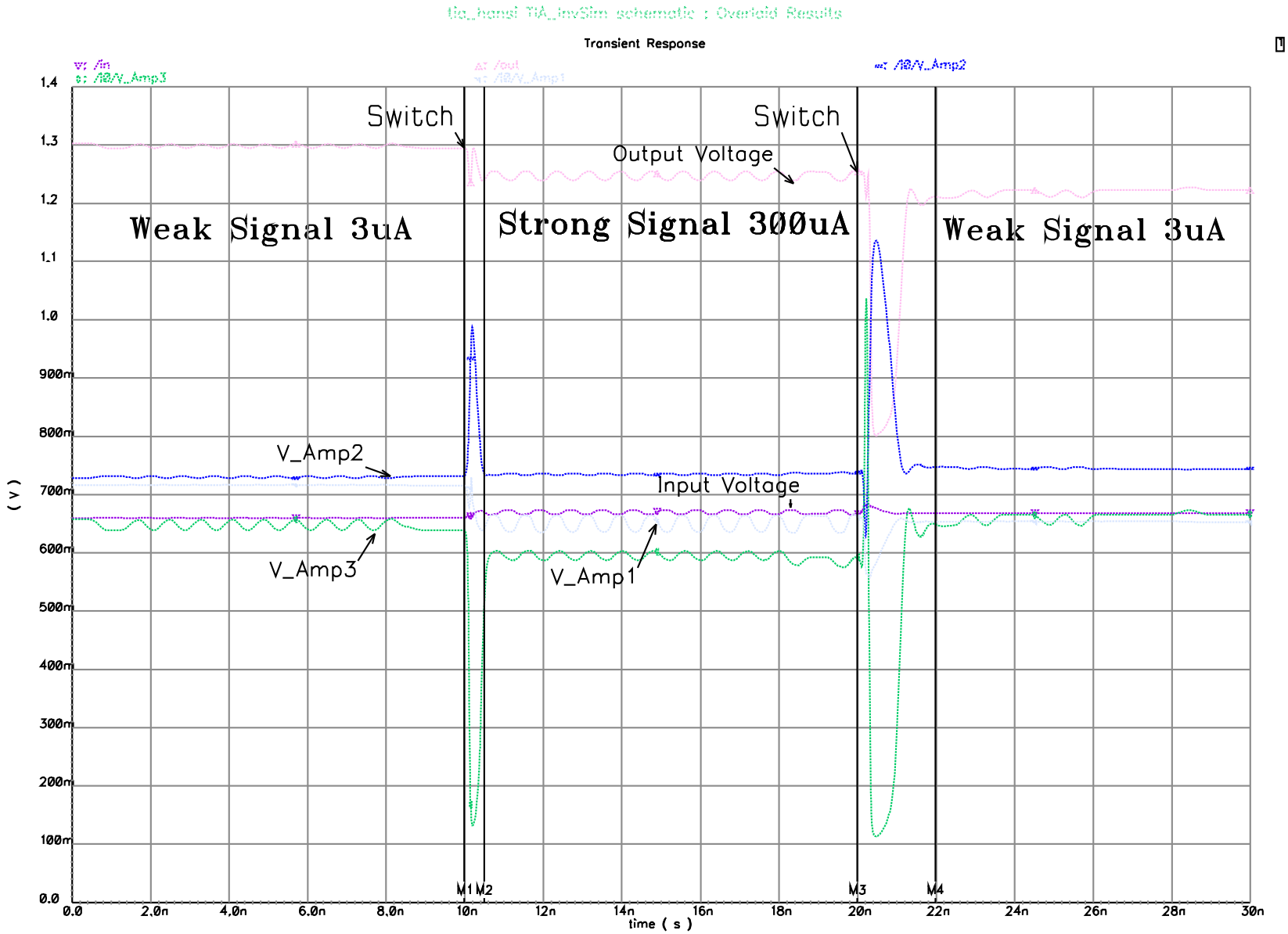
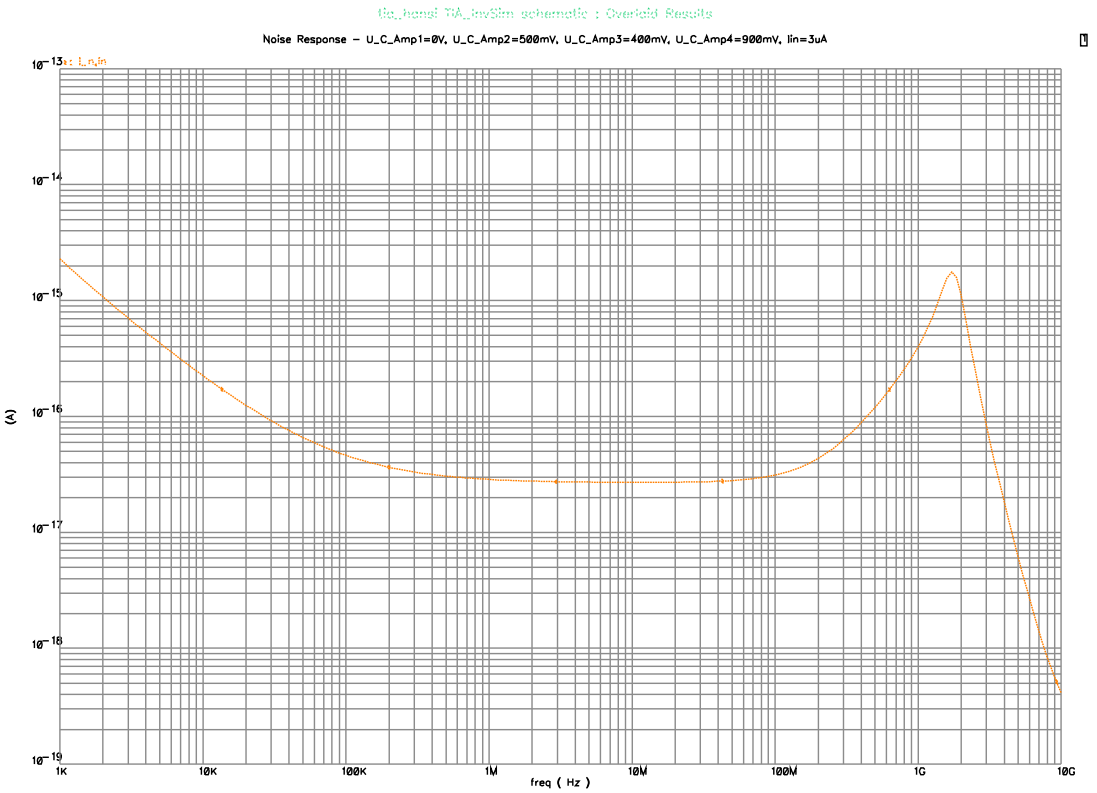


Figure 4.13: Noise analysis of the total TIA



4.2.5.1 Arrangement

In the layout plot (Fig. 4.14) the parts of the amplifier are marked. Table 4.3 describes the different parts.

Table 4.3: Areas of the layout of the TIA in Fig. 4.14

Label	Part
(1)	Input amplifier (inverter)
(2)	Input amplifier (loads)
(3)	Feedback network
(4)	Inner amplifier (second stage)
(5)	Switches
(6)	Inner amplifier (first stage)
(7)	Output amplifier

The arrangement of the different parts is highly optimized. The signal flow therefore is not from top to bottom but helical. It enters at the top left (see the

Figure 4.14: Layout of the TIA: (1) Input amplifier (inverter); (2) Input amplifier (loads); (3) Feedback network; (4) Inner amplifier (second stage); (5) Switches; (6) Inner amplifier (first stage); (7) Output amplifier

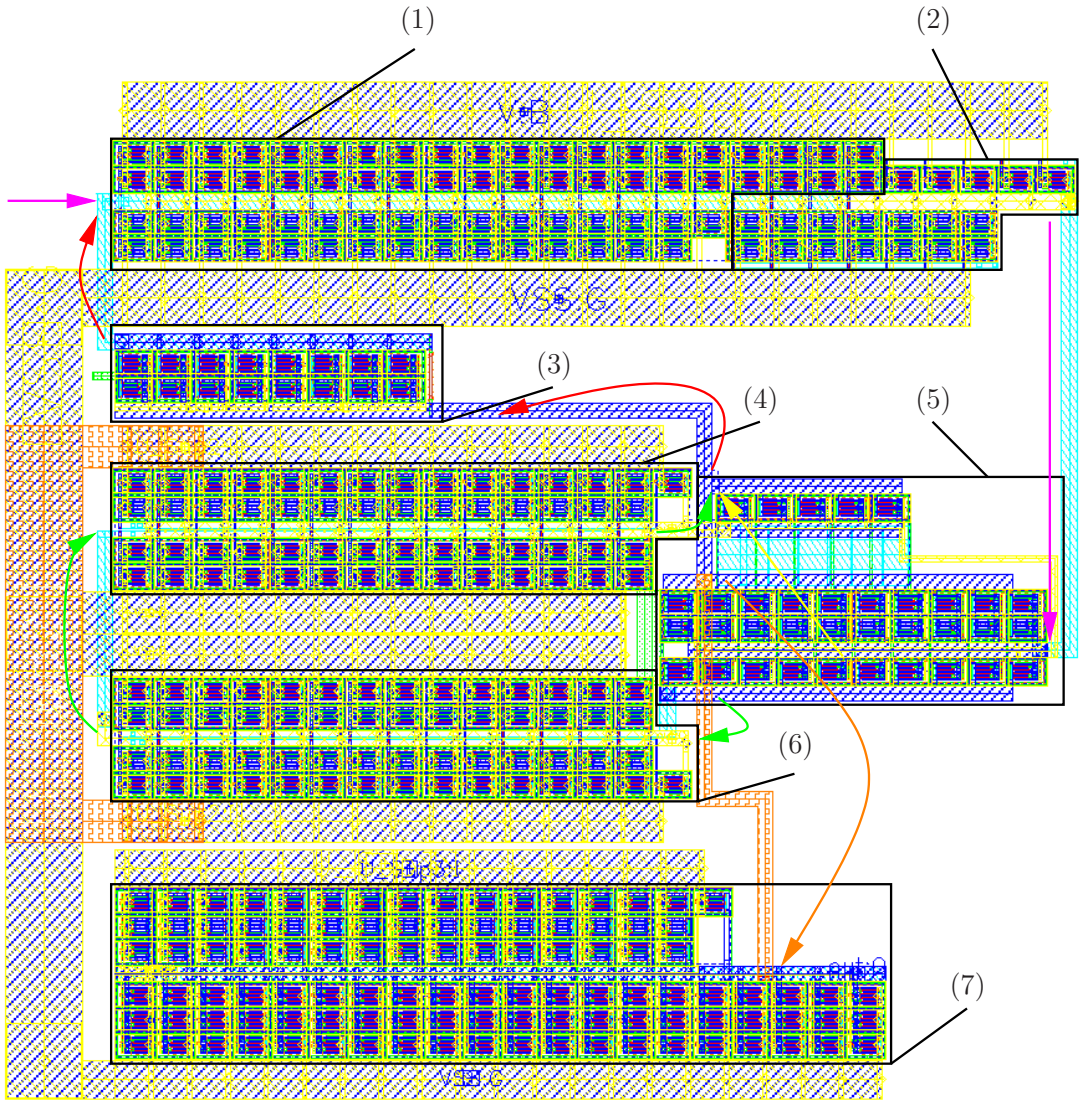
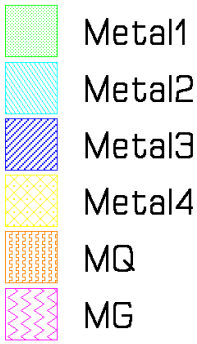


Figure 4.15: Color coding in the layout



magenta arrow). At the right of the input amplifier (1) and (2) the signal goes down (again magenta arrow) to the switches (5). From there it is either directly connected to the feedback network (3) (see the yellow arrow). This is the bypass mode for low gain.

For high gain the signal goes from the bottom side of the switches (5) (see the green arrows) to the first stage if the inner amplifier (6). Its output is connected to the input of the second stage (4). The output of the second stage is then connected via the switch (5) with only 5 transistors to the feedback network (3).

The red arrows denote the path to the feedback network (3). One side of it is directly connected with the input (top left). The other side is connected with the output of the switches (right side).

Finally the signal goes to the output amplifier (7). This is marked by the orange arrow. The output of the TIA is at the right side of the output amplifier (7).

4.3 Prepare and Hold

The *Prepare and Hold (P&H)* circuit is designed to provide the control voltages for the TIA.

4.3.1 Application

The control voltages for the TIA are supplied from the outside of the developed chip. In the final chip they will come from a Digital to Analog Converter (DAC).

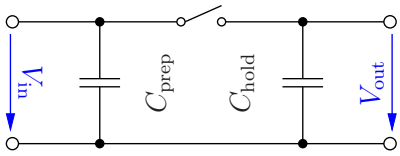
Section 4.1.1.3 describes the hard conditions for the change of the control voltages. No such DACs are available. It is not even possible to reliably conduct these fast edges via a bond wire into the chip.

To circumvent these problems the P&H circuit is implemented. The control voltages can be prepared relatively slowly. This temporary process is decoupled by the P&H from the inner circuit. Finally in a precise moment the prepared *new* control voltages are switched to the inner circuit (= the TIA). During this transient process the TIA's output is unusable so this change must be as fast as possible to avoid loss of received bits. It is even possible to implement a relative time shift ($\approx 20 - 200\,\mathrm{ps}$) between the various control voltages with little delay circuits in the P&H's control signals to optimize the switching behavior of the TIA.

4.3.2 Function

In Fig. 4.16 the basic structure of the P&H circuit is drawn. It consists of two capacitors C_{prep} and C_{hold} and a switch. In normal operation the switch is open. The hold-capacitor C_{hold} presents its "saved" voltage V_{out} to the circuit following the P&H. It is decoupled from the (possibly noisy) input.

Figure 4.16: Basic structure of the P&H circuit



Concurrently from outside the voltage V_{in} at the prepare-capacitor C_{prep} is setup. In other words, the *new* voltage is prepared. In a precisely defined moment the switch is closed for a short time. The prepared voltage is "copied" to the hold-capacitor. When the switch is open again, the new voltage $V_{\mathrm{out,new}} \approx V_{\mathrm{in}}$ is presented to the following circuit.

Naturally the voltage is not "copied". Physically the charges in both capacitors are balanced. The final state is reached when both capacitors have equal voltages. Before the switch is closed, the charge at C_{prep} and C_{hold} are

$$Q_{\mathrm{prep}} = C_{\mathrm{prep}} V_{\mathrm{in}} \tag{4.2}$$

$$Q_{\mathrm{hold}} = C_{\mathrm{hold}} V_{\mathrm{out}}. \tag{4.3}$$

When the switch is closed, after some time both voltages will be equal

$$V_{\mathrm{out,new}} = V_{\mathrm{in,new}}. \tag{4.4}$$

The total charge in both transistors is

$$Q = Q_{\mathrm{prep}} + Q_{\mathrm{hold}} = C_{\mathrm{prep}} V_{\mathrm{in}} + C_{\mathrm{hold}} V_{\mathrm{out}}. \tag{4.5}$$

No charge can pop up or or vanish (we assume lossless conduction). The total charge after the transient process must be the same as before. Since both voltages will be equal we can write

$$Q = (C_{\text{prep}} + C_{\text{hold}})V_{\text{out,new}}. \tag{4.6}$$

$$V_{\text{out,new}} = \frac{Q}{C_{\text{prep}} + C_{\text{hold}}} \tag{4.7}$$

Inserting (4.5) we get

$$V_{\text{out,new}} = \frac{C_{\text{prep}}V_{\text{in}} + C_{\text{hold}}V_{\text{out}}}{C_{\text{prep}} + C_{\text{hold}}} = V_{\text{in}} + (V_{\text{out}} - V_{\text{in}})\frac{C_{\text{hold}}}{C_{\text{prep}} + C_{\text{hold}}}. \tag{4.8}$$

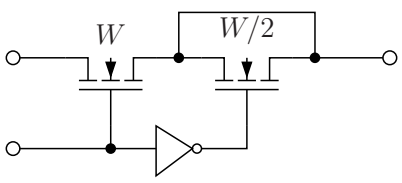
If C_{prep} is large compared to C_{hold} the final voltage $V_{\text{out,new}}$ will be nearly the prepared voltage V_{in}.

4.3.3 Implementation

The implementation is very similar to the schematic shown in Fig. 4.16. The switch is built as an NMOS and a PMOS FET in parallel. This is necessary to provide good conductivity for low voltages ($0\,\text{V} - 1\,\text{V}$) and for high voltages ($0.5\,\text{V} - 1.5\,\text{V}$).

The gate control voltage for the switch is a very sharp pulse. Unfortunately the edges of the pulse inject some charge to both capacitors C_{prep} and C_{hold}. This charge is high enough to disturb the output voltage for more than 20%! Luckily special Sample and Hold switch circuits are known from literature. [Zim04a] In Fig. 4.17 the NMOS switch is shown. The actual FET switch is followed by a second one with approximately half the gate width $W/2$. It is short-circuited and controlled by the inverted pulse. With careful optimization of the gate width $\approx W/2$ the load injection can be minimized.

Figure 4.17: Switch structure of the P&H circuit



4.3.4 Simulation

The simulation results are shown in Fig. 4.18 and 4.19. The first graph shows ten consecutive burst cycles. In every cycle the *next* voltage is prepared. At every 100 ns interval the pulse to close the switch for a short moment is generated. There are several lines drawn. The "Destination Voltage" is the desired voltage after both capacitors have the same voltage. Therefore the "Prepared Voltage" must be slightly larger or smaller, depending on the direction of the change.

"`U_C_prep`" is the voltage at $C_{\text{prep}} = 15\,\text{pF}$. This capacitor is loaded through the output resistor of the DAC. This is why we see exponential convergence. Finally, the "Hold Voltage" is switched to the new value when the switch is closed. Due to residual charge injection, it differs slightly from the destination voltage. Unfortunately, the switch in its "Off" state doesn't isolate good enough. This is why the sharp edges of "Prepared Voltage" cross-talk to the hold voltage.

The hold capacitor $C_{\text{hold}} = 203\,\text{fF}$. This value is chosen to result in a total capacitance of 1 pF combined with the gate of the comparator after the TIA. In the simulation this transistor is also included.

In Fig. 4.19 a tiny time interval of only 1 ns is zoomed. The "Prepared Voltage" and "Destination Voltage" already settled for the next interval. The "Hold Voltage" still has the old value. At 500 ns the "Input Pulse" starts. From this signal the real pulse is generated. We will look at this in a moment. During this pulse the switch is closed. The "Hold Voltage" exponentially converges to the "Destination Voltage". The "Prepared Voltage" decreases a little bit. As you can see, the destination is reached very accurately. The falling edge of the pulse then injects some charge which changes the final "Hold Voltage". The transient process is finished within less than 500 ps.

4.3.5 Layout

In Fig. 4.20 the layout of the P&H is shown. The six large rectangles at the top are the C_{prep} with a total capacity of 15 pF. At the bottom the switch built with NMOS and PMOS FETs is shown. The small rectangle at the bottom right is the $C_{\text{hold}} = 203\,\text{fF}$.

4.3.6 Pulse Generator

A dedicated *pulse generator* is included on the chip. It is a modified *mono-stable trigger circuit*. See [TS02] for details. The pulse duration is given by

$$t_{\text{Pulse}} \approx 0.7RC. \tag{4.9}$$

Figure 4.18: Ten P&H cycles: different voltages are (slowly) prepared and then applied very quickly.

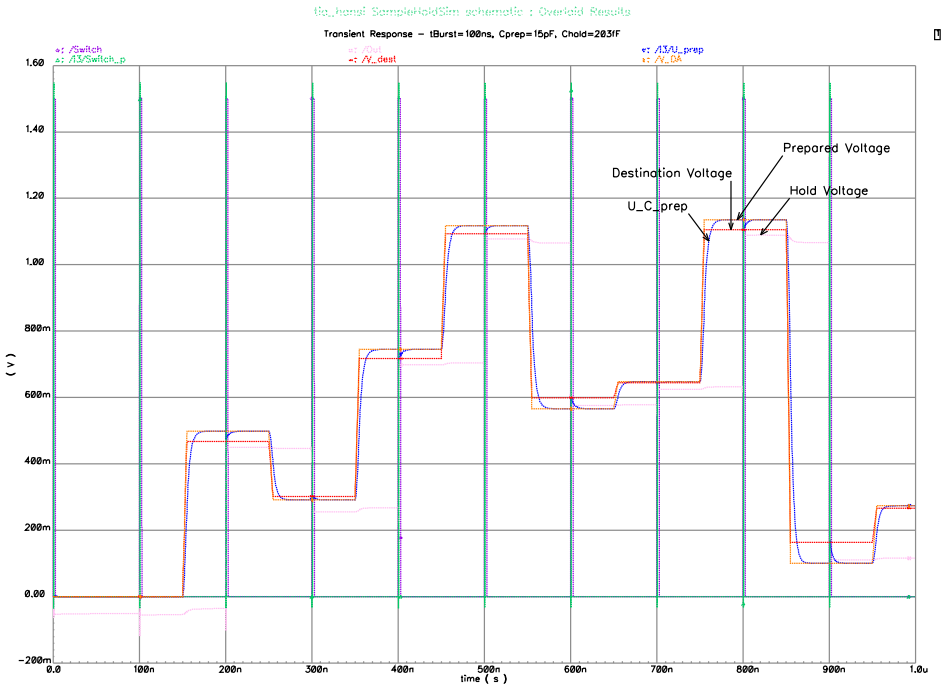


Figure 4.19: The transient process in the P&H

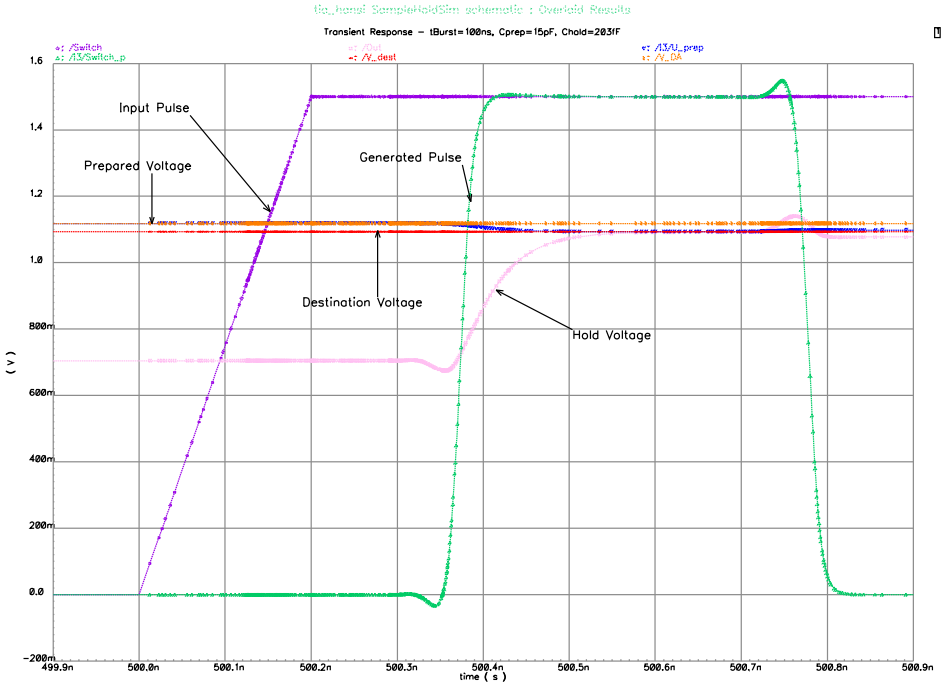


Figure 4.20: Layout of the P&H circuit

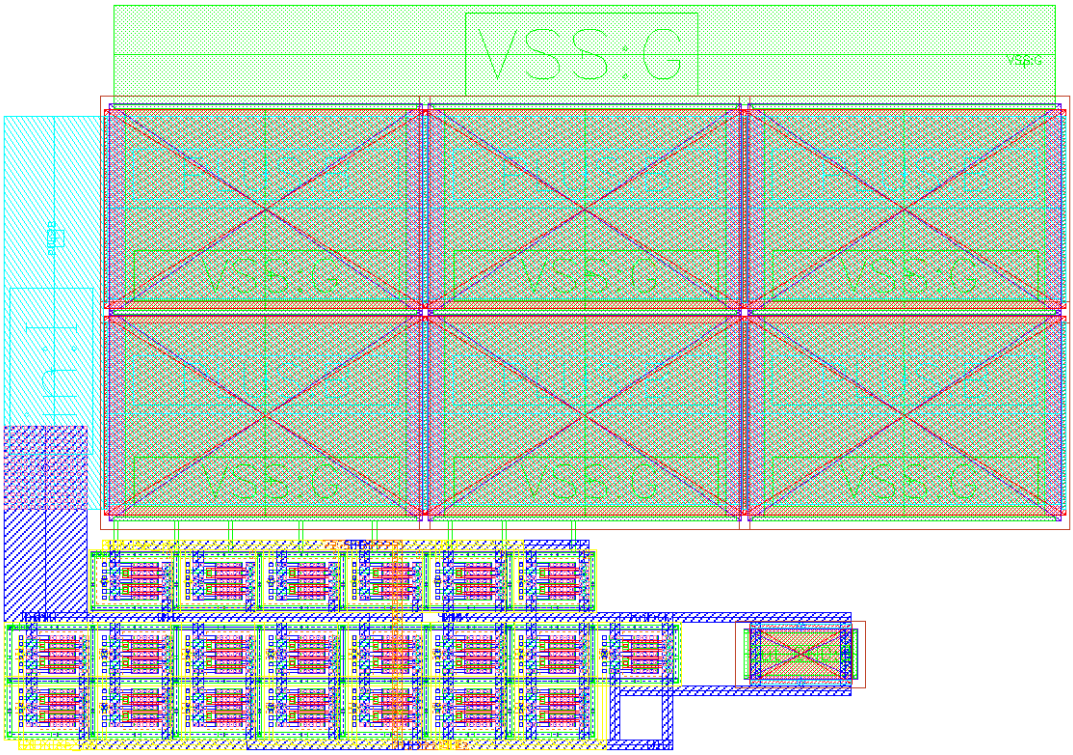
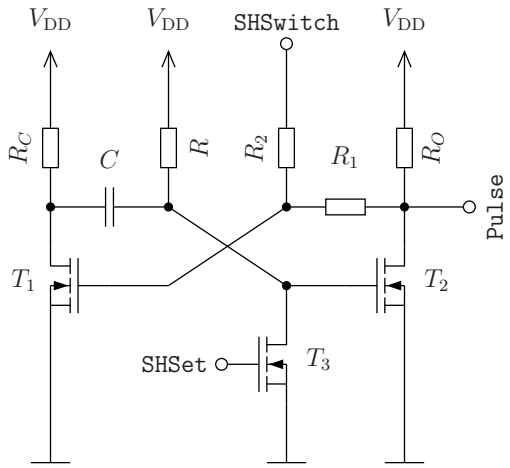


Figure 4.21: Schematic of the pulse generator



For a pulse width of $t_{\text{Pulse}} = 600\,\text{ps}$ the values $R = 1.7\,\text{k}\Omega$ and $C = 500\,\text{fF}$ have been chosen. The other values are $R_C = 5\,\text{k}\Omega$ and $R_1 = R_2 = R_C = 1\,\text{k}\Omega$.

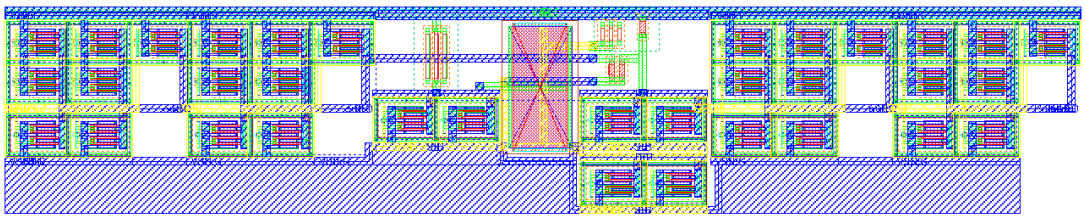
When a rising edge at the input "SHSwitch" is applied, a pulse at the output "Pulse" is generated. This output is followed by two inverters for sharp edges. The pulse in Fig. 4.19 is the final result. The input SHSwitch is also "pre-filtered" by two inverters (not shown in the figure).

The additional FET T_3 at the bottom is used to permanently emit a logical "1" signal. This is necessary to operate the designed chip in continuous mode. The control signal SHSet switches to this operating mode.

4.3.6.1 Layout

The layout of the pulse generator is shown in Fig. 4.22. The two arrays of seven FETs each at the left and at the right are the double-inverter pulse shapers. The red rectangle in the center is the capacitor C. To the left the (double-)transistor T_1 is placed. T_2 is at the right of C. The "always-on" transistor T_3 is below T_2.

Figure 4.22: Layout of the pulse generator for the P&H



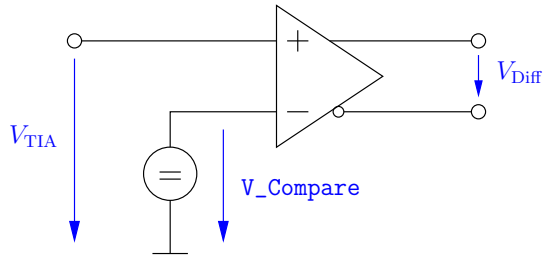
The resistors R and R_C have short-circuited dummy resistors on both sides. This is necessary because of the semiconductor process characteristics. The input SHSwitch of the pulse generator is the Metal4 path at the left between the five PMOS at the top and the two NMOS at the bottom. The output Pulse is the Metal3 path at the right between the NMOS and PMOS. The input SHSet is the Metal4 path below T_3.

4.4 Comparator and Output Drivers

As mentioned earlier the TIA is a pure single-ended amplifier. We want to amplify its output even further to drive 50 Ω loads like an oscilloscope. To avoid additional noise, interference and crosstalk this output amplifier should be differential. The single-ended signal from the TIA has to be converted to a differential signal.

This conversion is accomplished by a differential amplifier which compares the output of the TIA to the reference level V_Compare. See Fig. 4.23 for a simplified schematic. V_Compare is applied as a control voltage from the outside. It is the only control voltage not directly supplied to the TIA.

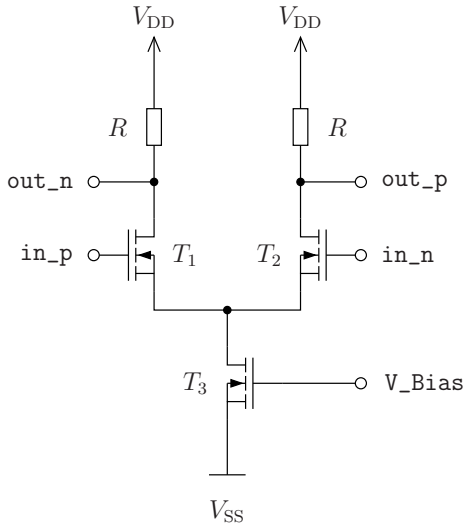
Figure 4.23: Schematic of the comparator



4.4.1 Differential Amplifier

The cell `rf_Diff` is used for the afore mentioned comparison. Figure 4.24 shows the schematic of it. As always the transistors are only drawn once but placed multiple.

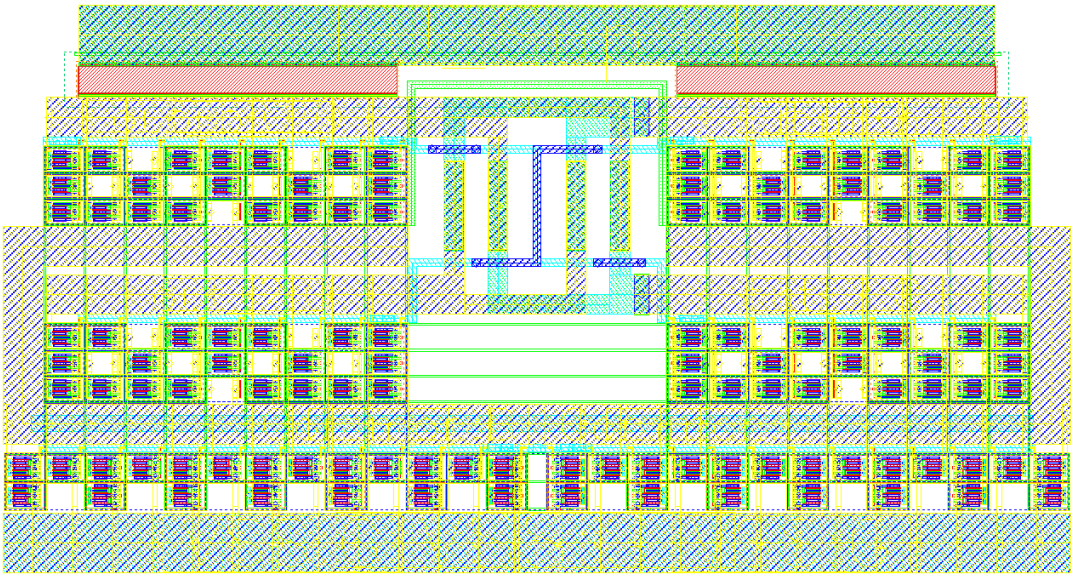
Figure 4.24: Schematic of the differential amplifier



A second such amplifier is placed in series to increase the gain. The `V_Bias` bias input is supplied by a bias network which will be discussed in the next subsection.

The layout of `rf_Diff` is shown in Fig. 4.25. Please note the exact symmetry of the amplifier. It is built of two identical halves. They are connected with a specially designed symmetric network. The easy parts are the common ground at the bottom (`Metal2`, `Metal3` and `Metal4`) as well as the common source connection of T_1 and T_2. The latter is the horizontal "C"-shape `Metal2`+`Metal3` path. Both drain connections are crossed in the area at the top center. At the very top the common supply V_{DD} and both resistors R (red) are shown.

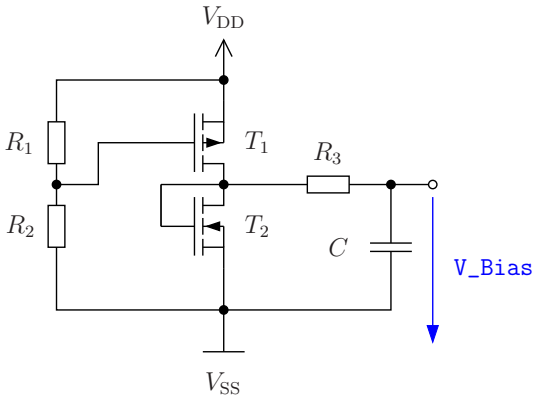
Figure 4.25: Layout of the differential amplifier `rf_Diff`



4.4.2 Bias Networks

All amplifiers after the TIA get their bias voltages from internal bias networks. The disadvantage is that the operating points depend on process variations. Beneficial is the reduction of bond pads of the chip. In Fig. 4.26 the schematic is shown. A layout of one bias network is presented in Fig. 4.27.

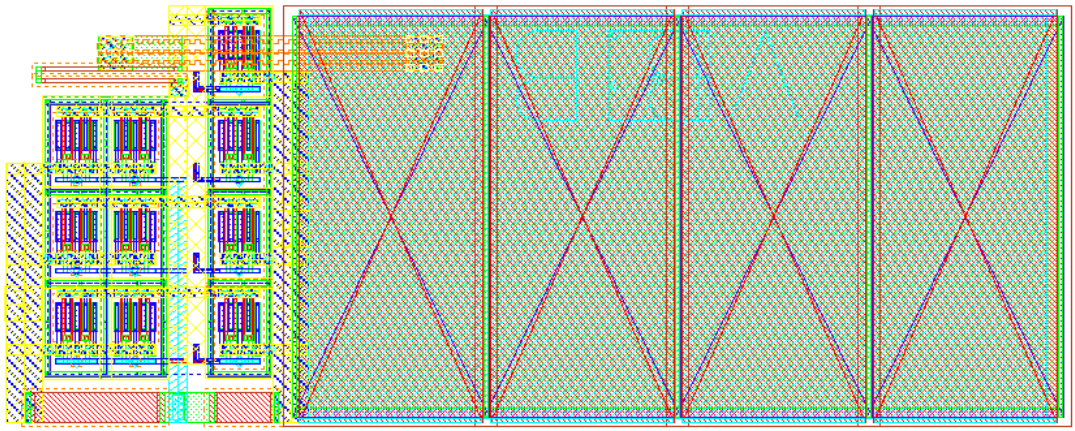
Figure 4.26: Schematic of the bias network



The values of R_1 and R_2 as well as the multiplication factor of the transistors T_1 and T_2 determines the bias voltage `V_Bias`. The RC network with $R_3 = 30\,\mathrm{k\Omega}$ and $C = 10\,\mathrm{pF}$ filters and stabilizes the bias voltage. There are three different

bias networks on the designed chip. They differ in the resistor values, FET counts and gate connections.

Figure 4.27: Layout of a bias network



4.4.3 NMOS Source Follower

After the two differential amplifiers an NMOS source follower shifts down the signal levels. Figure 4.28 shows the schematic. One source follower for both signal polarities each is implemented on the chip. The layout is depicted in Fig. 4.29.

Figure 4.28: Schematic of the NMOS source follower. The bulk of T_1 is also connected to VSS.

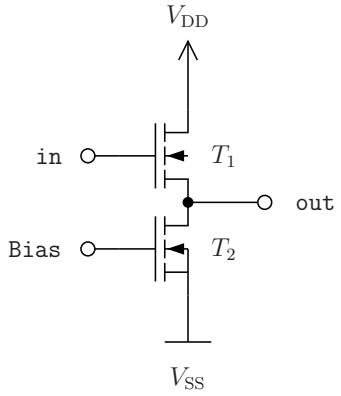
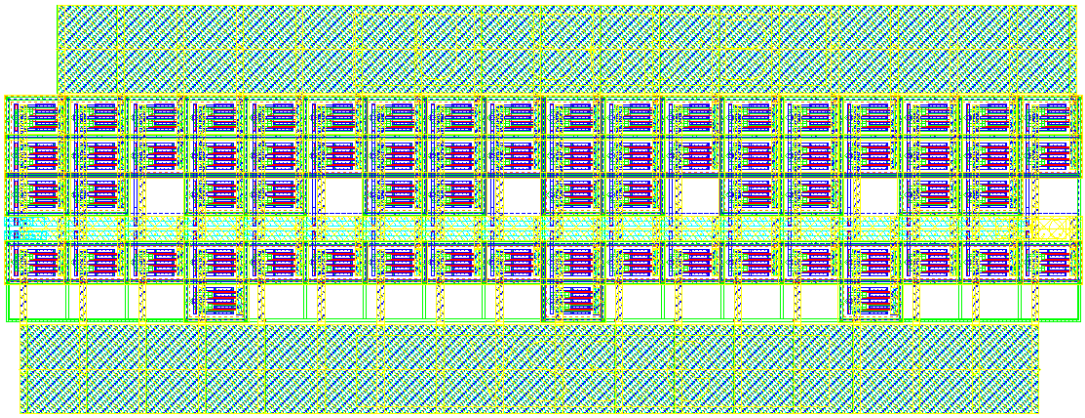


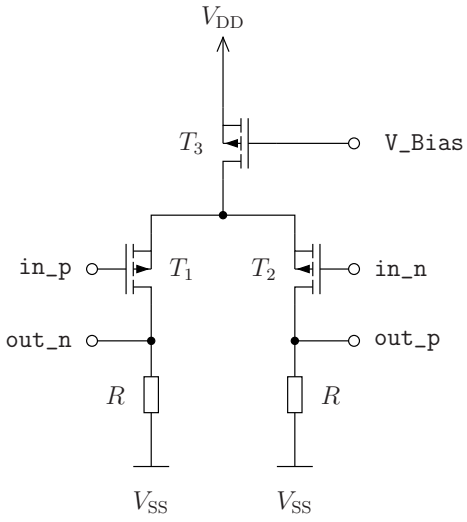
Figure 4.29: Layout of the NMOS source follower



4.4.4 Output Driver

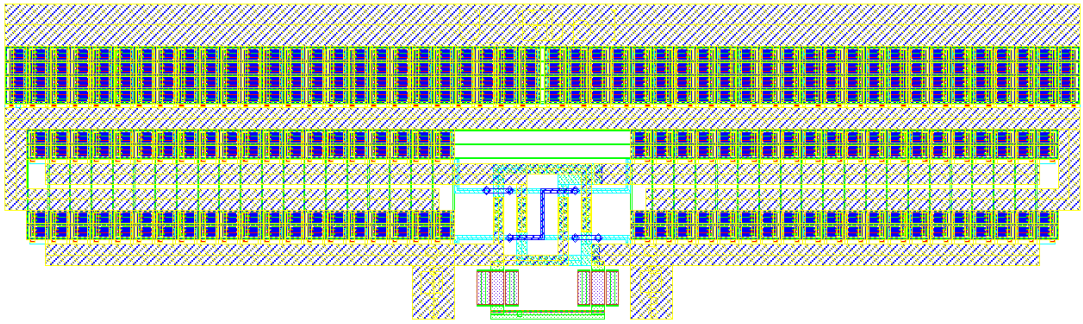
The output driver directly drives the two output pads `out_p` and `out_n`. It is a PMOS differential amplifier. In Fig. 4.30 the schematic is drawn. The value of both resistors to $R = 200\,\Omega$.

Figure 4.30: Schematic of the output driver



See Fig. 4.31 for the layout. Here again special care has been taken to achieve most possible symmetry. The huge FET array at the top is T_3. T_1 and T_2 are split in to halves and drawn below T_3. At the bottom both resistors R are placed. The `Metal1` path in the center is the ground V_{DD} connection. The two `Metal3`+`Metal4` paths pointing downwards are the outputs `out_p` and `out_n`. The positive supply is applied at the large path at the top.

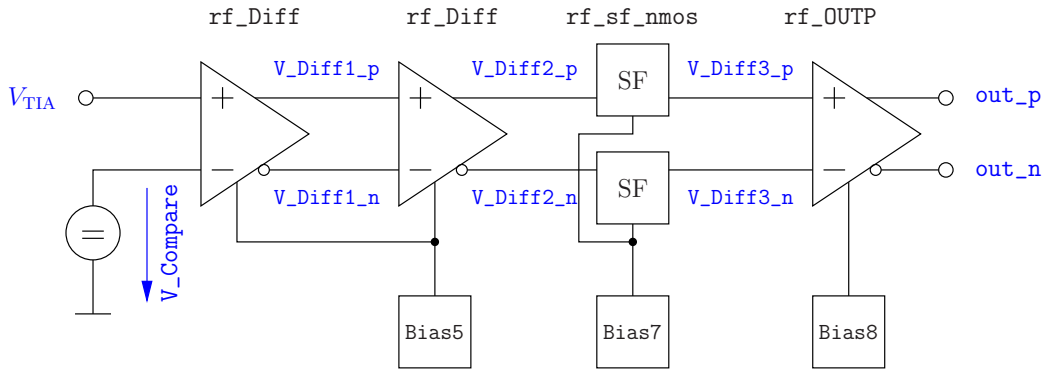
Figure 4.31: Layout of the output driver `rf_OUTP`



4.4.5 Simulation

The complete *output amplifier* is sketched in Fig. 4.32. The `Input` receives the signal directly from the TIA. Both outputs `out_p` and `out_n` are directly connected to the bond pads.

Figure 4.32: Block diagram of the complete output amplifier

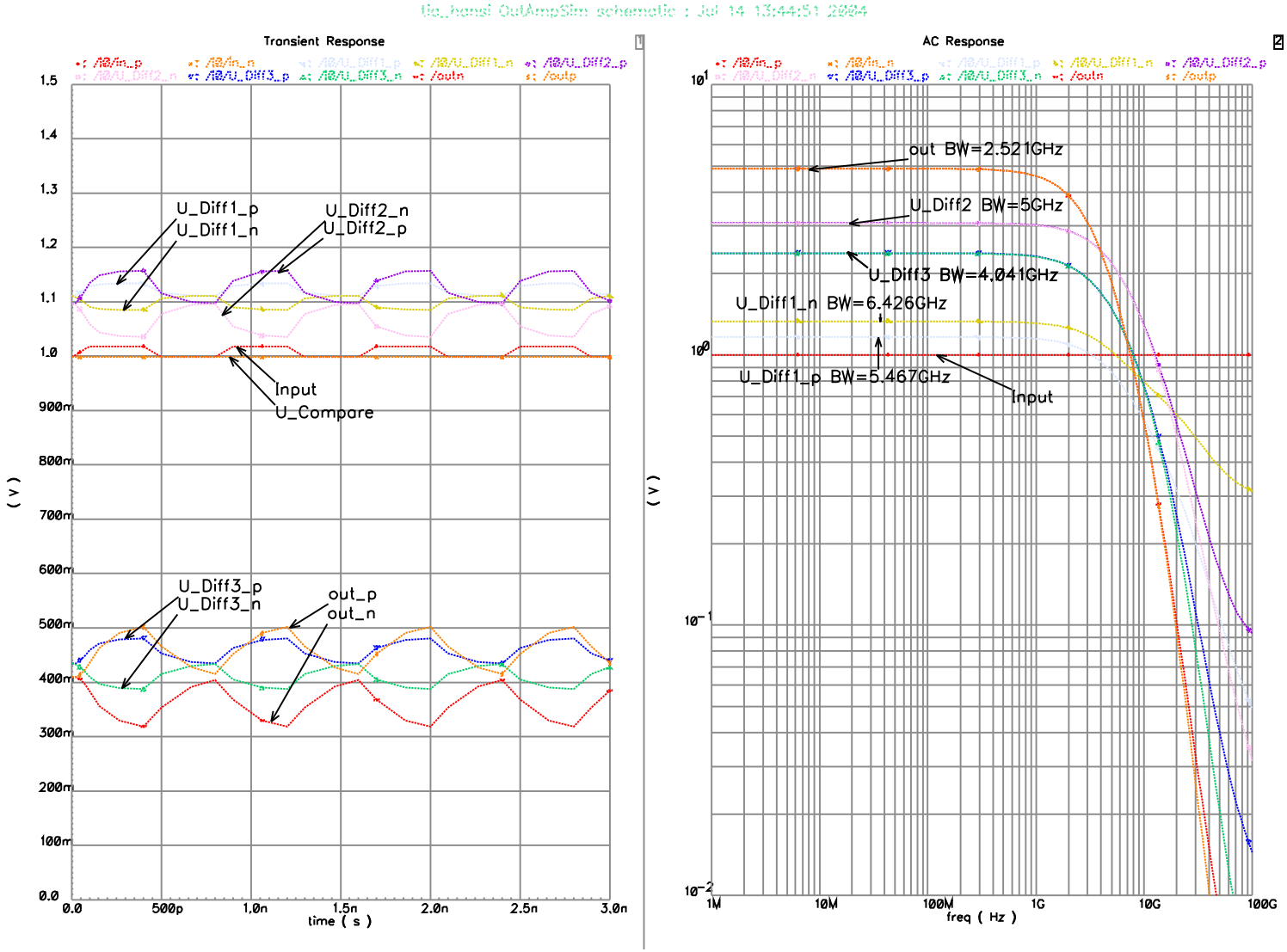


In Fig. 4.33 a transient and AC simulation of the complete output amplifier including the voltage comparison is shown. The transient simulation uses a trapezoidal input signal with "10101010" bit pattern. The bit duration is 400 ps. The rising edge of the trapezoid is 100 ps. The signal names are the same as in the schematic Fig. 4.32. Where no `_p` or `_n` suffix is written both graphs overlap.

4.5 Supply

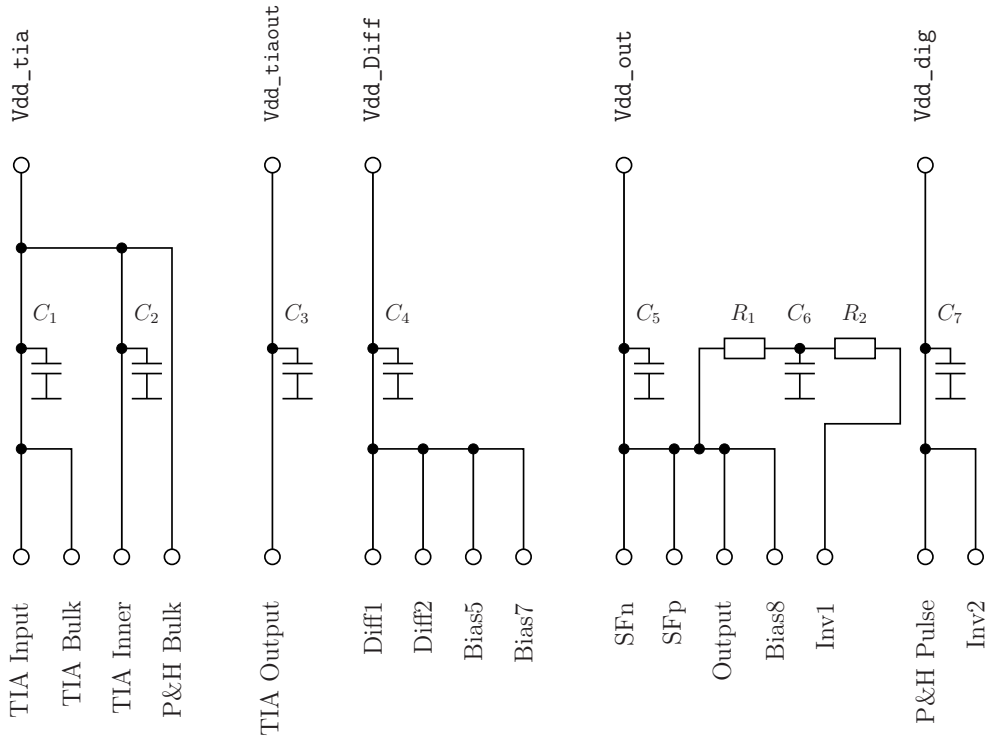
Supply is a curcial part of the developed chip. High stability and good decoupling of each supply for every amplifier stage is necessary to achieve the high bandwidth

Figure 4.33: Transient and AC simulation of the total output amplifier



and to switch the gain fast enough. In Fig. 4.34 the supply distribution network is drawn.

Figure 4.34: Schematic of the supply network



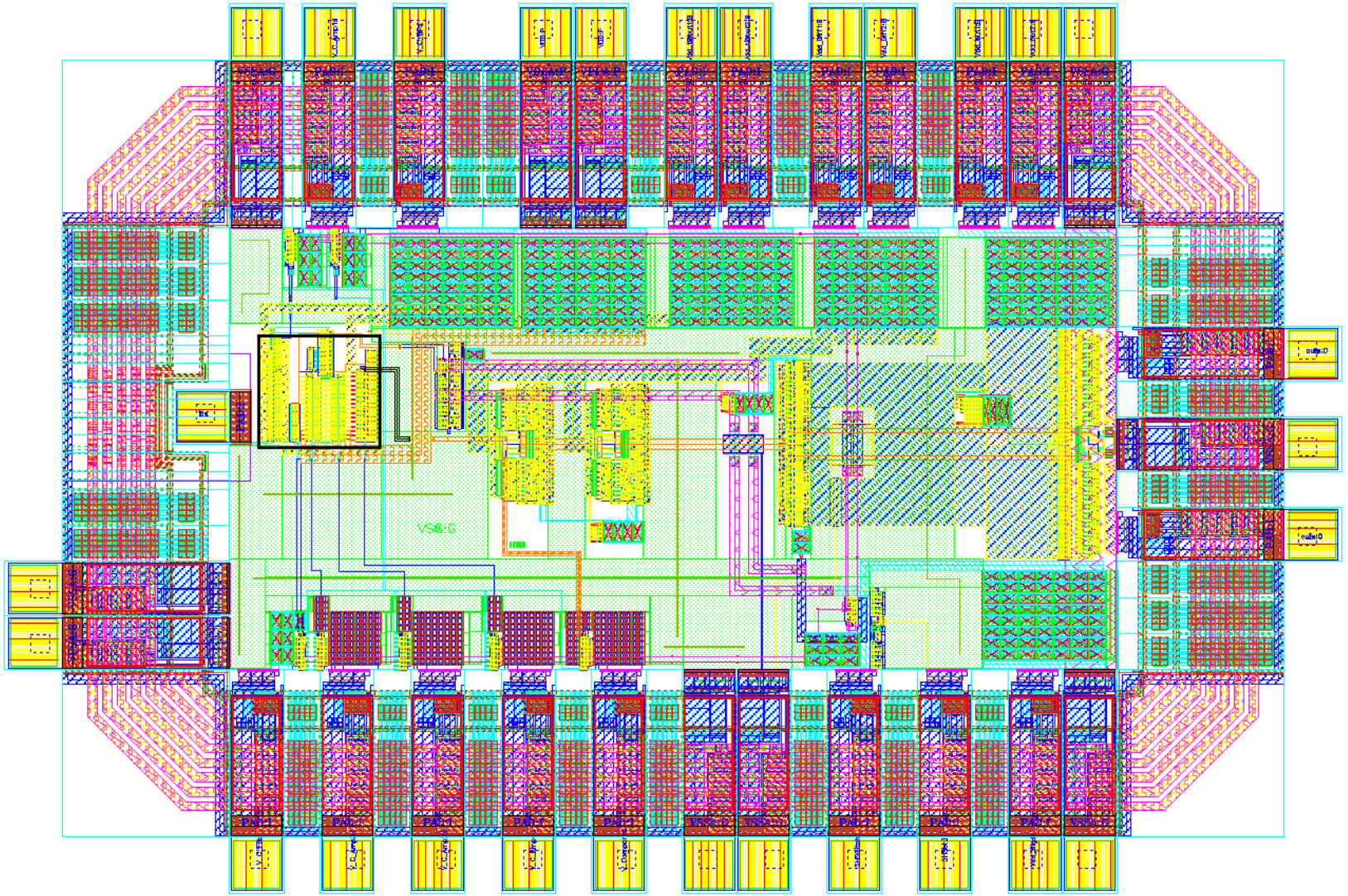
The six labels at the top correspond to the six external supply bond pads. All of them are placed twice to half the bond wire resistance. Only `Vdd_dig` is a single pad because no high loads are supplied.

The labels at the bottom denote the target of the supply. Please refer to Tab. 4.4 for description of them. It should be noted that the digital control voltage `V_C_BP` is pulse shaped by two on-chip inverters. Its inverted signal $\overline{\texttt{V\_C\_BP}}$ (compare Fig. 4.5 and Tab. 4.2) is delayed for approximately 200 ps. This improves the gain switching. Therefore nine inverters are used in series. They are supplied by the "Inv2" supply. Those inverters which have an output connected to the TIA or the P&H circuits are supplied by the extra filtered "Inv1".

4.6 Total Chip

The layout of the total chip is shown in Fig. 4.35. The dimension of the chip is $1500 \times 1000\,\mu\text{m}^2 = 1.5 \times 1\,\text{mm}^2$. The black frame marks the TIA. The size of the TIA $18840\,\mu\text{m}^2$ is only an $\frac{1}{80}$ of the total chip size.

Figure 4.35: Layout of the developed chip



4.6.1 Chip Core

The *chip core* is the central part of the chip. Its size is $980 \times 480\,\mu\text{m}^2$. This core is surrounded by the so called "*pad frame*". The pad frame contains an *Electrostatic Sensitive Device (ESD)* protection circuit for every bond pad. The input pad has no ESD protection circuits for better input signal quality. In Fig. 4.35 the pads are drawn as yellow squares along the chip border. Positive and negative supply paths are placed around the chip in the pad frame. The easily visible $45\,^\circ$ paths at all 4 corners are used to close this supply ring. The ESD protection circuits are connected to this supply paths.

4.6.2 Simulation

4.6.2.1 AC and transient analysis

The AC and transient simulation results of the total chip are shown in Figs. 4.36, 4.37, 4.38 and 4.39. For an input signal as low as $3\,\mu\text{A}$ and maximum gain of the TIA Figs. 4.36 and 4.37 show the AC and transient analysis respectively. An input signal with $300\,\mu\text{A}$ and minimum gain is used for the AC and transient analysis shown in Fig. 4.38 and 4.39, respectively.

Table 4.4: Supply destination descriptions

Label	Description
TIA Input	TIA Input Amplifier
TIA Bulk	TIA PMOS Bulks
TIA Inner	TIA Inner Amplifier
P&H Bulk	P&H PMOS Bulks
TIA Output	TIA Output Driver
Diff1	first `rf_Diff`
Diff2	second `rf_Diff`
Bias5	`Bias5`
Bias7	`Bias7`
SFn	Source Follower in "n" path
SFp	Source Follower in "p" path
Output	Output Driver
Bias8	`Bias8`
Inv1	Inverters with control voltage outputs
P&H Pulse	P&H Pulse Generator
Inv2	long inverter Chain

Figure 4.36: AC transfer characteristic of the total developed chip for weak (3 μA) input signal

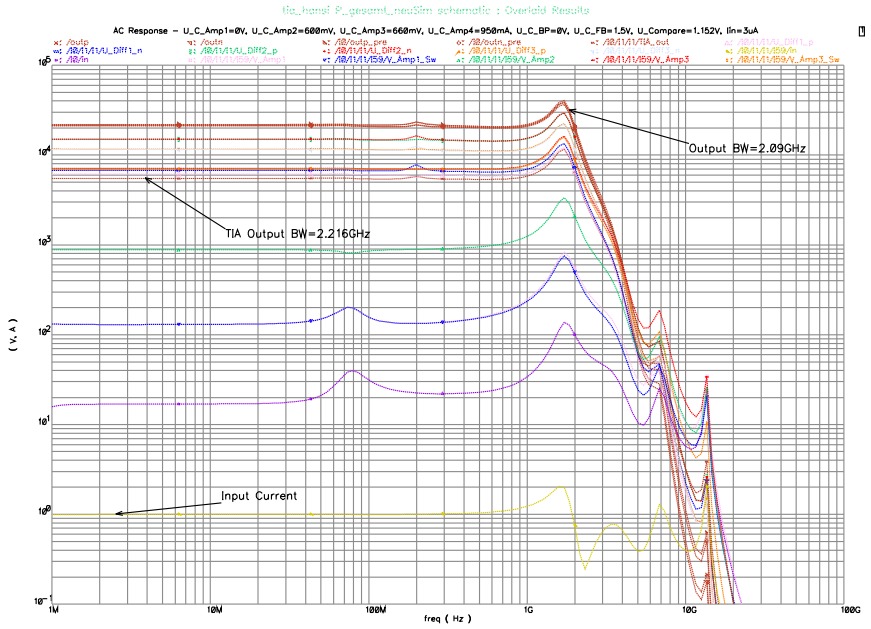


Figure 4.37: Transient analysis of the total developed chip for weak input signal (3 μA) at 2.5 GBit/s for the data signal "000100010010111010111110111"

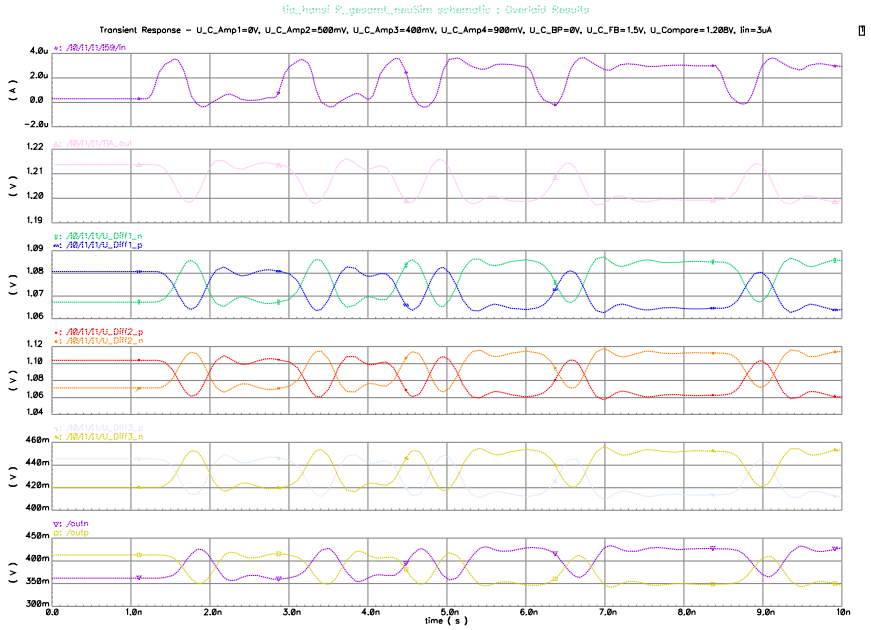


Figure 4.38: AC transfer characteristic of the total developed chip for strong (300 μA) input signal

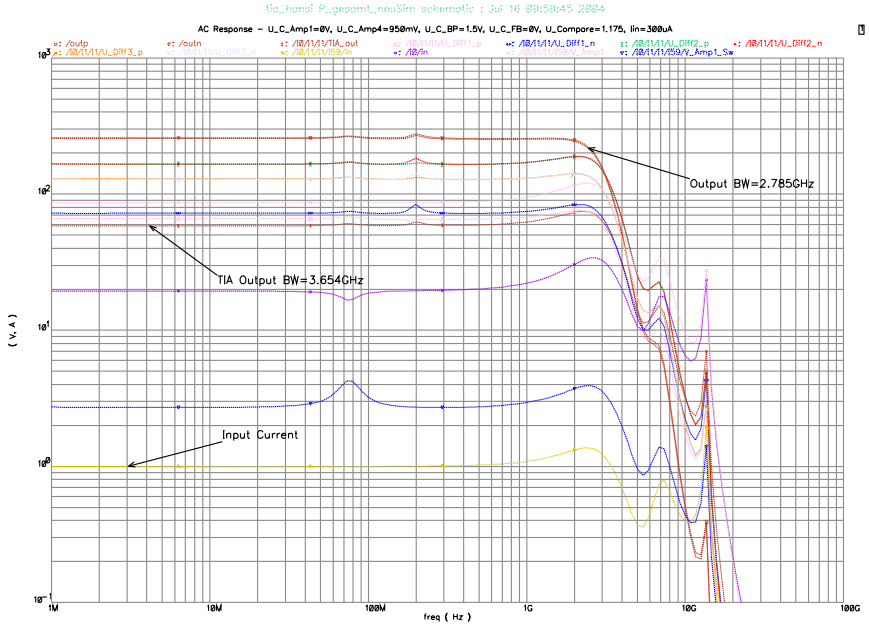
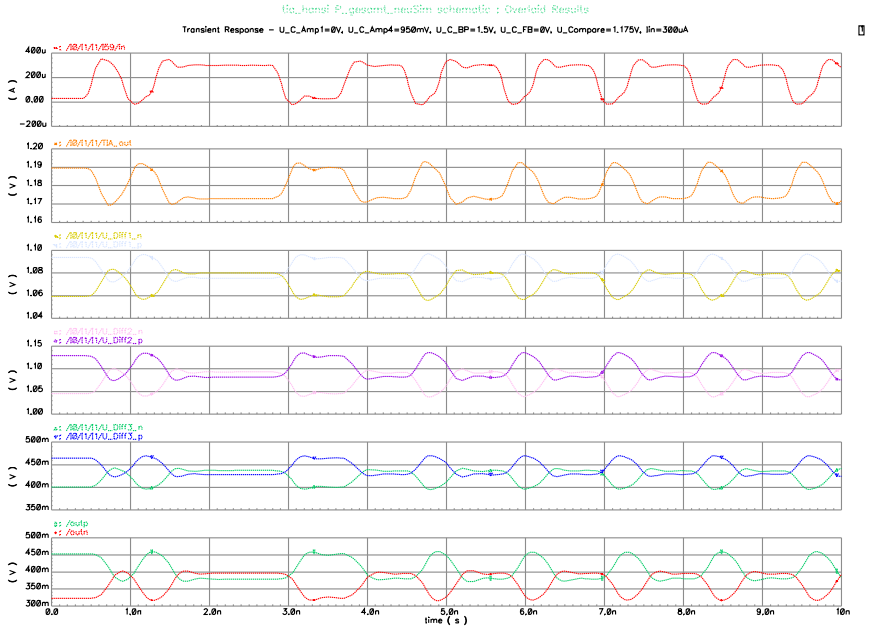


Figure 4.39: Transient analysis for strong input signal (300 μA) at 2.5 GBit/s for the data signal "01011110011011011011011101"



At highest gain the total transimpedance is approximately $R_{\text{chip}} = 32\,\text{k}\Omega$ at a bandwidth of $f_{\text{c,chip}} = 2.09\,\text{GHz}$. This bandwidth is less than for the TIA alone ($f_{\text{c,TIA}} = 2.111\,\text{GHz}$ (with a transipedance $R_{\text{TIA}} = 5.3\,\text{k}\Omega$), see Sec. 4.2.4).

When operating at lowest gain the total transimpedance is approximately $R_{\text{chip}} = 260\,\Omega$ compared to the TIA alone with $R_{\text{TIA}} = 60\,\Omega$. The bandwidth of $f_{\text{c,chip}} = 2.785\,\text{GHz}$ is less than $f_{\text{c,TIA}} = 3.41\,\text{GHz}$ too due to the output amplifier.

4.6.2.2 Switch the gain

The transient analysis result for alternating weak ($3\,\mu\text{A}$) and strong ($300\,\mu\text{A}$) input current for the whole chip is shown in Fig. 4.40. The input data signal "`Data`" normalized to 1 is shown as dark orange pulse train. The output of the TIA "`TIA_out`" is visible around 1.2 V together with the comparison voltage "`U_Compare`". The output signals "`outp`" and "`outn`" are drawn in bold black lines around 400 mV.

After layout the parasitic extraction returned high capacity and resistance of the path from the P&H pulse generator to the P&H circuits. These shorten the pulse which leads to non-optimal conductivity during the closed state of the P&H circuits. Therefore the prepared voltages are not transmitted properly to the hold capacitors. This is not a problem during operation because the prepared voltages simply have to take this into account.

In Fig. 4.40 a piece of the simulation from 150 ns until the end is shown. The first 10 ns shown belong to a burst interval with strong input signal ($300\,\mu\text{A}$). From 160 ns to 180 ns weak input signal was applied ($3\,\mu\text{A}$). In the last interval from 180 ns to 200 ns a strong input signal with $300\,\mu\text{A}$ was applied again.

The markers "`M1`" and "`M2`" denote the time to switch from low gain to high gain which needs 2.3 ns. The switch period from high gain to low gain (marked with "`M3`" and "`M4`") is only 0.8 ns.

Due to limited chip area the supplies could not be stabilized good enough. Additionally the P&H is not absolutely closed during the off period which leads to coupling from the preparation input to the held output voltage. Both effects result in varying DC operating points visible as slowly changing difference in the output signal.

4.6.2.3 Power consumption

In Tab. 4.5 the the supply currents during a typical simulation run are shown. These values are taken from the initial DC operating point solution. Since no measurement of the individual supply currents was possible the simulation results are taken to calculate the power consumption.

Figure 4.40: Chip transient analysis with switch of gain. Switching from low gain to high gain needs 2.3 ns. The reverse processes is finished in only 0.8 ns.

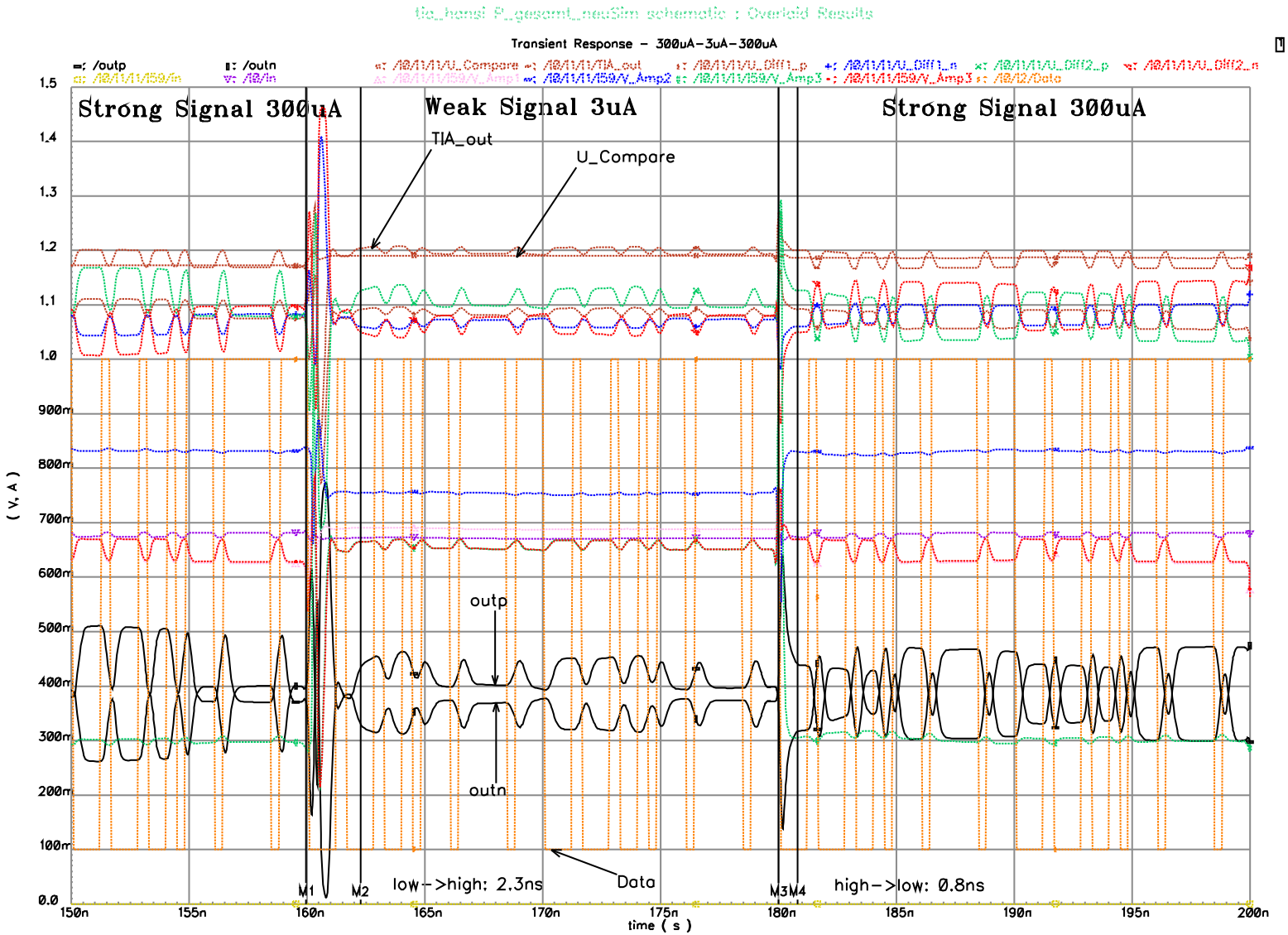


Table 4.5: Power consumption at the supply pads

Supply	Symbol	Current
Vdd_tia	I_{tia}	61.3 mA
Vdd_tiaout	I_{tiaout}	5.2 mA
Vdd_Diff	I_{Diff}	59.5 mA
Vdd_out	I_{out}	67.3 mA
Vdd_dig	I_{dig}	2.0 mA

The TIA alone consumes

$$\begin{aligned} P_{\text{TIA}} &= V_{\text{tia}}\, I_{\text{tia}} + V_{\text{tiaout}}\, I_{\text{tiaout}} \\ &= 1.5\,\text{V}\,(61.3\,\text{mA} + 5.2\,\text{mA}) \\ &= 99.8\,\text{mW}. \end{aligned} \tag{4.10}$$

The total chip consumes

$$\begin{aligned} P_{\text{chip}} &= V \cdot \sum I \\ &= 1.5\,\text{V}\,(61.3\,\text{mA} + 5.2\,\text{mA} + 59.5\,\text{mA} + 67.3\,\text{mA} + 2.0\,\text{mA}) \\ &= 293\,\text{mW}. \end{aligned} \tag{4.11}$$

4.7 Tools

The chip development was completely done with Cadence ICFB and associated tools. The ICFB tool suite contains Virtuoso Schematic Editing, Virtuoso Layout Editing, Affirma Analog Artist and the Spectre simulator.

The design checks (*Design Rule Check (DRC)*, *Electrical Rule Check (ERC)* and *Layout versus Schematic (LVS)*) have been done with the Assura tools.

When the chip layout was completed a GDS file was generated. This was sent to the RAMEZ center of Infineon. They produced the mask data. This had to be verified to the layout in the so called *Job Deck Viewing (JDV)*. The tools used therefore are partly optimized and customized by Infineon.

5

Printed Circuit Boards

THE characteristics of the fabricated chip have been measured. Two special PCBs have been designed and produced therefore. The first *Printed Circuit Board (PCB)* was developed to test the behavior and properties of the chip without switching the gain. The second PCB was specially designed to generate the laser driver signals and to test the switching behavior of the chip.

In this chapter the necessary measurements and the prerequisites are discussed. Afterwards the design of both PCBs is presented in detail.

5.1 Requirements

5.1.1 Measurements

In Sec. 1.3 the required specifications of the chip are given. To measure the actual characteristics of the developed and produced chip, the PCBs have to provide the necessary equipment. The following measurements are to be done

- Principal function
- Analog 3 dB cut-off bandwidth
- Eye diagram
- Minimum average optical input power at specified BERs and bit rates
- Switching behavior

5.1.2 PCB Content

The PCB has to contain the following parts:

- 5 adjustable supply voltages $1.5\,\mathrm{V} \pm 0.1\,\mathrm{V}$
- supply for photodiode
- 6 analog control voltages
- 1 digital control voltage
- 2 digital control signals
- good ground connection
- 2 microstrip lines to SMA connectors for outputs
- chip and photodiode

In the following Secs. 5.2 and 5.3 the circuits for the mentioned parts are described in detail.

5.1.3 PCB base material

The PCB base material is the Rogers RO4003C$^{\mathrm{TM}}$. The data sheet [Rog02] gives the properties of the material as summarized in Tab.5.1.

Table 5.1: RO4003$^{\mathrm{TM}}$ high frequency circuit material properties

Property		**Value**	
ε_r	=	3.48 ± 0.05	
Thermal Conductivity	=	0.62	$^{\mathrm{W}}/_{\mathrm{m\,K}}$
Density	=	1.86	$^{\mathrm{g}}/_{\mathrm{cm}^3}$
Thickness	=	0.508	mm
Copper cladding thickness	=	17	μm

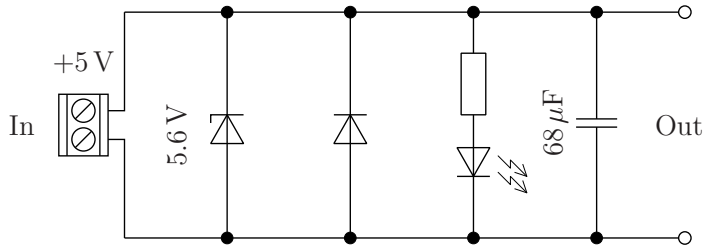
5.2 Static PCB

The first PCB developed was to test everything in the chip except switching behaviour.

5.2.1 PCB Supply

For an easy supply from an external power source a +5 V input was selected. To protect the circuit from too high voltages a 5.6 V Z-diode is in place. Additionally a reverse biased diode protects the circuit from wrong polarity of the supply. A green LED signals the presence of power supply. Figure 5.1 shows the schematic. The power supply of the PD is realized with exactly the same circuit.

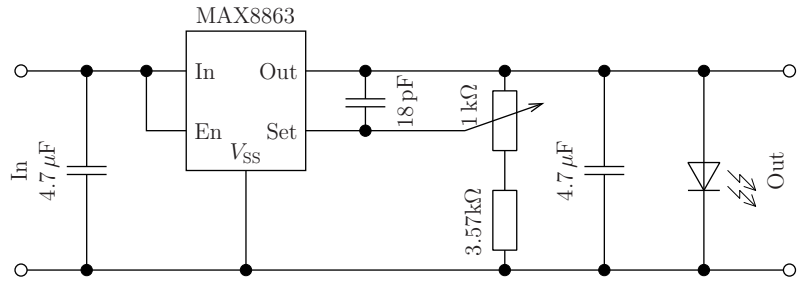
Figure 5.1: Supply for the PCB



5.2.2 Chip Supply

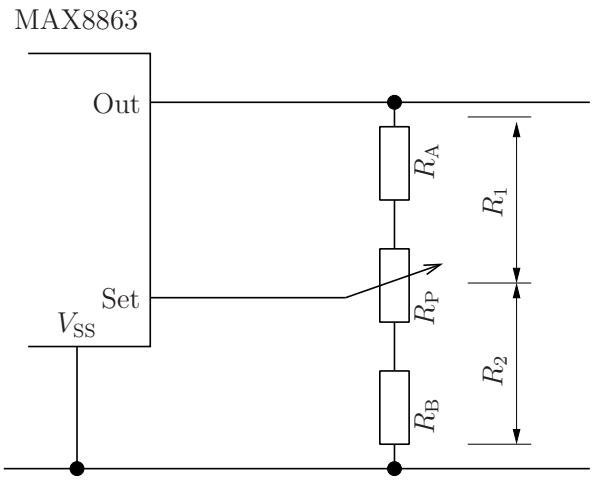
As stated above there are five independent supplies for the chip and one dedicated supply for the control voltages. Each of these supplies sources a maximum current of 100 mA. The output voltage can be adjusted in a range from 1.25 V − 1.6 V. Two special security circuits protect the supplied circuit (i.e. the chip) of too high voltages. Once the adjustment range is limited by a series resistor to the potentiometer. Additionally a LED without series resistor with $V_F \approx 1.6\,V$ limits the output voltage. See Fig. 5.2 for the schematic.

Figure 5.2: Adjustable supply for the chip



The MAX8863 chip is an adjustable *Low Drop Out (LDO)* voltage regulator. It is packaged in a SOT23-5 case. The "En" pin must be tied high to enable the output. The "Set" input is held at $V_{Set} = 1.25\,V$. With an external voltage divider the output voltage can be adjusted.

Figure 5.3: Output voltage adjustment



We want the potentiometer to be limited in its end positions. Therefore series resistors at both sides (R_A and R_B) are planned. The two halves of the total voltage divider are denoted as R_1 and R_2 as shown in Fig. 5.3.

The data sheet [Max98] of the MAX8863 says that the voltage at the Set input is held at 1.25V. Thus the output voltage can be calculated by

$$V_{\mathrm{Out}} = V_{\mathrm{Set}} \left(1 + \frac{R_1}{R_2}\right). \tag{5.1}$$

The minimum output voltage can easily be obtained by setting $\frac{R1}{R2}$ to 0.

$$R_1 = 0 \qquad \Longrightarrow \qquad V_{\mathrm{Out,min}} = V_{\mathrm{Set}} = 1.25\,\mathrm{V} \tag{5.2}$$

The maximum voltage is limited by the input voltage and the voltage drop. We want the output voltage to be limited to $V_{\mathrm{Out}} < V_{\mathrm{Out,max}}$. The feedback ratio has to be setup accordingly.

$$\begin{aligned}
V_{\mathrm{Out}} &= V_{\mathrm{Set}} \left(1 + \frac{R_1}{R_2}\right) \leq V_{\mathrm{Out,max}} \\
1 + \frac{R_1}{R_2} &= \frac{V_{\mathrm{Out,max}}}{V_{\mathrm{Set}}} \\
\frac{R_1}{R_2} &= \frac{V_{\mathrm{Out,max}}}{V_{\mathrm{Set}}} - 1 \\
\frac{R_2}{R_1} &= \frac{V_{\mathrm{Set}}}{V_{\mathrm{Out,max}} - V_{\mathrm{Set}}} \\
R_2 &= R_1 \frac{V_{\mathrm{Set}}}{V_{\mathrm{Out,max}} - V_{\mathrm{Set}}}
\end{aligned} \tag{5.3}$$

In the derivation we used R_1 and R_2 as sum resistance of $R_\mathrm{A} + R_\mathrm{P1}$ and $R_\mathrm{P2} + R_\mathrm{B}$ respectively, where R_P1 and R_P2 are the two partial resistances of the potentiometer. Evidently $R_{P1} + R_{P2} = R_\mathrm{P}$, $0 \leq R_\mathrm{P1} \leq R_\mathrm{P}$ and $0 \leq R_\mathrm{P2} \leq R_\mathrm{P}$.

From the above derivation and the properties of R_{P1} and R_{P2} it is clear that

$$R_\mathrm{A} = 0\,\Omega \tag{5.4}$$

$$R_\mathrm{B} = R_\mathrm{P}\frac{V_\mathrm{Set}}{V_\mathrm{Out,max} - V_\mathrm{Set}}. \tag{5.5}$$

In our case we want to limit $V_\mathrm{Out} \leq V_\mathrm{Out,max} = 1.6\,\mathrm{V}$. With a potentiometer with $R_\mathrm{P} = 1\,\mathrm{k}\Omega$ we get $R_\mathrm{A} = 0\,\Omega$ and $R_\mathrm{B} = 3.57\,\mathrm{k}\Omega$. The maximum leakage current is

$$I_\mathrm{R} = \frac{V_\mathrm{Out,max}}{R_\mathrm{A} + R_\mathrm{P} + R_\mathrm{B}} = \frac{1.6\,\mathrm{V}}{0 + 1\,\mathrm{k}\Omega + 3.57\,\mathrm{k}\Omega} \approx 350\,\mu\mathrm{A}. \tag{5.6}$$

The power dissipation at the MAX8863 LDO at maximum current $I_\mathrm{max} = 100\,\mathrm{mA}$ and with the maximum input voltage $V_\mathrm{In,max} = 5.5\,\mathrm{V}$ is

$$\begin{aligned} P_v &= I_\mathrm{max}\,(V_\mathrm{In,max} - V_\mathrm{Out,min}) \\ &= 100\,\mathrm{mA} \cdot (5.5\,\mathrm{V} - 1.25\,\mathrm{V}) \\ &= 0.425\,\mathrm{W}. \end{aligned} \tag{5.7}$$

The maximum permissible power dissipation is

$$P_\mathrm{max} = \frac{T_J - T_A}{\theta_{JA}} = \frac{150\,^\circ\mathrm{C} - 30\,^\circ\mathrm{C}}{244\,^\circ\mathrm{C/W}} = 0.49\,\mathrm{W}. \tag{5.8}$$

The data sheet recommends an 18 pF capacitor between Out and Set of the MAX8863 LDO for better stability and output ripple.

There is a red LED (Fairchild QTLP630C-7 LED) without series resistor. This is the second step of security. It starts to glow at approximately 1.4 V. This is a "stop sign" when turning at the potentiometer. Additionally its forward voltage is at about 1.6 V which limits the LDOs output voltage. Unfortunately the LED has a quite shallow V/I curve and thus is not really a protection circuit. There are no Z-Diodes or similar available for 1.5 V.

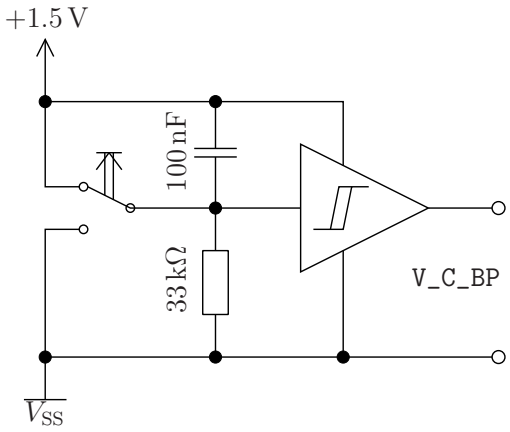
5.2.3 Analog control voltages

The analog control voltages are simply adjusted by a potentiometer. This is connected between 1.5 V and V_SS.

5.2.4 Digital control voltage

The single digital control voltage `V_C_BP` is fed by a digital Schmitt trigger chip (Fairchild NC7SV17P5X). It is a single gate device for low voltage (1.5 V) operation in a tiny SC70-5 package. The input of this Schmitt trigger is set by a switch with a rudimentary de-bounce circuit. See Fig. 5.4 for the schematic. The `V_C_BP` voltage can be measured at a pinhead.

Figure 5.4: Digital control voltage



5.2.5 Digital control signals

The on-chip P&H circuit is controlled from outside the chip by two digital control signals `SHSwitch` and `SHSet`. Both signals are generated exactly as the digital control voltages (see Sec. 5.2.4). The Schmitt trigger IC is a Fairchild NC7WV17P6X which has two gates built in. The output of the Schmitt triggers are connected with a pin head to connect a multimeter.

The most important difference to the Burst PCB is that at the Static PCB we have a very slow circuit to drive `SHSwitch`. In burst mode operation of the chip this is the high speed input pulse to present the prepared control voltages at a precise moment.

5.2.6 Output

The chip's outputs `outp` and `outn` need an external 90 Ω resistor each. Together with the on-chip 200 Ω resistors this yields approximately 50 Ω output resistance. From this point balanced lines to the SMA connectors are necessary. A microstrip line was chosen.

The PCB substrate material Rogers RO4003 with 0.508 mm thickness, 17 μm copper thickness has $\varepsilon_r = 3.38$. The program TXLine and simulations with MicroWave Office yield an optimum width of the strip line $w = 1.145\,\text{mm} = 45.1\,\text{mil}$. The microstrip line was laid out as smooth as possible to avoid reflections.

5.2.7 Chip and photodiode bonds

Both, the chip and the photodiode are glued on the PCB. Therefore a special glue with high silver portion (>80 %) is used. This guarantees high electrical and thermal conductivity. The distance between the chip and the PD is minimized for a very short bond wire to the input pad.

The chip pads are bonded to tiny traces on the PCB. For good adhesion the PCB was gold plated. At the chip and photodiode area the stop mask was excluded. Additional 1 μF chip capacitors for the five supplies of the chip are soldered as close as possible to the chip. They are mounted at the bottom side of the PCB.

Figure 5.5: Chip and photodiode bond layout

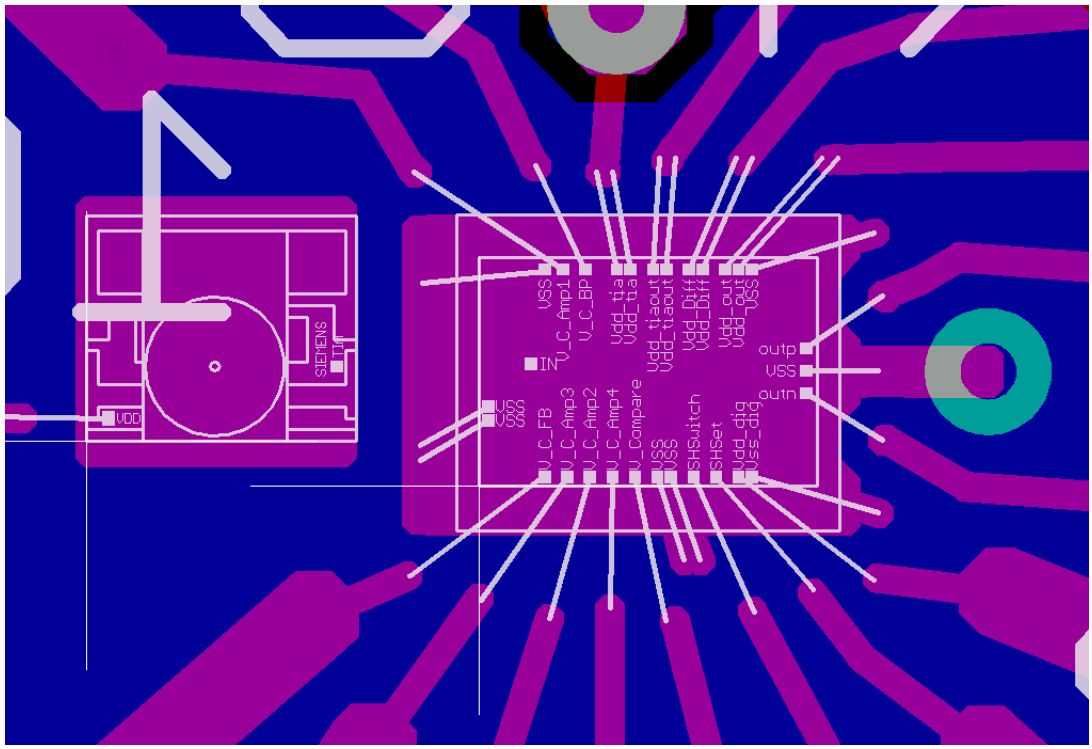
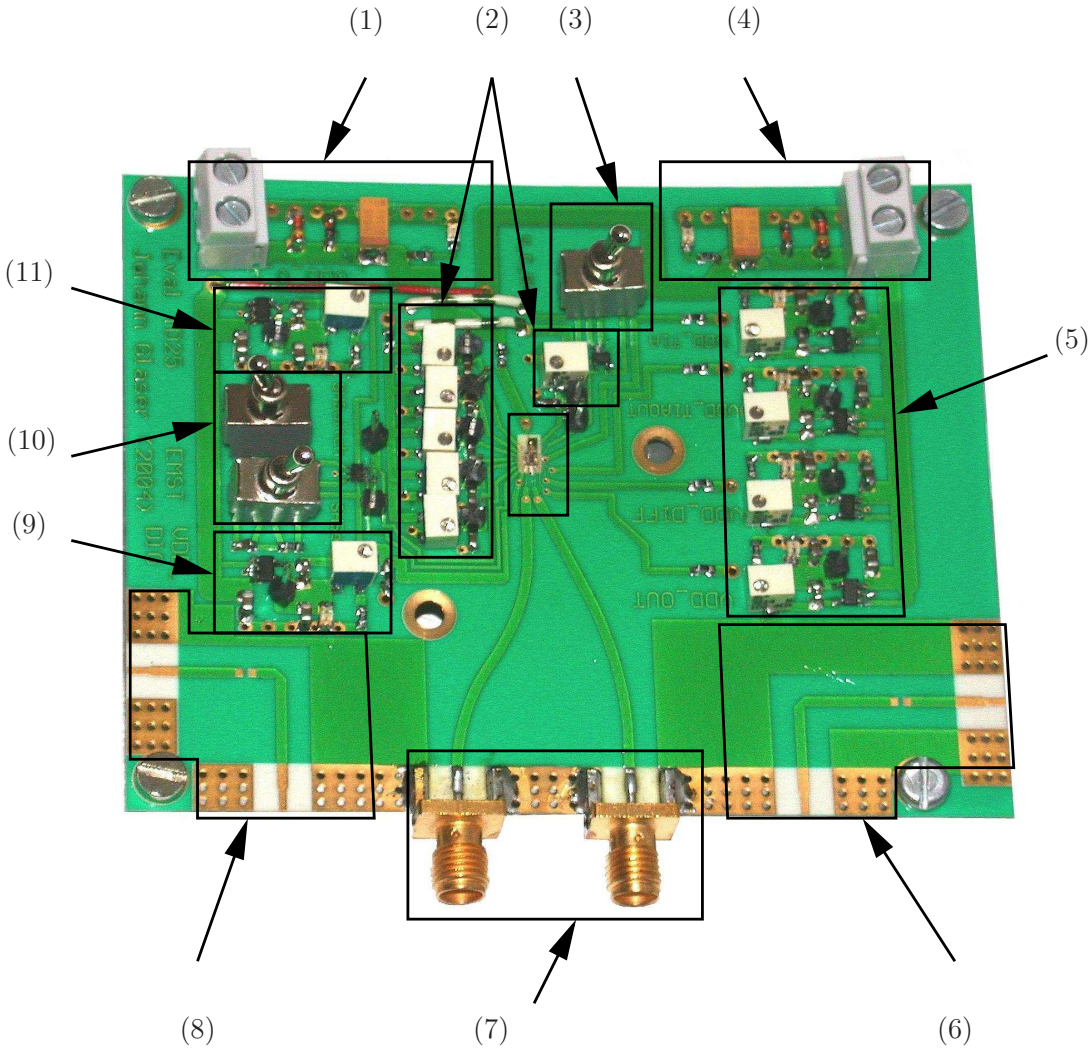


Figure 5.5 shows the PCB layout with the bond wires between chip, PD and the PCB. The distance between the bonding pads on the chip are far smaller than

the PCB DRC rules allow to place traces. To overcome this limitation the bond wires are placed star-like.

In Fig. 5.6 all areas of the PCB are marked. Please read the picture caption for a description of each area.

Figure 5.6: Static PCB photograph: (1) photodiode supply; (2) analog control voltages; (3) digital control voltage; (4) PCB supply; (5) supply voltages for the chip; (6) DC block circuit; (7) output SMA connectors; (8) DC block circuit; (9) supply voltage for the chip; (10) digital control signals (11) supply voltage for the control voltages; The PD and the chip are framed in the center of the PCB.



5.3 Burst PCB

With the Static PCB the chip's behavior at constant gain (i.e. constant control voltages) was measured. The intended operation is to rapidly switch the gain. To test this behavior the Burst PCB is designed.

This section will not deal with the facts already presented in Sec. 5.2. Only the differences and new parts will be discussed. For this PCB the total measurement setup has to be considered. Especially the cable lengths have a great impact on the results because the length of a single bit at 2.5 GBit/s in the cable is just ≈ 65 mm. This implies careful choice of cables and the need for delay devices.

5.3.1 Burst Clock

Each burst consists of a number of bits. For characterization 64, 128, 256, ... bits per burst are used. The bit pattern generator has outputs for the bit clock `Clk` and quarter of that frequency `Clk/4`. The lower frequencies (with more bits in each period) must be generated on the Burst PCB. Big effort was necessary to find fast frequency prescalers for that task.

Finally the Analog Devices *ADF4007 High Frequency Divider / PLL Synthesizer* chip [Ana04] meets the requirements. It can operate up to 7.5 GHz at the input. The division ratio can be set to 8, 16, 32 or 64.

We generate a signal `BurstClk` which is "1" for one burst periode (e.g. with strong optical signal) and "0" for the other burst periode (with weak optical signal). The chip needs a positive edge for each burst periode. We could either use an edge detection circuit to generate a pulse for each rising and falling edge of `BurstClk`.

The easier way is to use the double frequency, or vice versa to half the frequency from the ADF4007's output for `BurstClk`. Thus the output of the ADF4007 is then `BurstClkx2` (see Fig. 5.7). This is halved by a toggle flip-flop (*74LCX112 J-K Flip-Flop* [Fai01] from Fairchild Semiconductor) and results in `BurstClk`.

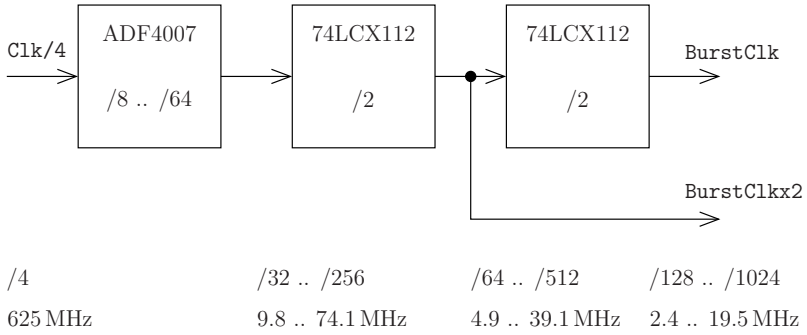
Between the output of the ADF4007 and `BurstClkx2` another toggle flip-flop is in place to create steep edges in the signal. Figure 5.7 shows the block diagram of the frequency divider.

In the picture the division ratio at every point as well as the frequency is noted. The `BurstClk` has a range of 128 to 1024 bits. This can be lowered by using `Clk` instead of `Clk/4` as input of the frequency divider.

5.3.2 Cable lengths and Delay lines

As mentioned before the latency of every edge is important in the measurement setup. Even trace lengths on the PCB have an impact in the range of half a bit

Figure 5.7: Frequency Divider



period. Therefore electronic delay lines are placed on the PCB to compensate these effects. The Maxim / Dallas Semiconductor *DS1020 Programmable 8-Bit Silicon Delay Line* (see [Dal99] for the data sheet) fits best.

The DS1020 has an adjustable delay. Eight digital inputs select 256 equally spaced delay steps. The chip is available in five options with 150 ps, 250 ps, 500 ps, 1 ns and 2 ns steps. The minimum delay of each version is 10 ns at P[7..0] = "00000000". The maximum delay of the 150 ps version is $10\,\text{ns} + 255 \cdot 150\,\text{ps} = 48.25\,\text{ns}$. The 2 ns version has a maximum delay of 520 ns. Both with program input pins P[7..0] = "11111111". The circuit of every delay line including the code switches to set their delay is shown in Fig. 5.8.

Figure 5.8: Schematic of the delay line chip DS1020

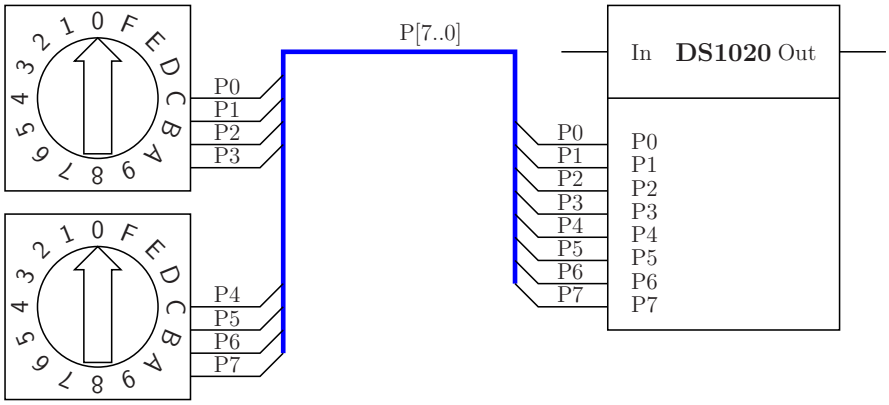


Figure 5.9 shows the measurement setup with all cables and delay lines. The ADF4007 and the first 74LCX112 frequency divider chips are summarized in the single box denoted by "/16 .. /128". The delay lines are t_1, t_4 and t_8. The circuit on the test PCB is surrounded by a dashed line.

Figure 5.9: Delays in the measurement setup

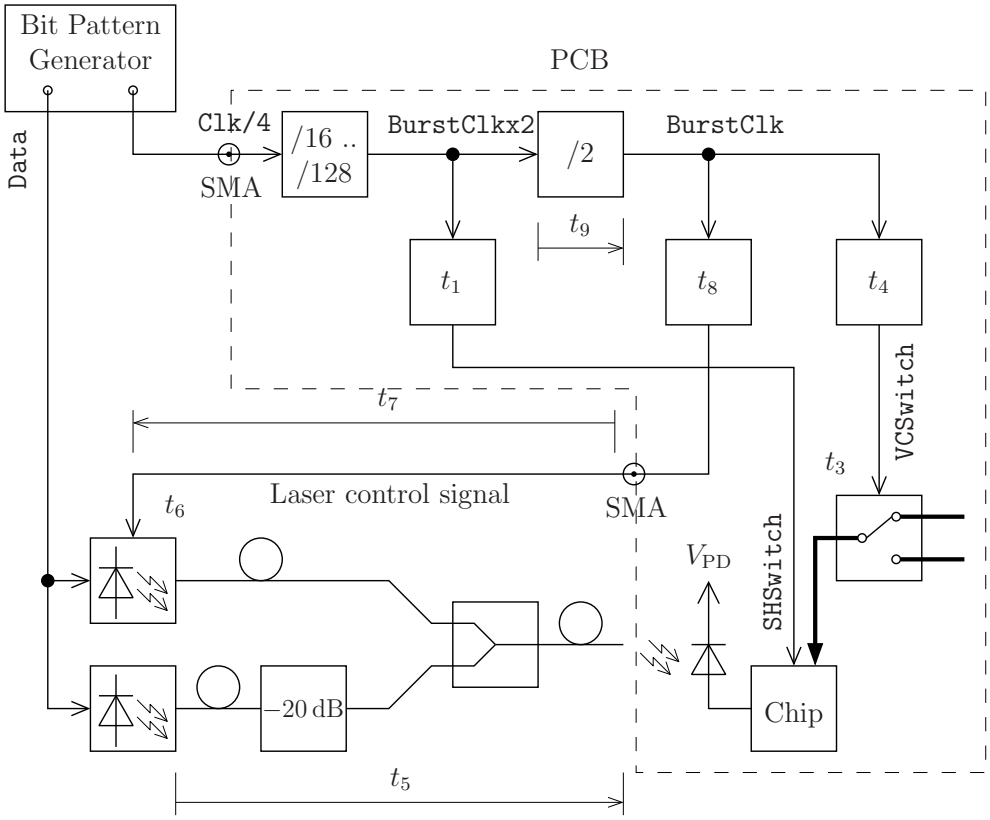


Table 5.2 summarizes every delay contribution. The delay line t_1 is a 150 ps and a 2 ns DS1020 in series, t_4 is a 2 ns version and t_8 is realized with a 150 ps version. In the timing diagram Fig. 5.10 every signal and the relative delay to each other are shown. The sum of all delays from the clock generator to special points is printed too.

From Fig. 5.9 it is clear, that three clock signals are generated.

1. `SHSwitch`
2. `VCSwitch`
3. Laser control signal

`SHSwitch` (with the double frequency of `VCSwitch`) is directly fed to the chip. `VCSwitch` on the other hand is the "Select"-Signal for the switch which selects the control voltages coming from outside. See the next section for details on that. The laser control signal is brought to an SMA connector. A cable connects the test PCB with the laser driver with strong optical power.

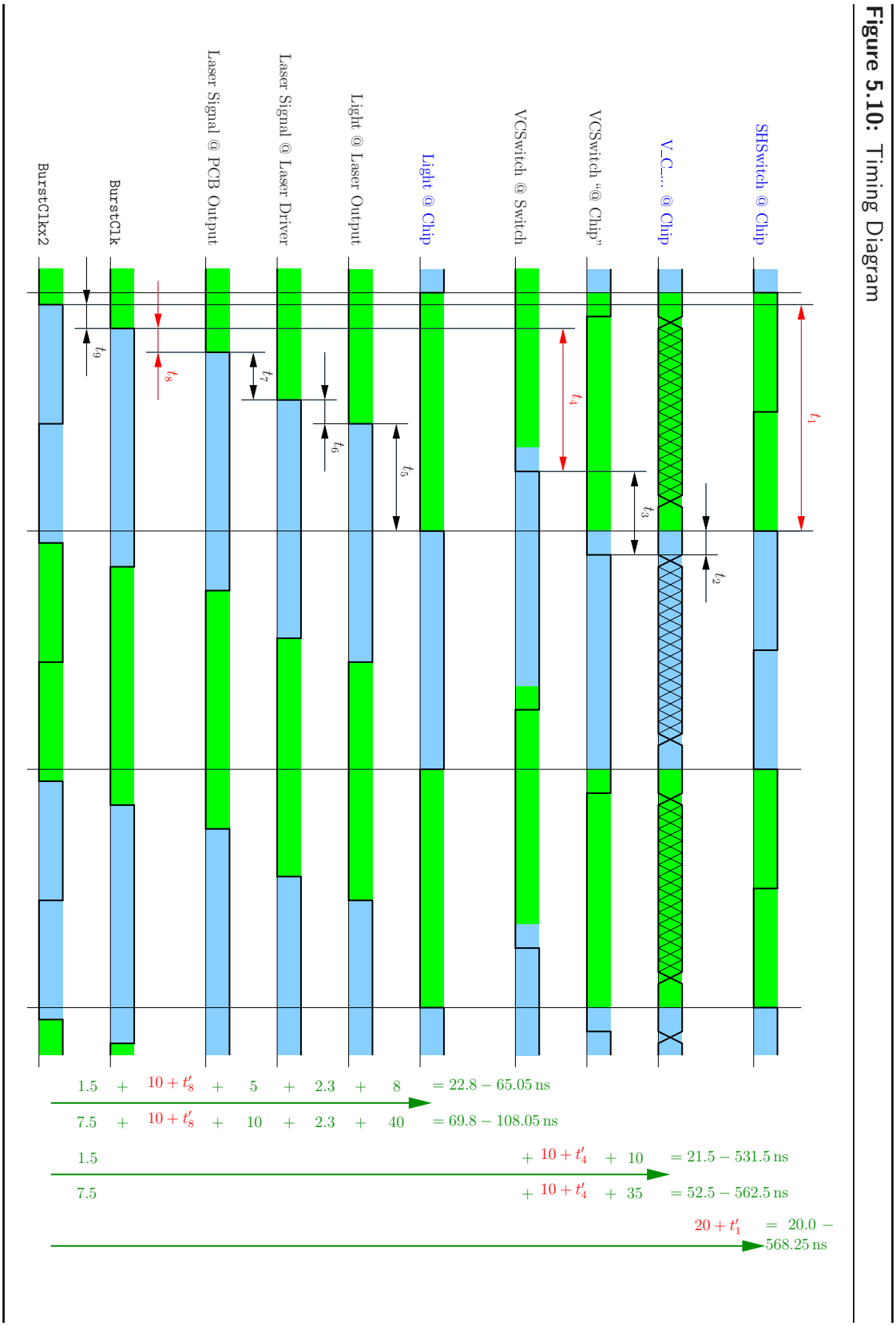


Figure 5.10: Timing Diagram

The laser driver for low intensity is sending without interruption. Its signal is weakened by an attenuator. In the optical multiplexer it is added to the light from the strong laser. The latter is switched off during weak periods.

5.3.3 Control Voltages

The external control voltages must be prepared *before* they are needed. The moment when they are to be applied to the inner circuit is indicated the chip by a positive edge of `SHSwitch`.

5.3.3.1 Adjustment

There are two different sets of control voltages named "A" and "B". They are alternated for every burst period. The signal `VCSwitch` is the select input for the analog Single Pole Dual Throw (SPDT) switches. Figure 5.11 shows a schematic of this circuit.

The *Maxim MAX498 Quad, SPDT, RGB Switch with 250MHz Video Buffer Amplifier* (see [Max96] for the datasheet) was chosen. This chip has four switches (=channels) built in. Every channel has an output buffer with a gain of 2. For a $0 - 1.5\,\mathrm{V}$ output the range of the potentiometers must be chosen accordingly.

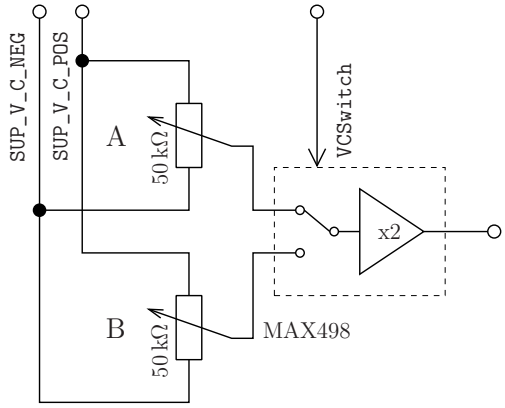
5.3.3.2 Potentiometer supply

The positive and negative supply of the potentiometers is provided by two opamps. Their output voltage can be varied from -0.1 V to 0.8 V. This is achieved

Table 5.2: Timing parameters

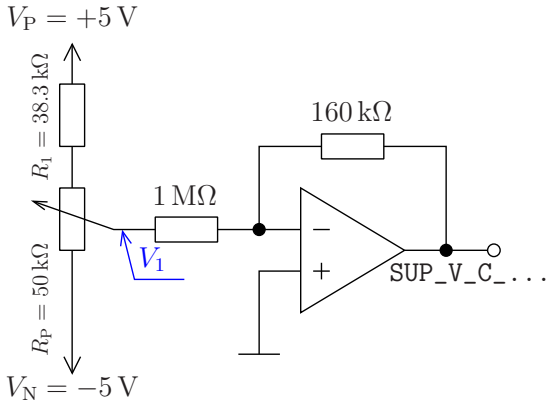
Symbol	Value		Description
t_1	$20 - 568.25$	ns	delay line for `SHSwitch`
t_2	$1 - 3$	ns	t_{hold}: keep the control voltages applied after P&H action
t_3	$10 - 35$	ns	t_{pd} of the analog switch
t_4	$10 - 520$	ns	delay line for the switch signal `VCSwitch`
t_5	$8 - 40$	ns	delay of fiber cable $(2 - 10\,\mathrm{m})$
t_6	2.3	ns	t_{pd} of the laser driver [Max03]
t_7	$5 - 10$	ns	delay of the coax cable from the PCB to the laser driver $(1 - 2\,\mathrm{m})$
t_8	$10 - 48.25$	ns	delay line for the laser control signal
t_9	$1.5 - 7.5$	ns	t_{pd} of the 74LCX112 clock divider (/2)

Figure 5.11: Analog Control voltage switch



with feedback resistors for the opamps and series resistors for the potentiometer. The schematic is drawn in Fig. 5.12.

Figure 5.12: Supply for the analog control voltage potentiometers



The output voltage `SUP_V_C_...` of the opamp should be $-0.1\,V - +0.8\,V$. $+0.8\,V$ results from an input voltage of $V_1 = -5\,V$. A division ratio of

$$G = \frac{0.8\,V}{-5\,V} = -0.16 = -\frac{160\,k\Omega}{1\,M\Omega} \tag{5.9}$$

is necessary therefore. The resistor values are chosen high enough to be able to neglect the load of the previous voltage divider. The input voltage V_1 for an output voltage of $-0.1\,V$ is then given by

$$V_1 = \frac{-0.1\,V}{G} = \frac{-0.1\,V}{-0.16} = +0.625\,V. \tag{5.10}$$

The voltage divider should not allow to adjust V_1 outside the range of $-5\,V$ to $+0.625\,V$. This is easily achieved by adding the resistor R_1. We consider the case

when the potentiometer's tap is at the topmost position. The output voltage V_1 is then given by

$$V_1 = V_N + \left(V_P - V_N\right) \frac{R_P}{R_1 + R_P} \stackrel{!}{=} +0.625\,\mathrm{V} \tag{5.11}$$

Solving this equation for R_1 yields

$$R_1 = R_P \frac{V_P - V_1}{V_1 - R_N} = 50\,\mathrm{k\Omega} \frac{+5\,\mathrm{V} - 0.625\,\mathrm{V}}{0.625\,\mathrm{V} - (-5\,\mathrm{V})} = 38.\overline{8}\mathrm{k\Omega} \tag{5.12}$$

The resistance $R_1 = 38.3\,\mathrm{k\Omega}$ was chosen to have a safety margin if tolerance of the potentiometer is adverse.

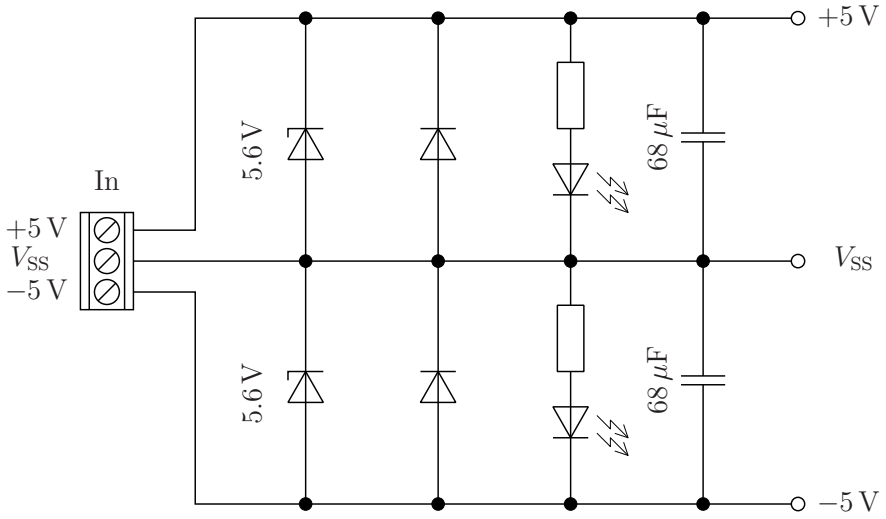
Unfortunately the opamp is unstable for a gain below one $|G| < 1$ and oscillates. Therefore the described approach was removed from the PCB and replaced by a direct V_{SS} connection for `SUP_V_C_NEG` and a flying 0.75 V regulator for `SUP_V_C_POS`.

The digital control voltage `V_C_BP` is also switched via a MAX498. Its two different values are not adjusted via potentiometers but jumpers. The `SHSet` control signal is setup with a jumper too but not switched with the MAX498.

5.3.4 Power Supply

The PCB needs +5 V as well as −5 V. Therefore a bipolar supply is connected at a three-tap clamp. The circuit is similar to the one shown in Fig. 5.1. Figure 5.13 shows this circuit.

Figure 5.13: Supply for the Burst PCB



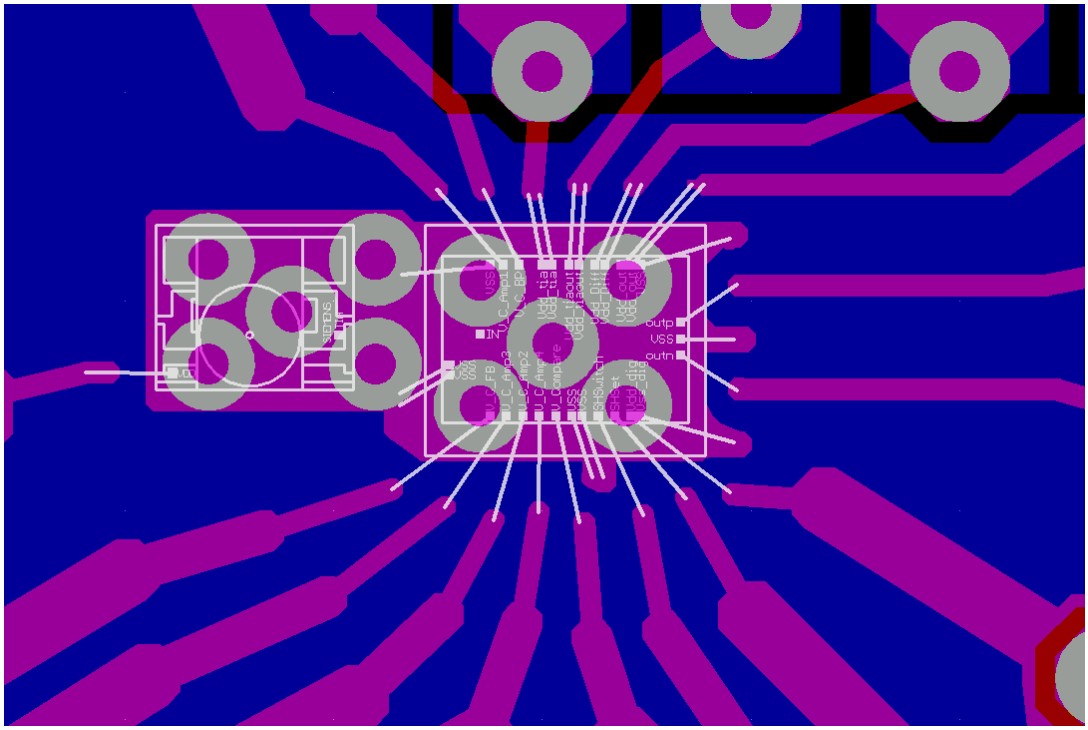
The ADF4007 frequency divider and the 74LCX112 J-K flip-flops are operated at +3.3 V. This voltage is regulated by a *MAX8888 LDO* ([Max01]). A green LED indicates the presence of this supply voltage.

At the static PCB there have been six adjustable supplies in a range of 1.25 V to 1.6 V (using MAX8863 chips). Five of them for the chip and one for the control voltages. At the Burst PCB the control voltages are supplied from the opamps. Thus there are only five MAX8863 mounted.

5.3.5 Chip and photodiode bonds

The principles how the chip is mounted are equal to the static PCB (see Sec. 5.2.7). With the experience from the Static PCB following improvements where incorporated. First of all there was only one via to connect the chip to ground. At the Burst PCB there are many vias directly below the chip for a good ground connection. Figure 5.14 is a screen shot of the layout.

Figure 5.14: Chip and photodiode bond layout



5.3.6 Layout of the Burst PCB

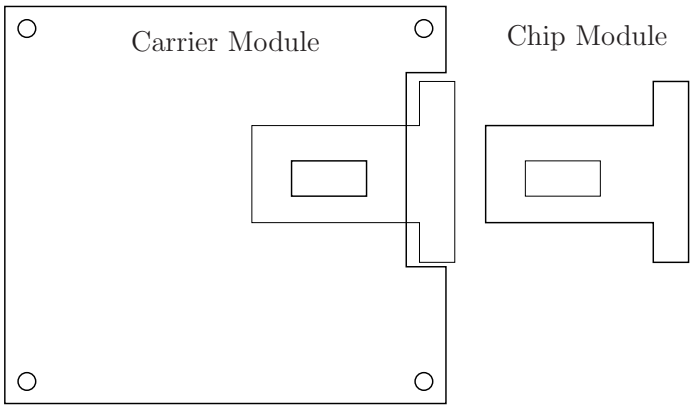
5.3.6.1 Module architecture

The PCB was separated into two modules:

1. Carrier module
2. Chip module

The *chip module* is a tiny board which only holds the chip, the photo diode and the SMA connectors. Everything else is placed at the *carrier module*. The chip module is then "plugged" in the carrier module. Figure 5.15 shows the outline of the modules. The thin lines show the position of the chip module above the carrier module.

Figure 5.15: Supply for the Burst PCB



The carrier module has a rectangular hole right below the chip module. This is exactly at the position of the supply bypass capacitors at the bottom side of the chip module (as indicated by the thin rectangle in the chip module). The two SMA connectors for the output signals `outp` and `outn` are mounted at the right side of the T-shaped chip module. This form is necessary to keep the microstrip tracks without edges.

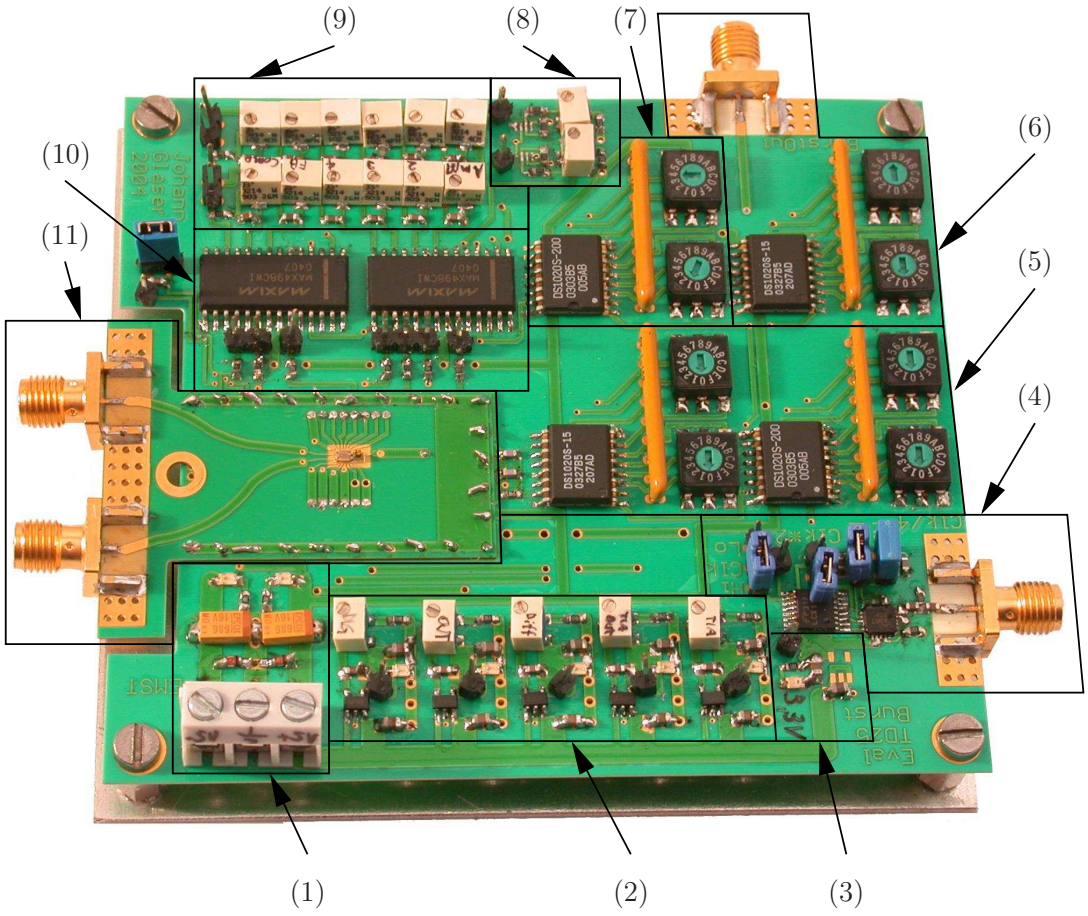
Both modules are connected with wire bridges. Holes on both modules at exactly overlapping positions are used to solder a wire at both sides. These "vias" for the supply and control voltages of the chip are near the border of the rectangular hole. At the circumference of the overlapping area of both modules many additional "vias" are placed to provide a good ground connection.

The advantage of the module architecture are the following:

- for chip related defects only the chip module has to be rebuilt
- easy and save soldering and testing of the carrier module without endangering the chip and its sensitive bonds
- cheaper PCB manufacturing because only the chip modules need to be produced several times (to have some spare parts). This reduces the area.

A photo of the Burst PCB with both modules plugged together is shown in Fig. 5.16. The different areas are marked and described in the caption.

Figure 5.16: Static PCB photograph: (1) PCB supply; (2) supply voltages for the chip; (3) 3.3 V supply; (4) clock input and frequency prescaler; (5) delay line for `SHSwitch`; (6) delay line for the laser control signal; (7) delay line for `VCSwitch`; (8) supply for the control voltages; (9) control voltage sets A and B; (10) analog control voltage switch; (11) chip module with output SMA connectors; The PD and the chip are placed in the center of the chip module.



5.4 Tools

The schematic and layout for the PCBs have been drawn with Eagle made by CadSoft (`http://www.cadsoft.de/`). This is a full featured PCB design tool comparable to expensive products like Cadence Allegro, Protel, PCad and others.

6

Measurements

THE actually produced chip is characterized with a number of measurements. The preparation, the setup and the results are given in this chapter.

6.1 Introduction

This section discusses the desired measurements. The necessary prerequisites as well as the methods are given.

Basically we have to distinguish between static and burst measurements. For static measurements the chip is operated as it would be a receiver for continuous data transmission. The burst measurements characterize the behavior for the very special case of the BMR.

The optical signal is coupled into the InGaAs/InP photodiode SRD00214 [Inf99] on the test PCB. Therefore the carefully cut fiber end is placed directly above it with an appropriate attachment. Note that an open fiber end is used instead of a PD with integrated pigtail because PDs with a pigtail are only available in packages. This would introduce additional capacity and inductivity because no direct bond is possible. The measurement device is connected with $50\,\Omega$ cables to the SMA connectors of the test PCB.

6.1.1 Static Measurements

The chip is driven with a data signal at a given bit rate and optical input power. The data signal is a *Pseudo random bit sequence (PRBS)* signal. Constant control voltages are applied to the chip and forwarded directly to the TIA by setting the signal `SHSet` to a logic "1" (see Sec. 4.3.6).

Figure 6.1: Tektronix CSA8000 Communication Signal Analyzer

The *Eye Diagram* is recorded with an oscilloscope. The Tektronix CSA8000 communication signal analyzer with a dual-channel 80E02 plug-in module (input bandwidth of 12.5 GHz) is used therefore. This device is able to measure Q, the argument of the $\mathcal{Q}$-function as described in Sec. 1.3.3. Figure 6.1 shows a photo from the homepage of its manufacturer `http://www.tek.com/`.

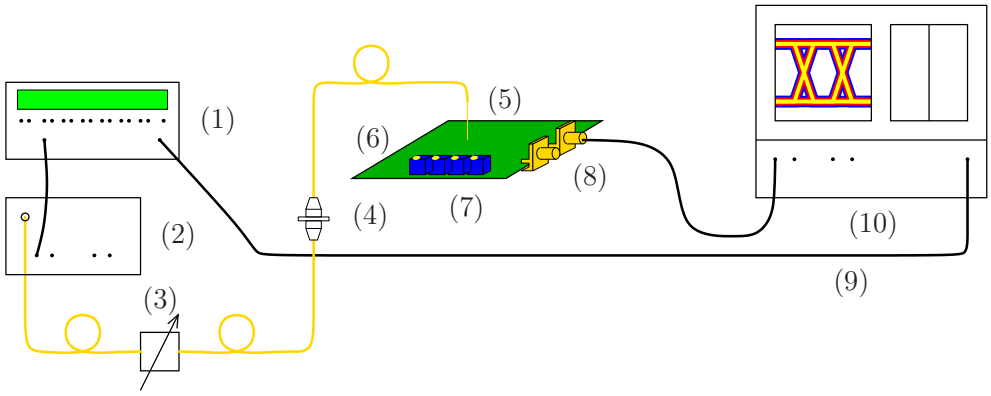
Q and the BER are related with $\mathrm{BER} = \mathcal{Q}(Q)$. Table 6.1 shows typical values.

Table 6.1: Typical values for BER and Q

BER	$\boldsymbol{Q}$
10^{-9}	6
10^{-10}	6.3
10^{-12}	7

The optical power is attenuated until a desired value of Q or BER is obtained. The mean optical power $\overline{P}_{\mathrm{opt}}$ is then measured. This measurement is executed at the last optical connector. The attenuation of the last fiber and the transition into the PD are omitted. This error is determined after all measurements and considered for the final results.

Figure 6.2: Setup for the static measurement of the eye diagram: (1) bit pattern generator; (2) laser driver; (3) adjustable attenuator; (4) last connector; (5) fiber pigtail with open end; (6) test PCB; (7) potentiometers for control voltage; (8) SMA output connectors; (9) bit clock /4 signal for the scope trigger; (10) oscilloscope.



In Fig. 6.2 the principal measurement setup is drawn. The bit pattern generator (1) generates a PRBS at an adjustable data rate. The laser driver (2) feeds the electrical signal to the laser and emits light at $\lambda = 1300\,\text{nm}$. This is conducted via SMFs. An adjustable attenuator (3) is used for continuous adjustment of the optical power $\overline{P}_{\text{opt}}$. The light pulses pass through a connector (4). This is opened to measure $\overline{P}_{\text{opt}}$. Finally the light exits the fiber at the open end (5) and propagates to the photodiode on the test PCB (6).

The output of the chip (8) is fed via a $50\,\Omega$ cable to the oscilloscope (10). The trigger for the scope (9) is derived from the bit clock / 4 output of the bit pattern generator.

6.1.2 Burst Measurements

For the burst measurement the `SHSet` control signal is set to a logic "0". This decouples the externally supplied control voltages from the internally active control voltages. These internal control voltages are "updated" with new values by a positive edge of the `SHSwitch` signal (see Sec. 4.3.6).

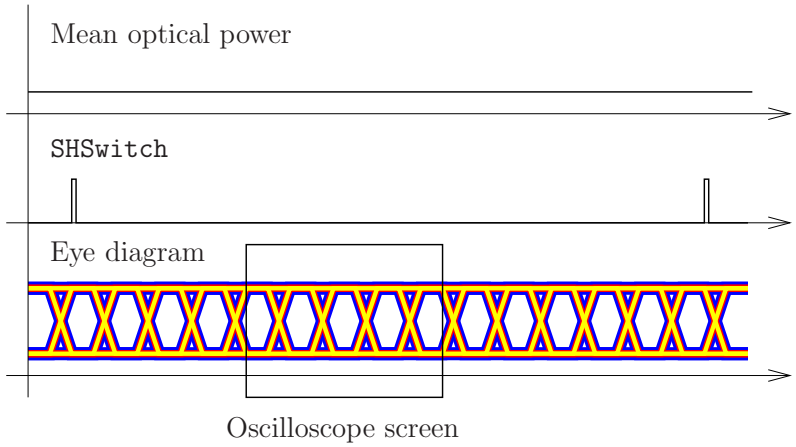
Two scenarios are interesting:

1. constant control voltages
2. alternating control voltages

With constant control voltages the switching behavior and especially the noise characteristics can be determined. It is interesting if noise is lower with decoupled

external control voltages. Therefore a section of the output signal which is well after the last `SHSwitch` pulse and well before the next pulse is triggered and inspected with the oscilloscope. See Fig. 6.3 for an illustration.[1,2] The "silent" or "isolated" environment for the TIA should result in a better noise performance.

Figure 6.3: Section of the output signal



The final and most important measurement concentrates on the moment when the gain is switched. The duration from the switching instant until the signal has settled is measured. Both, switching the gain from high to low as well as from low to high are interesting. Therefore the external control voltages are alternated between two sets of values. One set is dedicated for a weak optical input power, the other set for strong input power. Figure 6.4 shows a schematic example of this test case. The signal distortion and the transient process until the gain has settled is observed with the oscilloscope.

The setup for these measurements already has been shown in Fig. 5.9. Unfortunately the second laser and the according measurement setup was not available in time so no burst measurements could be performed.

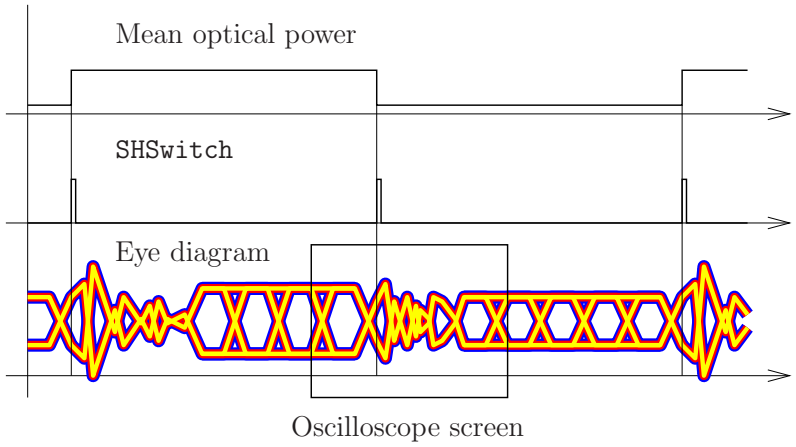
6.2 Eye Diagrams

This section gives the results from measurements with the oscilloscope. The main point of interest is the *sensitivity* of the amplifier. The sensitivity is given as the minimum necessary optical input power $\overline{P}_{\mathrm{opt,min}}$ to achieve a certain BER at a

[1] The distortion of the output signal during the pulse of `SHSwitch` is not drawn.

[2] The figure is meant schematically. Because a sampling oscilloscope is used the drawn section is not really a part of a single burst period.

Figure 6.4: Section of the moment where the gain is switched



given bit rate. As already mentioned earlier, the optical input power is decreased until a certain level of Q (measured with the scope) is reached.

In Tab. 6.2 the measurement results are listed. They show the sensitivity of the characterized chips at certain bit rates and BERs.

The measurements with number 1–8 have been done with the Static PCB (see Sec. 5.2). Number 9–17 where carried out with the Burst PCB (see Sec. 5.3). In both cases the control voltages have been kept constant for the individual bit rates and `SHSet` was set to "1". Even better results could have been obtained if the control voltages were adjusted for every particular optical input power. This was omitted for more time-effective laboratory utilization.

Q was measured with the CSA8000 communication signal analyzer. These values have been used to conclude on the BER. The eye diagrams for the Static PCB (measurements 2–8) are shown in Tab. 6.3. There are no results for BER $= 10^{-10}$ and BER $= 10^{-12}$ at 2.5 GBit/s. The reason is that the necessary optical input power is too high and overloads the chip.

Table 6.4 shows the eye diagrams of measurements 9–17 which have been done with the Burst PCB. The results are almost (at least slightly) better than before. It was even possible to measure high BERs at 2.5 GBit/s.

The total transimpedance (noted as R_{TIA} in Tab. 6.2) is calculated as follows. (Ex = 10). In (1.16) the total transimpedance is given by

$$R_{\mathrm{TIA}} = \frac{\Delta V_{\mathrm{TIA,out}}}{\Delta I}. \tag{6.1}$$

Inserting (1.9) we get

$$R_{\mathrm{TIA}} = \frac{\Delta V_{\mathrm{TIA,out}}}{2R \cdot \overline{P}_{\mathrm{opt}}} \frac{\mathrm{Ex}+1}{\mathrm{Ex}-1}. \tag{6.2}$$

Table 6.2: Corrected results

Nr.	Bit Rate	Q	$\overline{P}_{\mathrm{opt}}$	$\Delta V_{\mathrm{TIA,out}}$	R_{TIA}	$\sqrt{\overline{i^2_{\mathrm{n,in}}}}$
	GBit/s		dBm	mV	kΩ	nA
1	2	6.3	–23.92	53	9.4	448
2	1.25	6	–27.25	48	18.3	218
3	1.25	6.3	–27.01	52	18.8	220
4	1.25	7	–26.39	60	18.8	228
5	2	6	–24.00	110	19.9	461
6	2	6.3	–22.84	160	22.1	574
7	2	7	–20.67	250	21.0	851
8	2.5	6	–17.37	480	18.8	2124
9	1.25	6	–28.20	54	25.7	175
10	1.25	6.3	–27.59	60	24.8	192
11	1.25	7	–26.65	75	24.9	215
12	2	6	–23.93	130	23.1	469
13	2	6.3	–22.55	140	18.1	614
14	2	7	–20.85	150	13.1	817
15	2.5	6	–20.85	350	30.6	953
16	2.5	6.3	–20.41	400	31.6	1004
17	2.5	7	–19.68	450	30.1	1069

In Tab. 6.2 the values for R_{TIA} vary greatly for some test cases due to the alteration of the operating point through change in optical power.

Equation (1.15) gives the RMS input noise current:

$$\sqrt{\overline{i^2_{\mathrm{n,in}}}} = \frac{\Delta I}{2Q} \tag{6.3}$$

Inserting (1.9) here too yields

$$\sqrt{\overline{i^2_{\mathrm{n,in}}}} = \frac{R \cdot \overline{P}_{\mathrm{opt}}}{Q} \frac{\mathrm{Ex}-1}{\mathrm{Ex}+1}. \tag{6.4}$$

For bit rates like 1.25 GBit/s (see measurements 2–4 and 9–11) the signal distortion is purely from noise. The static PCB yields an average RMS input noise level of $\sqrt{\overline{i^2_{\mathrm{n,in}}}} \approx 223\,\mathrm{nA}$ whereas the static measurement at the Burst PCB yields an even lower value of $\sqrt{\overline{i^2_{\mathrm{n,in}}}} \approx 194\,\mathrm{nA}$. This is by far better than the simulation result $\sqrt{\overline{i^2_{\mathrm{n,in}}}} \approx 403\,\mathrm{nA}$ of Sec. 4.2.4.3.

Table 6.3: Eye diagrams for the Static PCB

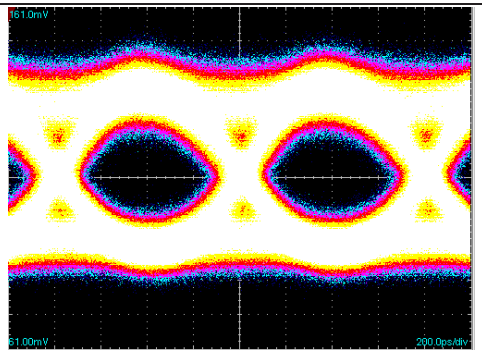
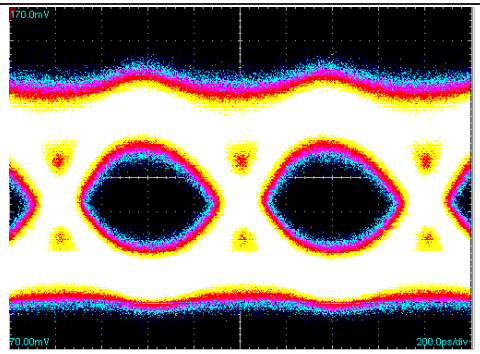
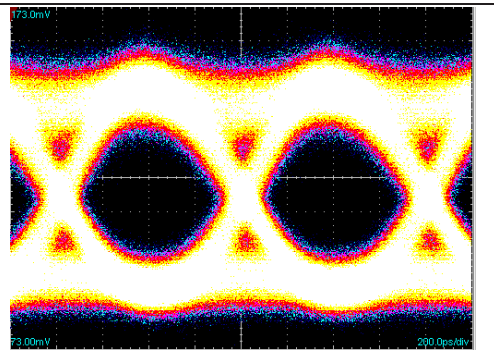
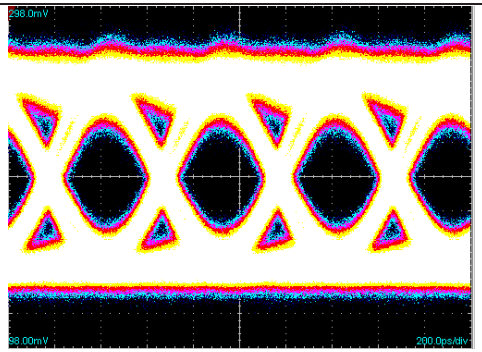
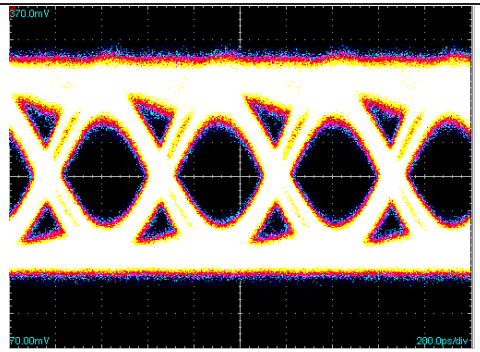
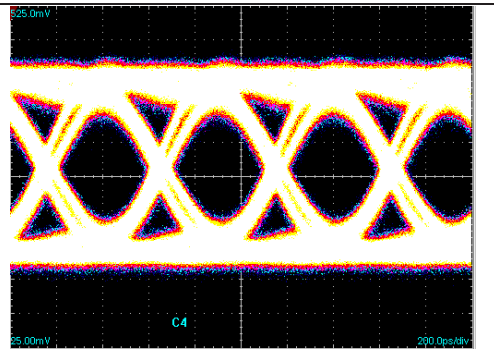
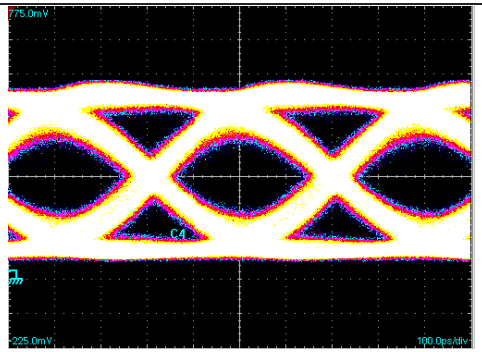
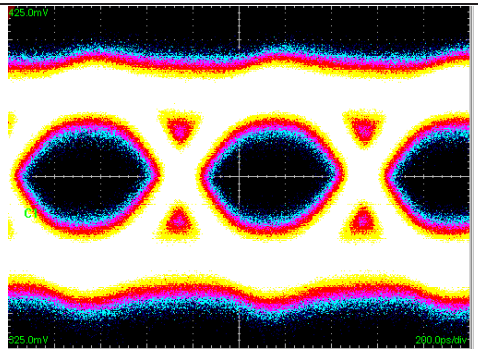
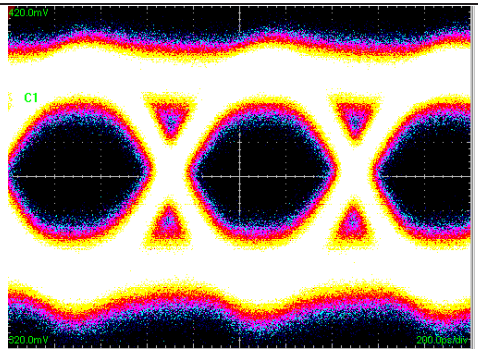
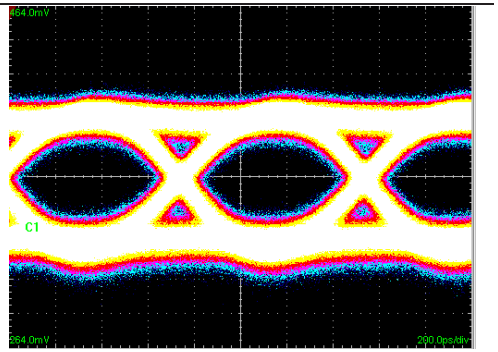
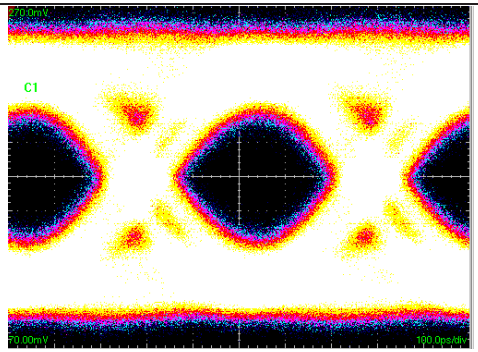
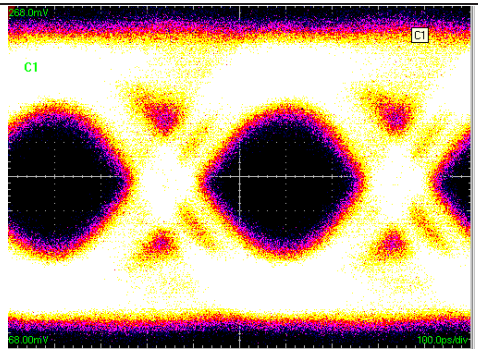
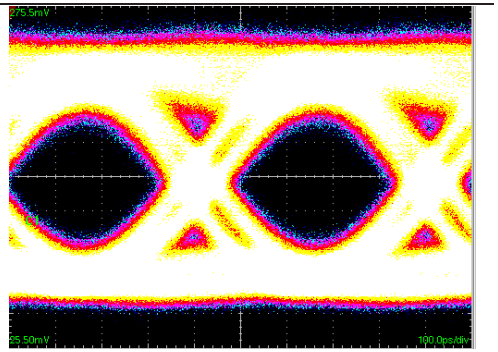
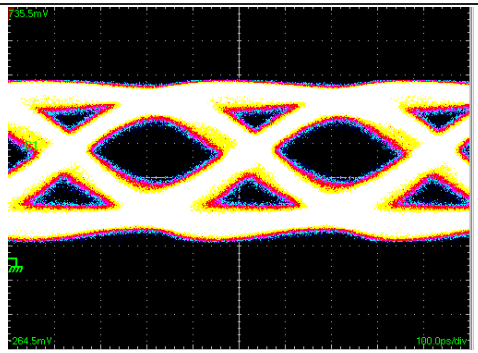
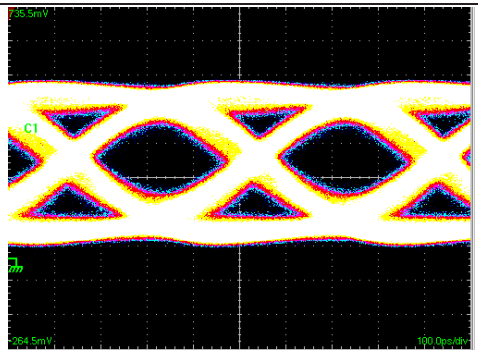
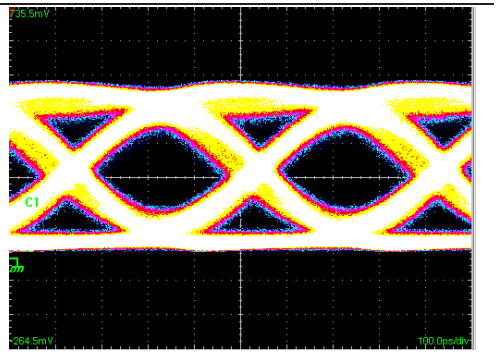
Bit Rate	$Q = 6$	$Q = 6.3$	$Q = 7$
1.25			
2			
2.5			

Table 6.4: Eye diagrams for the Burst PCB in static mode

Bit Rate	$Q = 6$	$Q = 6.3$	$Q = 7$
1.25			
2			
2.5			

Higher bit rates incorporate more signal distortion due to the non-optimum laser[3] as well as the limited bandwidth of the chip itself. The pure noise component of the calculated values in Tab. 6.2 are approximately the same as for low bit rates. The additional "noise" expressed in the high values (up to more than 1000 nA) results from the signal distortion due to limited bandwidth and the laser source. With a better laser the results for high bit rates will be better too.

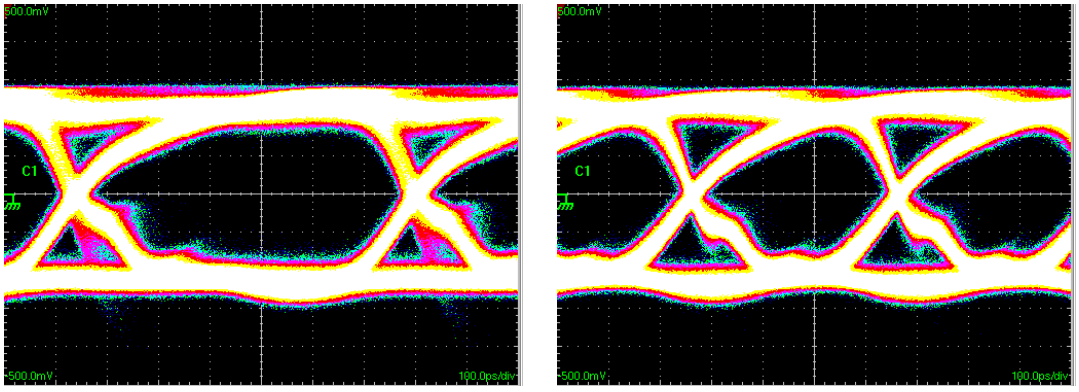
The strong 50 Ω output driver at the developed chip limits the total bandwidth. Unfortunately it is not possible to measure the output of the TIA directly. This would give the real bandwidth which is important for the final chip. Process variations at the developed chip cause different operating point of the output driver stages. This changes their bandwidth so they don't reach the highly optimized values as in simulation.

The sensitivity of −27.6 dBm at BER = 10^{-10} with BR = 1.25 GBit/s is better than the specification requires (see Tab. 1.1) by 4.6 dB but for a lower bit rate as specified. For BR = 2.5 GBit/s the sensitivity of −20.41 dBm does not meet the specification and differs by −2.6 dB. This should be better when using an adequate laser and the specification will be met.

The measurement results differ greatly from the simulated results (including the operating points). This is because the simulation results of the TIA have not been optimized that carefully due to the long analysis duration. When using the chip in a measurement setup it is very easy to change the control voltages and you get the actual results instantly. Therefore optimization of the control voltage values was deferred from simulation to the actual measurements.

At the bottom in Fig. 4.9 the output of the chip is simulated. The shape is quite sinus-like similar to the eye diagrams in Tab. 6.3 and Tab. 6.4. The signal should be more rectangular for a better eye diagram but it is bandwidth limited by the 50 Ω driver.

[3] At 2.5 GBit/s the laser emits a "lobe" inside of the eye diagram (see the right picture). This means that the emitted optical signal already has a very small eye opening with $Q = 7.86$. At 1.25 GBit/s the eye is wide open with $Q = 11.56$ (see the left picture).



6.3 Photons per bit

In this section we want to calculate the number of photons for a single bit at minimum input power.

The optical input power is given as

$$\overline{P}_{\text{opt}} = -27\,\text{dBm} = 2\,\mu\text{W} \tag{6.5}$$

and the bit rate is

$$\text{BR} = 1.25\,\text{GBit/s} \tag{6.6}$$

at a wave length of

$$\lambda = 1300\,\text{nm}. \tag{6.7}$$

The energy of a single photo is given by

$$E_{\text{photon}} = h\,f \tag{6.8}$$

with Planck's constant

$$h = 6.626 \cdot 10^{-34}\text{Js} \tag{6.9}$$

and

$$f = \frac{c_0}{\lambda} \tag{6.10}$$

where we have used the fact that λ is the wavelength in vacuum (despite the wave propagates in the optical fiber). The mean optical power for a logical "1" is given by

$$P_1 = \overline{P}_{\text{opt}} \frac{2\,\text{Ex}}{1+\text{Ex}} \tag{6.11}$$

(see equation (1.6)). We can calculate the energy of a single "1" bit now as

$$E_1 = P_1\,t_{\text{Bit}} = \frac{P_1}{\text{BR}} \tag{6.12}$$

This energy is built up by n_1 photons, each with E_{photon}. This yields the count of photons for a "1" bit as

$$n_1 = \frac{E_1}{E_{\text{photon}}} = \frac{\overline{P}_{\text{opt}}}{\text{BR}} \frac{2\,\text{Ex}}{1+\text{Ex}} \frac{\lambda}{c_0\,h}. \tag{6.13}$$

For the given values a single "1" bit is represented by

$$n_1 \approx 19000\,\text{Photons}. \tag{6.14}$$

7

Summary

A burst mode receiver for passive optical networks was developed. The receiver is built as a transimpedance amplifier with the ability to change the gain within a few bits. For verification of the development a test chip with 50 Ω output drivers was fabricated and characterized.

A 120 nm digital silicon CMOS semiconductor process without analog extensions was used. The receiver was optimized for high sensitivity as well as fast switching of its gain.

7.1 Specifications and Results

A bit rate up to 2.5 GBit is given. The receiver should have a sensitivity better than −23 dBm at a bit error rate of 10^{-10} and is supplied with 1.5 V. The gain should be switched within 1 ns.

7.1.1 Sensitivity

The produced chip provides a sensitivity of $-27.6\,\mathrm{dBm}$[1] at 1.25 GBit and BER $= 10^{-10}$ as given in Tab. 6.2. For a bit rate of 2.5 GBit the sensitivity still is as high as $-20.4\,\mathrm{dBm}$ for the same BER. This number will increase when the chip is characterized with a better laser source. At 2 GBit the sensitivity is $-22.8\,\mathrm{dBm}$.

At a BER $= 10^{-9}$ the sensitivity for 1.25 GBit is $-28.2\,\mathrm{dBm}$. A bit rate of 2 GBit can be detected at $-24\,\mathrm{dBm}$. For the desired 2.5 GBit $-20.85\,\mathrm{dBm}$ are required.

Very low bit error ratios of BER $= 10^{-12}$ where also measured. At 1.25 GBit an optical input power of $-26.7\,\mathrm{dBm}$ were necessary. 2 GBit required $-20.9\,\mathrm{dBm}$ and for 2.5 GBit $-19.7\,\mathrm{dBm}$ were necessary. (Ex = 10, PRBS $2^{31}-1$, $\lambda = 1300\,\mathrm{nm}$)

7.1.2 Switch the gain

Simulations (see Sec. 4.6.2.2) have shown that switching the gain is accomplished within 2.3 ns from low to high. Switching from high gain down to low gain is even done in 0.8 ns. No measurements where done because no appropriate laser and control circuits where available when this thesis was finished.

7.2 Comparison to Literature

Two commercially available TIAs for 2.5 GBit/s are compared to the developed chip. The Maxim MAX3267 reaches a sensitivity of $-24\,\mathrm{dBm}$ at BER $= 10^{-12}$ [Max00] compared to $-19.7\,\mathrm{dBm}$ in this work. MAX3866 reaches $-22\,\mathrm{dBm}$ at unspecified BER [Max99]. Both chips are produced in a (possibly SiGe) bipolar process and work with a 3-5.5 V supply which enables more complex circuits with higher gain than usable at 1.5 V supply. They are not capable to change their gain.

[CL02] shows an amplifier with a sensitivity of $-20.9\,\mathrm{dBm}$ at 1.25 GBit/s and $-17.9\,\mathrm{dBm}$ at 2.5 GBit/s in a CMOS 0.35 μm process. [SKR+01] presents $-17.1\,\mathrm{dBm}$ at 2.5 GBit/s with BER $= 10^{-10}$ and is produced in a deep-trench DRAM technology. Both have approximately 3 dB less sensitivity than the developed chip in this thesis.

The chip presented in [SZW04] has a sensitivity of $-28.2\,\mathrm{dBm}$ at 1.25 GBit/s and BER $= 10^{-10}$ compared to $-27.6\,\mathrm{dBm}$ determined for the chip developed in this thesis. Both chips are produced in the same CMOS 120 nm process.

[1] all sensitivity values are given as average optical power $\overline{P}_{\mathrm{opt}}$

It is difficult to find literature for receivers at 2.5 GBit/s but a 3 GBit/s receiver with integrated PD was found at [RAN04]. The sensitivity is −19.6 dBm at 3 GBit/s compared to −20.4 dBm at 2.5 GBit/s both at BER = 10^{-10}.

Dedicated burst mode receivers with switchable gain (soft-loud range approximately 20 dB) for 1.25 GBit/s are presented in Tab. 7.1.

Table 7.1: Comparison to other works

Work	**Sensitivity** dBm	**BER**	**max. BR** GBit/s	$\mathbf{t_{Switch}}$ ns	**Process**
[LLO+04]	−22	10^{-12}	1.25	300	CMOS 180 nm
[OYB+04]	−30.2	10^{-10}	1.25	25.6	SiGe BiCMOS 350 nm
[KHLC04]	−27	10^{-12}	1.25	74	CMOS 350 nm
[SHL+03]	−29	unkn.	1.25	15-40	CMOS 180 nm
[HL03]	−27	10^{-12}	1.25	74	unknown
this work	−26.7	10^{-12}	2.5	0.8-2.3	CMOS 120 nm

All of them except the first have better sensitivity. Especially for the SiGe BiCMOS chip described in [OYB+04] which is combined with an APD with multiplicator $m = 6$ this is no surprise[2]. On the other hand, the developed chip outperforms these works by far with the time to switch the gain $t_{\text{Switch}} = 0.8 - 2.3$ ns.

The developed chip complies to the IEEE 802.3ah "Ethernet in the First Mile" specification" [Ins] demanding −27 dBm and surpasses the time to switch gain (specified as 512 ns laser on/off time plus 400 ns receiver settling time) by two to three orders of magnitude. The more stringent ITU-T G.984.2 recommendation [Int] specifies a maximum of 25.6 ns to switch the gain which is surpassed by more than one order of magnitude.

By the best knowledge of the author there are no published BMRs at 2.5 GBit/s so no comparison can be done yet. Compared to all other published works the transimpedance of the TIA $R_{\text{TIA}} = 7\,\text{k}\Omega$ itself is higher by a factor of $1.4 - 4.5$.

7.3 Possible Improvements

During and especially after the development some ideas for improvements where collected. They are summarized in the following list.

[2] A factor of 6 means an improvement by 7.8 dB what reduces the sensitivity of -30.2 dBm down to -22.4 dBm.

- Move the inverters of `Pulse_p` and `Pulse_n` directly to the P&H at the top left and the bottom left.
- Increase capacities for supply as chip area allows.
- Try if shunt resistors for supply between the pad and the capacitors yield better supply stability.
- Decrease the crosstalk of P&H when switched off.
- Use pcell FETs (digital CMOS) for inverters.
- Use dummy resistors for every resistor.

7.4 Conclusion

A burst-mode receiver for passive optical networks is presented. It operates at a bit-rate of 2.5 GBit/s with a sensitivity of -20.4 dBm at BER $= 10^{-10}$. When a better laser source is available, this result will be re-determined and is expected to be better by $2 - 4$ dB. At 1.25 GBit/s the sensitivity is -27.6 dBm which is similar to other currently published works.

The time to switch the gain from low to high (i.e. strongest input signal followed by the weakest) is only 2.3 ns which is better by more than one order of magnitude to any published work. The time to switch from highest gain to lowest is even shorter – 0.8 ns – which means a loss of only two bits at 2.5 GBit/s.

A

Abbreviations

ADSL	Asymmetric Digital Subscriber Line	22
APD	Avalanche Photo Diode	20
BER	Bit Error Ratio	8
BJT	Bipolar Junction Transistor	25
BMR	Burst Mode Receiver	2
CDR	Clock/Data Recovery	21
CSMA/CD	Carrier Sense Multiple Access with Collision Detection	12
DAC	Digital to Analog Converter	62
DRC	Design Rule Check	82
EAM	Electro-optical Absorption Modulator	15
ERC	Electrical Rule Check	82
ESD	Electro-static Sensitive Device	77
FET	Field Effect Transistor	26
FTTB	Fiber To The Building	1
FTTC	Fiber To The Curb	1
FTTD	Fiber To The Desk	1
FTTH	Fiber To The Home	1
FTTO	Fiber To The Office	1
FTTx	Fiber To The x	1
JDV	Job Deck Viewing	82
JFET	Junction Field Effect Transistor	26
LDO	Low Drop Out	85
LED	Light Emitting Diode	14

LVS	Layout versus Schematic	82
MAC	Medium Access Control	22
MMF	Multi Mode Fiber	16
MOSFET	Metal Oxide Semiconductor Field Effect Transistor	26
MZM	Mach Zehnder Modulator	15
PCB	Printed Circuit Board	83
PD	Photodiode	2
P&H	Prepare and Hold	62
POF	Plastic Optical Fiber	16
PON	Passive Optical Network	1
PRBS	Pseudo random bit sequence	104
SiO_2	Silicon dioxide	16
SMF	Single Mode Fiber	16
SNR	Signal to Noise Ratio	9
SoC	System on Chip	3
SPDT	Single Pole Dual Throw	95
TDMA	Time Division Multiple Access	12
TDM	Time Division Multiplex	2
TIA	Trans-impedance Amplifier	3
WDD	Wavelength Division Duplex	22
xDSL	x Digital Subscriber Line	1

B

List of Symbols

Symbol	Description
B	bandwidth
BR	Bit Rate
BER	Bit Error Ratio
c_0	light speed in vacuum $c_0 = 299,792,458\,\mathrm{m/s}$
C'_{ox}	oxide capacity normalized to area
C_T	total input node capacity
C_{GS}	FET gate–source capacity
C_{GD}	FET gate–drain capacity
e	electron charge $e = 1.602 \cdot 10^{-19}\,\mathrm{As}$
η	external quantum efficiency
Ex	Laser Extinction Ratio
f	frequecny
$f_{\mathrm{c,chip}}$	3 dB cut-off frequency of the total chip
$f_{\mathrm{c,TIA}}$	3 dB cut-off frequency of the total TIA
f_T	transit frequency
Δf	bandwidth
G_o	open loop gain
g_m	transistor small signal conductivity
h	Planck's constant $h = 6.626 \cdot 10^{-34}\,\mathrm{Js}$
$\hbar$	Planck's constant $\hbar = \frac{h}{2\pi}$
I	current
I_0	input current for a logic "0"

Symbol	Description
I_1	input current for a logic “1”
$I_{1,\max}$	Maximum Input Current for a logic “1”
$I_{1,\min}$	Minimum Input Current for a logic “1”
$\sqrt{\overline{i^2_{\mathrm{n,in}}}}$	input referred RMS noise current
$\overline{i^2_{\mathrm{n,R}}}$	noise current densitiy of a resistor
$\overline{i^2_{\mathrm{n,i}}}$	input referred noise current density
$\overline{i^2_{\mathrm{n,A}}}$	input referred noise current density of an amplifier
ΔI	input current amplitude
I_{D}	FET drain current
r_{DS}	FET small signal drain–source resistance
t	time
t_{switch}	Amplification switch time
t_{Bit}	Bit duration
V_{A}	Early voltage
V_{DD}	supply voltage of the chip
V_{DS}	FET drain–source voltage
V_{GS}	FET gate–source voltage
V_{th}	threshold voltage
V_{PD}	photo diode supply voltage
$\Delta V_{\mathrm{TIA,out}}$	Output voltage of the TIA
$\overline{v^2_{\mathrm{n,R}}}$	noise voltage densitiy of a resistor
$\overline{v^2_{\mathrm{n,i}}}$	input referred noise voltage density
$\overline{v^2_{\mathrm{n,A}}}$	input referred noise voltage density of an amplifier
W	gate width

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