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DISSERTATION

Semiconductor devices and integrated circuits under short electrical stress

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Wien, im Februar 2012 .....

To
my mother

and
in memory of my father

Kurzfassung

Die Fortschritte bei der Verkleinerung der internen Strukturen in modernen elektronischen Geräten und der einhergehenden Verringerung der Betriebsspannungen von integrierten Schaltkreisen haben zu einer Erhöhung der internen Belastungen während elektrostatischer Entladungen (ESD) geführt. Deshalb müssen Schutzstrukturen, welche die auftretenden Überspannungen während ESD auf unkritische Werte begrenzen, ständig verbessert werden, um die zuverlässige Funktion von integrierten Schaltkreisen und elektronischen Systemen zu garantieren. Ebenso stellt die Vermeidung von Latch-up – eine Bezeichnung für unkontrollierbaren Stromfluss in der Stromversorgung – eine fortwährende Herausforderung für integrierte Schaltkreise dar. Mit jedem Verkleinerungsschritt werden die Abstände der internen Strukturen kleiner und deshalb steigt die Latch-up-Empfindlichkeit an. Trotz heutiger Simulationsmöglichkeiten ist in vielen Fällen eine experimentelle Untersuchung des internen Bauteilverhaltens unerlässlich. Dies ermöglicht ein besseres Verständnis des eingetretenen Verhaltens und erlaubt darüber hinaus eine Anpassungen der Simulationsmodelle.

Das transiente interferometrische Abbildungsverfahren (TIM), welches am Institut für Festkörperelektronik an der TU-Wien entwickelt wurde, erlaubt den experimentellen in-situ Zugriff von der Bauteilrückseite auf die interne freie Ladungsträger- und Temperaturverteilung in Halbleiterbauelementen. Mit diesem Verfahren konnten die gleichförmige Aktivierung sowie die Skalierungseigenschaften von einzel- und multifinger ESD-Schutzstrukturen untersucht werden. Entdeckte Puls-zu-Puls Instabilitäten in der Bauteilspannung und die Stromdichteverteilung innerhalb der Transistorfinger konnten detailliert von kleinen Strömen bis über die Belastungsgrenze hinaus analysiert werden. Die Ursache der auftretenden Stufen in den Strom-Spannungskurven konnten Instabilitäten im Aktivierungsmuster zugeordnet und mit Simulationen verifiziert werden.

Im Rahmen dieser Arbeit wurden die Messeinrichtungen unter anderem um die Möglichkeit von transienten Latch-up-Tests erweitert, um den Stromfluss im Substratmaterial als Ursache für externes transientes Latch-up eingehend untersuchen zu können. Für unterschiedliche Anordnungen und Ladungsträgerpolaritäten wurde die freie Ladungsträgerkonzentration analysiert und mit Simulationen ergänzt. Gebiete mit latch-up-kritischer freier Ladungsträgerkonzentration konnten lokalisiert, Optimierungsvorschläge erarbeitet und ein Fallbeispiel eines transienten Latch-up-Problems in einem kommerziellen Stromregelungsbaustein eingebracht werden. Die dargestellten Experimente erklärten den dynamischen Latch-up-Mechanismus und die höhere Latch-up-Empfindlichkeit für kurze Pulse.

Abschließend wurden inhomogenitäten in der Temperaturverteilung in einem geöffneten H-Brücken-Treiberbaustein während seines Betriebs in einem Beispielschaltkreis aufgedeckt. Es wurde festgestellt, dass die Ausgangstransistoren von der eingebauten Temperaturschutzschaltung nicht ausreichend geschützt wurden.

Abstract

Ongoing progress in down-scaling internal features in modern electronic devices and the corresponding lowering of operating voltages in integrated circuits have led to an increase in internal stress during electrostatic discharge (ESD) events. Thus, protective structures which clamp transient voltages during ESD to safe levels need to be continuously improved to guarantee reliable function of integrated circuits and electronic systems. Furthermore, prevention of latch-up – a synonym for an uncontrollable current flow in the power supply – is a continuing challenge for bulk silicon integrated circuits. The distances of the internal structures decrease with down-scaling, and consequently the sensitivity to latch-up increases. Even with state-of-the-art possibilities for device simulation, an experimental investigation of the internal behavior of semiconductor devices is inevitable in many cases. The experimental results allow a better understanding of the occurring device behavior and adjustments to the simulation models.

The transient interferometric mapping (TIM) method, which was developed at the Institute of Solid State Electronics at the Vienna University of Technology, provides in-situ experimental access to the internal excess charge carrier and temperature distribution from the backside of semiconductor devices. Based on this method, the triggering uniformity as well as the scaling behavior could be investigated in single and multi-finger ESD protection devices. The observed pulse-to-pulse instabilities in device voltage and the current distribution within the fingers of the transistors were analyzed in detail, from low currents up to the destruction level. The origin of observed steps in the pulsed current-voltage (I-V) characteristics could be related to instabilities in the triggering pattern. This finding was verified by device simulations.

Additionally, the TIM setups were adapted and enhanced with a facility for transient latch-up (TLU) testing to perform intensive analysis of substrate current flow acting as a trigger for possible external transient latch-up. The transient excess carrier concentration was studied for various layout configurations and injection carrier types and the results were complemented with device simulations. Regions with latch-up critical excess carrier concentration were identified and hints for layout optimizations were prepared. A case study of a transient induced latch-up problem in a commercial power control device was presented. The experiments revealed the dynamic latch-up triggering mechanism and the higher latch-up sensitivity for short pulses.

Finally, hot spots in an opened H-bridge driver IC were uncovered in-situ during full operation in an application board. It was found, that the output transistors were not sufficiently protected by the built-in thermal shutdown circuit.

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Contents

Chapter 1

Introduction

Nowadays, microelectronic devices are widely accepted and appreciated by society and they are used nearly everywhere in modern life. Due to mass production and down-scaling internal features from micro- to nanometer-scale, integrated circuits (ICs) get continuously cheaper and higher functionality. They make our life easier (e.g. mobile phones), more comfortable (e.g. remote controls) and safer (e.g. electronic stability control in automobiles).

1.1 Motivation

Consumer electronics are often exposed to unknown handling in an unknown environment. If the consumers are electrostatically charged – e.g. after walking along carpets – and touch a contact pin of a device electric discharge occurs through the touched pin. Such discharge process is called electrostatic discharge (ESD) and the local power density in an integrated circuit during such a discharge is very high[1]. Electrostatic discharge may lead to malfunction of the stressed pin – or in worst case – to damage of the whole device (e.g. ESD-induced latch-up). Therefore, microelectronics needs to be protected by special ESD protection structures, which prevent damage during such discharges by clamping the transient voltages to safe levels. Ongoing progress in down-scaling internal features in modern electronic devices and the corresponding lowering of operating voltages in integrated circuits have led to an increase in internal stress during ESD events. Thus, protective structures which clamp transient voltages during ESD to safe levels need to be

[1] The later presented ST-5 device sustains 75 W for 100 ns in ∼600 µm×3 µm×3 µm – resulting in roughly 10^{16} W/m^3.

continuously improved to guarantee reliable function of integrated circuits and electronic systems.

With increasing number of input/output (I/O) pins the occupied chip area of the corresponding ESD protection elements gets more relevant and smaller protection elements are desirable. Improvements of already qualified ESD protection circuits are necessary when:

- Next scaling of lithography process is launched – smaller area leads to higher power density.
- Next lower operating voltage is introduced – lower trigger voltage is required.
- Higher demands on device robustness are planned (e.g. in automotive industry) – higher failure currents are necessary.

Another important driving force for improving device robustness are expensive recalls and follow-up costs, if devices mounted in valuable or safety-relevant products (e.g. trigger circuits for airbags) fail in the field. Even with state-of-the-art possibilities for device simulation, an experimental investigation of the internal behavior of semiconductor devices is inevitable in many cases. The experimental results allow a better understanding of the occurring device behavior and adjustments to the simulation models.

The transient interferometric mapping (TIM) method, which was developed at the Institute of Solid State Electronics at the Vienna University of Technology, provides in-situ experimental access to the internal excess charge carrier and temperature distribution from the backside of semiconductor devices. Nano-second time resolution and micrometer space resolution make this method well suited for investigations in the ESD regime. Based on this method, the triggering uniformity as well as the scaling behavior of prototypes for new single and multi-finger ESD protection devices should be investigated. The current distribution within the fingers and current sharing over all fingers of the transistors should be analyzed from low currents up to the destruction level.

Furthermore, prevention of latch-up – a synonym for an uncontrollable current flow in the power supply – is a continuing challenge for bulk silicon integrated circuits. The distances to parasitic silicon-controlled rectifier (SCR) structures decrease with downscaling, and consequently the sensitivity to latch-up increases. Latch-up occurs, when a conductive path (e.g. a parasitic SCR structure or a parasitic bipolar transistor) between the voltage-supply and ground is activated in a circuit. The triggering mechanisms are often substrate currents originating from overshoots due to impedance mismatch, coil discharge, electrostatic discharge or electrical over-stress events. Generally, latch-up leads

to destruction of the circuit – unless the current is sufficiently fast limited by external devices. Thus, a lot of effort is made to reduce substrate currents and to prevent latch-up. Nowadays latch-up protection concepts with various guard-ring structures lead to complex layouts, which cannot be simulated in all details with reasonable effort. Consequently, experimental verification – and in case of problems experimental failure location – is essential.

Substrate currents causing *external* latch-up should be experimentally analyzed in the most prone test structures of *K. Domański*, who performed basic electrical experiments on many different latch-up test structures and stripped-down two-dimensional simulations. The higher sensitivity of these test structures for transient latch-up (TLU) – a three dimensional triggering mechanism is supposed – should be explained by analysis of the substrate current distribution using the TIM method. Therefore, the TIM setup needs to be adapted and enhanced with a facility for transient latch-up testing to perform intensive analysis of substrate current flow acting as a trigger for possible external transient latch-up. The transient excess carrier concentration should be studied for various layout configurations and injection carrier types under several guard-ring bias conditions. Furthermore, commercial I/O cells should be analyzed and hints for layout optimizations should be prepared.

With increasing device complexity, the simulation of integrated circuits gets more and more difficult. The behavior of complex chips cannot be simulated and predicted in all details. Therefore, small units are designed, simulated and for final qualification experimentally verified. The qualified units are collected in libraries for designing more complex integrated circuits. In some cases it might happen that problems occur due to interaction between library elements and the circuit does not behave as expected. Then electrical and optical measurement methods are essential to localize the failure position and analyze its origin. A case study of a transient induced latch-up problem in a commercial power control IC should demonstrate the ability of substrate current analysis in (for us) unknown device layouts. Finally, suspected hot spot problems during reliability tests of an H-bridge driver IC need to be investigated in-situ during full operation in an application board.

1.2 Scope and Outline

In the first Chapter a brief introduction to silicon technologies, electrostatic discharge, latch-up as well as to the state-of-the-art electrical and optical testing methods is given.

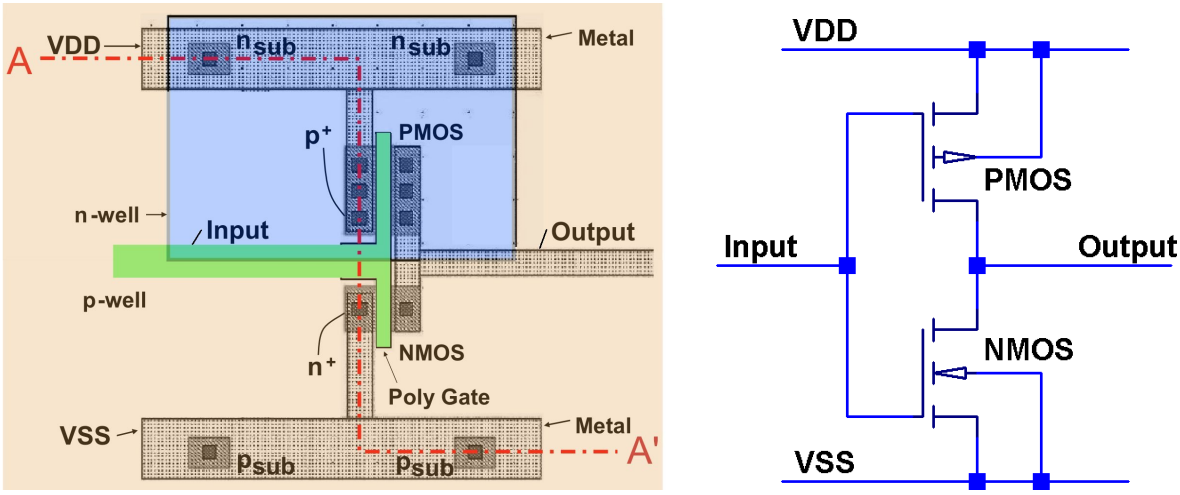
The verification of new ESD protection structures ($\sim$400 µm^2) for ESD libraries is presented in the second Chapter. In the third Chapter, the experiments get more complex with latch-up investigations under several bias conditions and layout configurations with distributed devices. Then, unknown area is entered with latch-up failure analysis of a complete power control device with unknown activity of its circuit elements. A hot spot case study of an opened H-bridge driver IC ($\sim$4 000 000 µm^2) during full operation in an application board is presented in Chapter 4. Finally, Chapter 5 concludes the investigations and shows prospects for future development.

1.3 Silicon technologies

The investigated devices are fabricated in bulk silicon technology and in silicon-on-insulator (SOI) technology. These technologies provide various device types [1] such as diodes, bipolar transistors, p-channel metal oxide semiconductors (PMOS) and n-channel metal oxide semiconductors (NMOS), SCRs etc.

1.3.1 CMOS bulk silicon technology

CMOS (complementary MOS) bulk silicon technology is mostly based on low doped p substrate, where p and n regions are created by diffusion or implantation processes. This technology allows the use of NMOS transistors, which can be placed directly at p substrate or in higher doped p wells as well as the use of PMOS transistors, which are placed in n wells. An exemplary layout section of a usual inverter structure in CMOS technology is shown in Figure 1.1a [2]. The corresponding circuit diagram is shown in Figure 1.1b [3]. The Figures show the PMOS transistor at the top, which can switch the output to *VDD* and at the bottom they show the NMOS transistor, which can switch the output to *VSS*. Both gates are connected to the input and the drain contacts are connected to the output.



(a) (b)

Figure 1.1: CMOS inverter (a) typical layout (after [2]), (b) circuit diagram (after [3]).

The wells of the transistors must be connected to potentials in such a way, that any forward current flow between p and n wells is prevented. This is achieved by reverse

biasing (blocking) these parasitic junctions. This gives the method the name *junction isolation*. The p substrate and the p wells are usually connected with a p_{sub} diffusion[2] to the lowest potential (VSS) and the n wells with an n_{sub} diffusion to the highest potential (VDD).

Parasitic SCR structures

The schematic cross section along A–A' of the layout of Figure 1.1a shows in Figure 1.2a the parasitic *pnp* transistor Q_1 and *npn* transistor Q_2 with their corresponding base resistances R_1 and R_2. The collector of *pnp* transistor Q_1 is the base of *npn* transistor Q_2 and the collector of *npn* transistor Q_2 is the base of *pnp* transistor Q_1. This forms a parasitic *pnpn* junction (SCR structure), which is unavoidable and always present in bulk silicon CMOS circuits. The equivalent circuit is shown in Figure 1.2b. The two bipolar transistors are normally inactive. Thus, no current flow occurs and the base-emitter voltages are negligible.

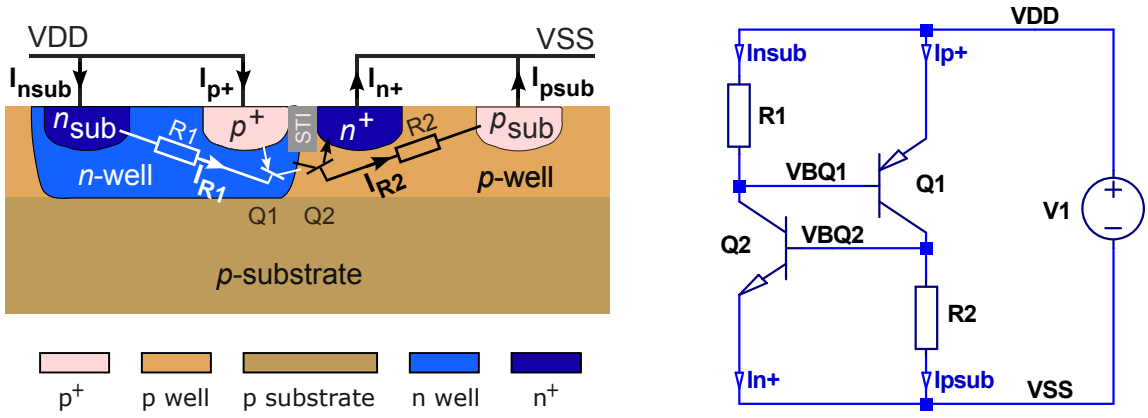


Figure 1.2: (a) Schematic cross section along A–A' of CMOS inverter in Figure 1.1a with parasitic *pnp* (Q_1) and *npn* (Q_2) transistor forming an SCR [4]. (b) Equivalent circuit of parasitic SCR with *pnp* transistor Q_1 and *npn* transistor Q_2.

Under certain circumstances the bipolar transistors might be activated – e.g. if a current[3] across R_1 or R_2 is high enough the corresponding transistor gets active ($V_{\text{BE2}} \simeq 0.6\,\text{V}$ or $V_{\text{BE1}} \simeq -0.6\,\text{V}$). When the resulting voltage drop at the other resistor gets high enough, the second transistor will be activated as well. If the total gain ($\beta_{\text{pnp}} \cdot \beta_{\text{npn}}$) is larger than one, transistor Q_2 keeps transistor Q_1 active and transistor Q_1 keeps transistor Q_2 active

[2] Short for p substrate (p well) contact.
[3] E.g. avalanche current, injected current or displacement current.

– even if the activating event is stopped. That means self-sustaining current flow occurs. This situation is called latch-up and it is usually visible as abrupt increase of supply current[4]. If this latch-up current is not limited sufficiently, the chip will be destroyed. Latch-up types and latch-up protection methods will be discussed in Section 1.5 and Chapter 3.

Thermal issues

A significant advantage of bulk silicon technology is the good thermal conduction of silicon substrate, which allows efficient cooling of devices through the silicon substrate. Some important (temperature dependent) properties of silicon around 300 K [5, 6] are the thermal conductivity $\kappa = 157\,\mathrm{W\,m^{-1}\,K^{-1}}$, the mass density $\rho = 2300\,\mathrm{kg\,m^{-3}}$ and the specific heat $C = 700\,\mathrm{J\,kg^{-1}\,K^{-1}}$. These thermal properties are in the range of aluminum ($\kappa = 235\,\mathrm{W\,m^{-1}\,K^{-1}}$, $\rho = 2700\,\mathrm{kg\,m^{-3}}$, $C = 897\,\mathrm{J\,kg^{-1}\,K^{-1}}$, $D = 9.7 \cdot 10^{-5}\,\mathrm{m^2\,s^{-1}}$).

The thermal diffusivity can be calculated with

$$D = \frac{\kappa}{\rho C} \tag{1.1}$$

and results in $D = 9.8 \cdot 10^{-5}\,\mathrm{m^2\,s^{-1}}$ ($0.98\,\mathrm{cm^2\,s^{-1}}$).

Using the model of a one dimensional heat diffusion into a homogeneous material [7]

$$\frac{\partial T}{\partial t} = D\frac{\partial^2 T}{\partial x^2} - \frac{T - T_\mathrm{a}}{\tau} \tag{1.2}$$

leads for steady state condition $\left(\frac{\partial T}{\partial t} = 0\right)$ to

$$D\frac{\partial^2 T}{\partial x^2} = \frac{T - T_\mathrm{a}}{\tau}. \tag{1.3}$$

With the thermal boundary condition of the temperature T_{x0} at $x = 0$ and the ambient temperature T_a the solution is

$$T(x) = T_\mathrm{a} + (T_{\mathrm{x0}} - T_\mathrm{a})\mathrm{e}^{-x/L} \tag{1.4}$$

with the spatial decay constant (thermal diffusion length L) of

$$L = \sqrt{D\tau}. \tag{1.5}$$

[4] An exemplary *SPICE* simulation of the triggering process is shown in Figure 3.14.

At the distance of the diffusion length L the excess temperature drops to 1/e ($\sim 37\%$). A simplified approximation for silicon is

$$L_{\mathrm{Si}} \simeq 0.3\sqrt{t\,[\mathrm{ns}]} \cdot [\mu\mathrm{m}]. \tag{1.6}$$

For example, the thermal diffusion length in silicon at $t = 100\,\mathrm{ns}$ is $L_{\mathrm{Si}} = 3.1\,\mu\mathrm{m}$ – see sketched and measured heat diffusion for silicon in Figure 1.3.

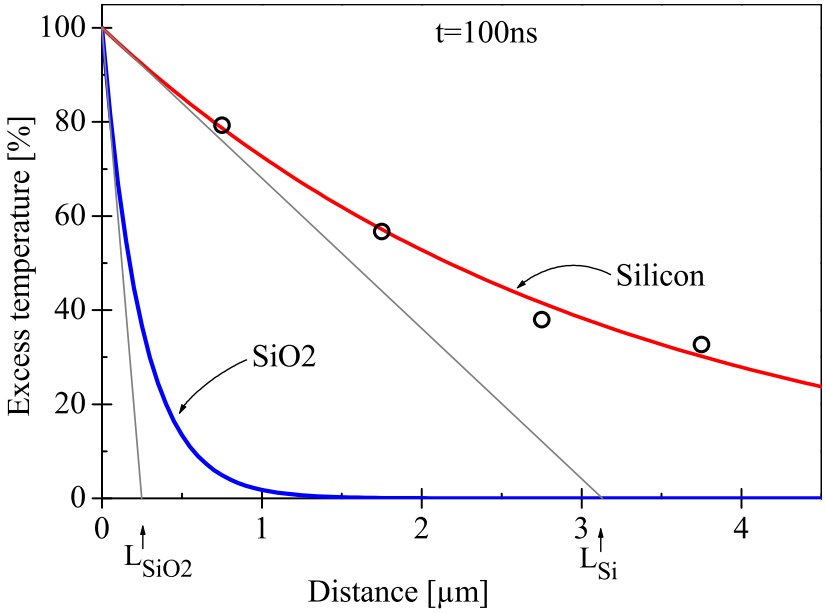


Figure 1.3: Schematic heat diffusion at $t = 100\,\mathrm{ns}$ in silicon (diffusion length $L_{\mathrm{Si}} = 3.1\,\mu\mathrm{m}$) and silicon dioxide (diffusion length $L_{\mathrm{SiO2}} = 0.25\,\mu\mathrm{m}$). Symbols represent measured phase shift data of silicon (see 0.1 A curve in Figure 2.12).

1.3.2 Silicon-on-insulator technology

In silicon-on-insulator technology the doped wells for the transistors are laterally isolated by trenches (*trench isolation*) and vertically isolated by a silicon dioxide (SiO_2) layer (see Figure 1.4). Thus no junction isolation is required and latch-up problems due to parasitic SCR structures and substrate currents are avoided [8]. The isolation from the bulk silicon reduces the parasitic capacitances and the layout can be realized denser than in bulk silicon technology.

The silicon dioxide layer (buried oxide, BOX) is either created with an oxygen ion beam implantation process and annealing or with wafer bonding.

Some important (temperature dependent) properties of silicon dioxide around 300 K [5, 6]

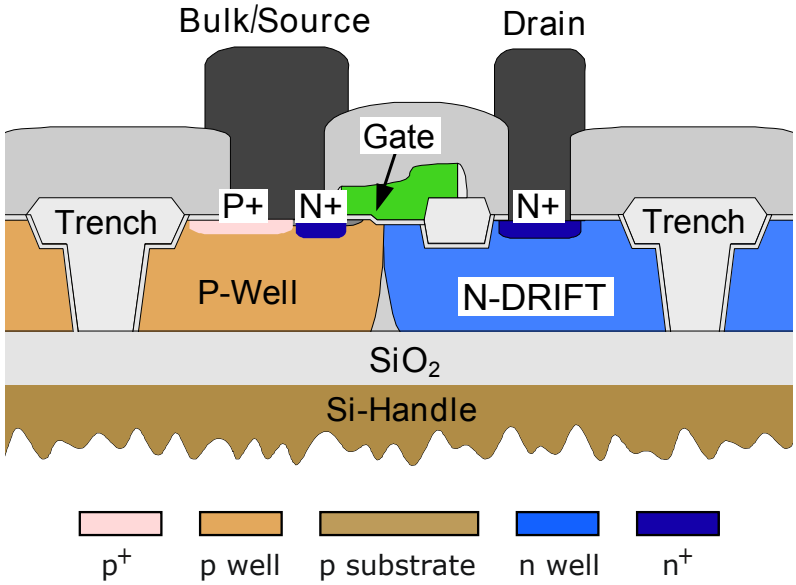


Figure 1.4: Cross section of one finger of a lateral SOI DMOS transistor. The active silicon layer is typically in the range of 2 µm and the SiO_2 layer is typically ~ 1 µm.

are the thermal conductivity $\kappa = 1.4\,\mathrm{W\,m^{-1}\,K^{-1}}$, the mass density $\rho = 2270\,\mathrm{kg\,m^{-3}}$ and the specific heat $C = 1000\,\mathrm{J\,kg^{-1}\,K^{-1}}$. The thermal conductivity of silicon dioxide is ~112 times lower than of silicon. The thermal diffusivity yields with Equation (1.1) to $D = 6.2 \cdot 10^{-7}\,\mathrm{m^2\,s^{-1}}$, this is even ~160 times lower than for silicon.

A simplified approximation of Equation (1.5) for the thermal diffusion length of silicon dioxide is

$$L_{\mathrm{SiO2}} \simeq 0.025\sqrt{t\,[\mathrm{ns}]} \cdot [\mu\mathrm{m}]. \tag{1.7}$$

For example, the thermal diffusion length in silicon dioxide at $t = 100\,\mathrm{ns}$ is $L_{\mathrm{SiO2}} = 0.25\,\mu\mathrm{m}$, which is twelve times lower than for silicon – see sketched heat diffusion for silicon dioxide in Figure 1.3.

In respect to bulk silicon technology, the heat transport through the buried oxide to the substrate (handle wafer) is very low due to the low thermal conductivity of silicon dioxide. As example for a buried oxide layer thickness of 1 µm nearly no heat will diffuse to the handle wafer at $t = 100\,\mathrm{ns}$ (see SiO_2 curve at 1 µm in Figure 1.3). Cooling will occur through the top side of the chip (vias and metal layers). Because of this enhanced self-heating effect, special focus should be taken to thermal optimization of SOI power devices [9–11].

1.4 Electrostatic discharge

Electrostatic charge can be generated by simple charge separation. The capacity C decreases with increasing distance l of the separated charge Q (i.e. the capacity of a plate-type capacitor with area A and permittivity ϵ is $C = \epsilon\frac{A}{l}$). Consequently, increasing distance leads to increasing electrostatic voltage

$$V = \frac{Q}{C}\,. \tag{1.8}$$

Some electrostatic voltages under several cases of charge separation are listed in Table 1.1 [12]. Besides the dissimilarity of the involved materials, the level of the electrostatic voltage depends very much on the relative humidity (%RH) of the surrounding atmosphere – the dryer the air the higher is the electrostatic voltage.

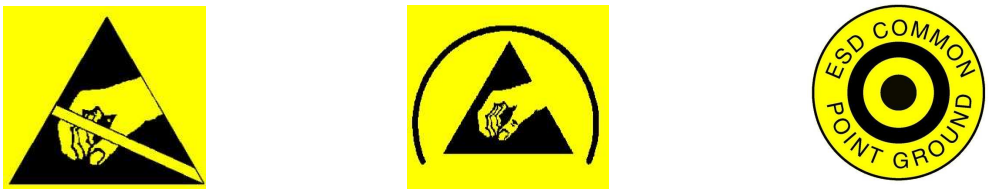
Origin of electrostatic voltage	Static voltage at 20 %RH	Static voltage at 80 %RH
Walking on synthetic carpet	35 kV	1.5 kV
Picking up polyethylene bag	20 kV	0.6 kV
Sliding styrene box on carpet	18 kV	1.5 kV
Arising from foam cushion	18 kV	1.5 kV
Shrinkable film on printed circuit board	16 kV	3.0 kV
Aerosol circuit freeze spray	15 kV	5.0 kV
Walking on vinyl floor	12 kV	0.3 kV
Triggering vacuum solder remover	8 kV	1.0 kV

Table 1.1: Electrostatic voltages depending on relative humidity of surrounding atmosphere [12].

In assembly lines, as well as during manipulation by hand, often insulated tools handle electronic components and thus inherent electrostatic charge cannot be drained. As well operators or handling tools can be electrostatically charged.

The discharge of electrostatically generated charge (electrostatic discharge, ESD) is a serious danger for microelectronic devices. For this reason ESD sensitive devices are commonly labeled with a triangle, a reaching hand and a slash through the reaching hand[5] (Figure 1.5a), which means *caution, don't touch*. ESD protective materials – such as wrist straps, mats etc. – are indicated with an arc around a reaching hand in a triangle

[5] ANSI ESD S8.1-1993 – ESD awareness symbols.



(a) (b) (c)

Figure 1.5: Standardized ESD awareness symbols. (a) ESD susceptibility symbol. (b) ESD protective symbol. (c) ESD common point ground symbol.

(Figure 1.5b). The common point ground for ESD protective materials is identified with a yellow disk (Figure 1.5c) labeled with *ESD common point ground*.

1.4.1 ESD models

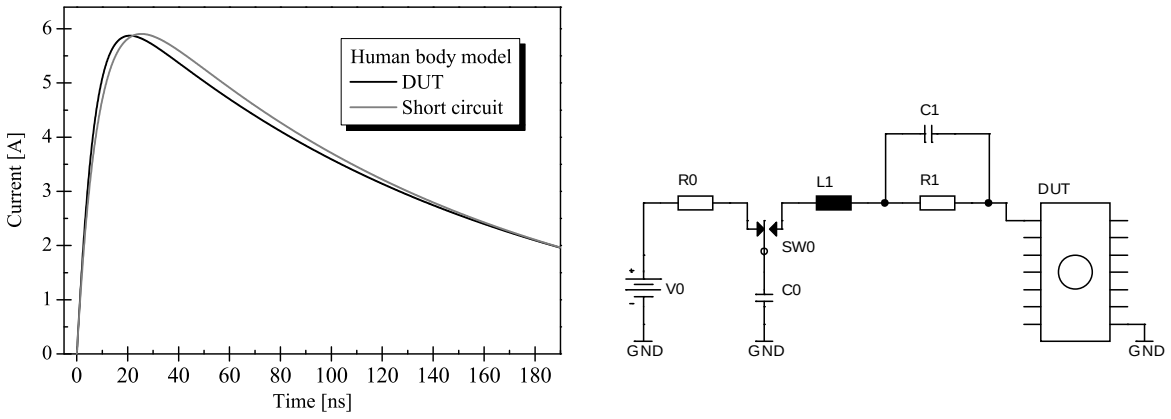
The processes of electrostatic discharge are very complex and stochastically distributed [13]. For industrial tests schematic models are defined to make repeatable electrostatic discharges possible. The most important ESD models distinguish the origin of discharge by men (human body model), by machines (machine model) and by the devices themselves (charged device model) [12]. The first two ESD models show similar failure mechanisms due to internal energy dissipation (melting of junctions). The failure mechanisms of the third model are mainly breakdowns of gate oxide in field effect transistors due to internal voltage distributions. Further models are developed to describe i.e. cable discharge events [14] or system-level ESD stress [15].

Human body model

The human body model (HBM) describes the discharge of a standing electrostatically charged man through a pointing finger into a grounded component. A typical discharge waveform with a rise-time[6] of 10 ns is shown in Figure 1.6a for a $50\,\Omega \parallel 10\,\mathrm{pF}$ device under test (DUT) and a short circuit.

The discharge process is modeled with a 100 pF capacitor (C_0), the approximated capacity of a standing man, which is charged by a 10 kV high voltage source (V_0) and a 10 MΩ series resistor (R_0) and discharged over a 12 µH inductor (L_1) and a 1.5 kΩ series resistor (R_1) with a parasitic stray capacity of 1 pF (C_1) into the DUT. The equivalent circuit

[6] 10% to 90% of peak level.



(a) (b)

Figure 1.6: Human body model. (a) Waveforms for 10 kV pulses. (b) Schematic diagram [16].

diagram is shown in Figure 1.6b. A simulation with *SPICE* [17] gives a pulse duration[7] of 126 ns for a DUT with 50 Ω and 10 pF impedance.

Machine model

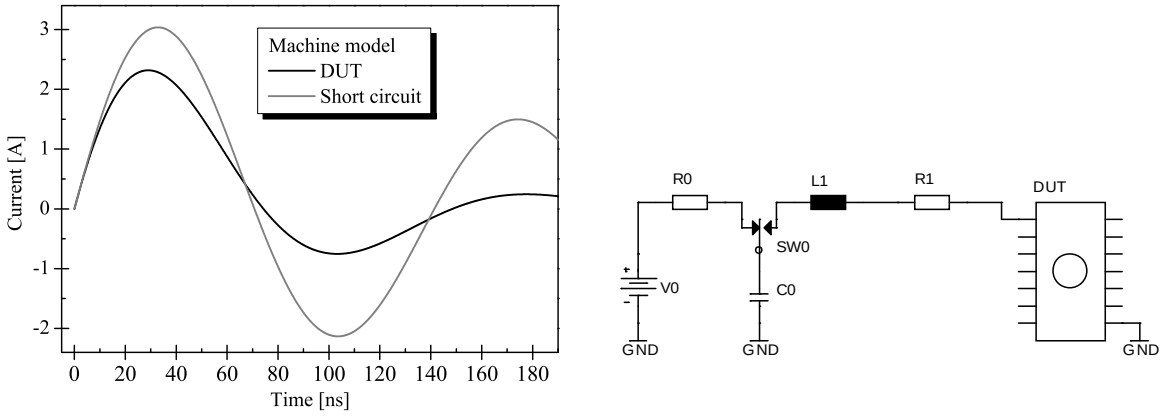
The machine model describes the discharge of a charged handling tool into a grounded component. A typical current through the DUT with a rise time of 18 ns and an oscillating rate of 6.7 MHz is shown in Figure 1.7a. The values of the series resistor and the inductor are much lower than in the human body model. The machine model circuit can be described with a 200 pF capacitor (C_0) discharging by a 2.5 µH inductor (L_1) and a 25 Ω series resistor (R_1) followed by the DUT (Figure 1.7b).

Charged device model

Devices can be charged during picking them from plastic packages or by sliding over insulators. The charged device model describes the discharge of a device by machines, mostly pick-and-place machines, to ground. Due to the very low inductance the current waveforms show a rise time below 1 ns (Figure 1.8a).

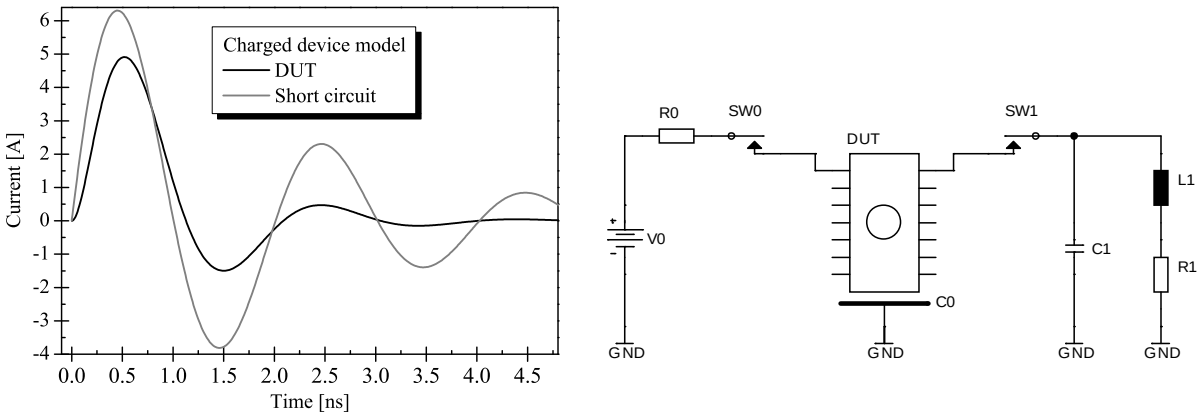
The simplified equivalent circuit diagram in Figure 1.8b is based on a 5 pF capacitor (C_0) discharging the DUT into a current probe, which consists of a 10 nH inductor (L_1) and a 10 Ω series resistor (R_1) with a stray capacity of 5 pF (C_1).

[7] 50% of peak level.



(a) (b)

Figure 1.7: Machine model. (a) Waveforms for 400 V pulses. (b) Schematic diagram [16].



(a) (b)

Figure 1.8: Charged device model. (a) Waveforms for 500 V pulses. (b) Schematic diagram [16].

1.4.2 ESD protection levels

Possible ESD stress increases from production of integrated circuits over ESD protected assembly of systems in factories to unknown handling of the final consumers. This is described with different ESD protection levels and ESD test methods. A good introduction to ESD protection in analog circuits with case studies of various scenarios is shown in [15].

ESD protection at chip level

Electrostatic discharge can occur at packaged integrated circuits only at the pins, because the package is well isolating. The pins of the lead frame are usually connected with bond wires to the (bond) pads on the semiconductor die[8]. ESD protection on chip level focuses on limiting the voltages at the I/O pads and on providing a discharge path over the ground circuitry of the integrated circuit [18]. An ESD protection unit has to absorb this discharge pulse and protect the rest of the integrated circuit from high voltages [19]. Protection elements limit the voltage reaching the core of the chip. High voltages at pads might cause permanent damage due to breakdown of isolations or gate dielectrics. High discharge currents might melt metal traces, vias or even silicon. The ESD protection circuits need to clamp transient voltages during ESD events to safe levels and to sustain the occurring currents. Their response must be fast enough and they should not influence normal operation of the integrated circuit – e.g. they should have very low parasitic capacitances.

The operating range of the protection element has to be designed in a way, that the trigger voltage (V_{TR}) is below the oxide breakdown voltage and the holding voltage (V_H) is higher than the supply voltage range plus a 10 % safety margin to avoid clamping the voltage below the applied supply voltage – which would result in latch-up and the damage of the chip (Figure 1.9) [20]. After activation – in the so called conductive mode – the differential resistance (r_{on}) of the protection device should be very low to keep the power dissipation and the heating of the protection device in an acceptable range. Therefore, many ESD protection devices show s-shaped characteristics.

Local ESD protection at every I/O pad. Every I/O pad is protected with a dedicated ESD protection unit, which drains the discharge current to ground. Figure 1.10 shows on the left the I/O pad, the ESD protection stage, an output driver and the input

[8] In flip-chip technology balls connect the pads to the contacts of the package.

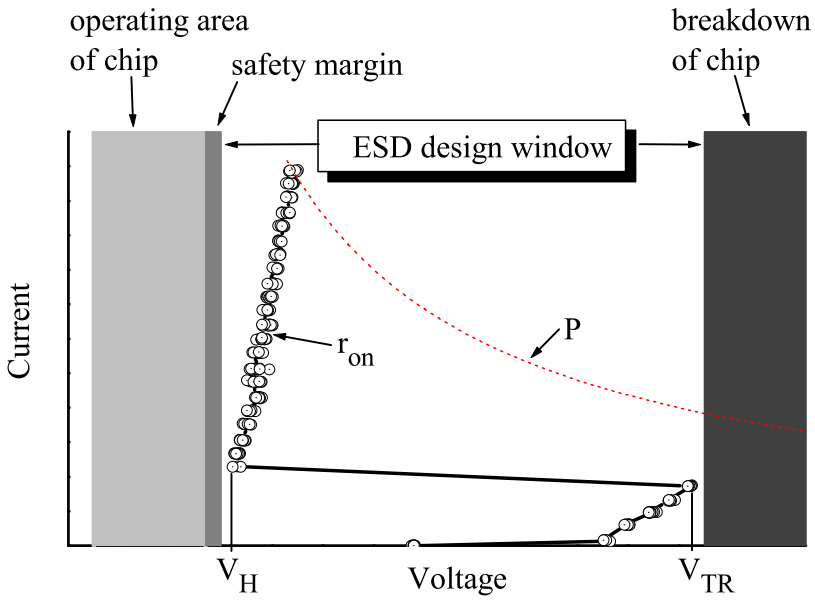


Figure 1.9: ESD design window with lower limit above the operating voltage of the chip plus a safety margin and upper limit below breakdown (destruction) of the chip. The dashed line P denotes a line of constant power.

stage which is connected to the core logic of the chip. If the output driver is activated by the pull-up or pull-down signal, the I/O pad acts as an output and the pad is forced either to VDD or to ground. The input stage converts a signal from the pad to an inverted binary (high/low) signal for the logic circuitry.

An exemplary discharge event is sketched with the dashed line in Figure 1.10, where a positive discharge pulse is applied at I/O-pad1 and ground is applied to I/O-pad2. The ESD pulse activates the ESD protection element PE1, which drains the ESD pulse to the ground network. From the ground network the current flows across the forward biased ESD protection element PE2 to the grounded I/O-pad2.

Every I/O pad can be individually protected according to the allowed voltages and parasitic capacitances. A disadvantage of this concept is, that chips with many pins cover a lot of space with ESD protection units. The protection units need to be robust (i.e. large) enough to absorb the energy of the ESD pulse without any degradation. The simplest ESD protection element is a Zener diode [21], which is operated in breakdown. NMOS transistors allow more flexibility in design. Active clamps use a gate coupling circuit to open the channel of a MOS transistor during the ESD event, which will drain the major discharge current. Grounded gate NMOS transistors use the parasitic bipolar transistor for snap-back operation [22]. Silicon-controlled rectifiers combine high trigger

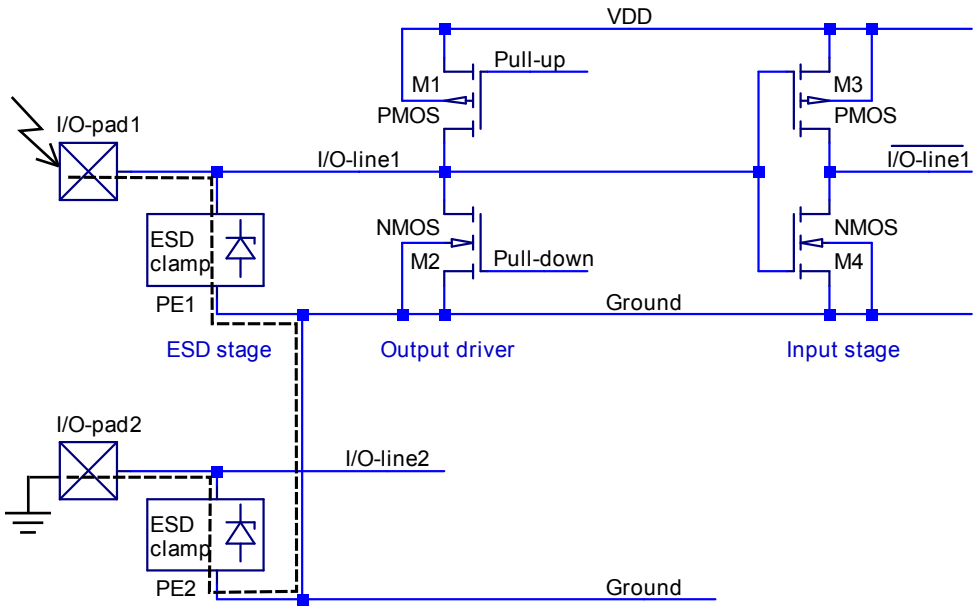


Figure 1.10: Schematic I/O cell with I/O-pad1, ESD protection element PE1, output transistors (M1 and M2) and input stage (transistors M3 and M4). I/O-pad2 and ESD protection element PE2 are related to the neighboring I/O cell.

voltages with very low clamp voltages around 2 V. After qualification the developed ESD protection units are merged in ESD-libraries, which are provided to chip designers.

ESD protection rails. In integrated circuits with many I/O pins, chip area can be saved by using only small diodes (D1–D4) at every single I/O pad, which connect the ESD stress to ESD rails as sketched in Figure 1.11 [15, 23]. ESDM denotes the negative (minus) rail and ESDP the positive (plus) rail. These diodes are operated in forward direction. That results in low power dissipation during ESD events. The voltage on the rails is limited with a few big ESD protection clamps, which are usually distributed along the ESD protection rails in the chip and not at every single I/O pad. An ESD pad ring with several ESD clamps is placed around the core circuitry of the chip.

The dashed line in Figure 1.11 indicates an exemplary discharge from I/O-pad1 over diode D1 to the ESDP rail. The ESD clamp in the rail limits the voltage and drains the current to the ESDM rail. From the ESDM rail the current flows across the forward biased diode D4 to the grounded I/O-pad2. Most of the energy of the ESD event is absorbed in the ESD protection clamp and only a part in the forward biased diodes D1 and D4. The voltage drop in the rails must be kept low during the ESD events.

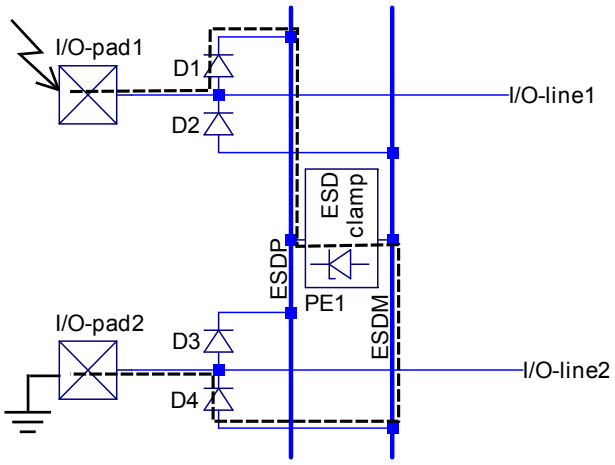


Figure 1.11: Simplified ESD protection network with common positive rail ESDP and common negative (minus) rail ESDM. Several I/O pads are connected with (small) diodes to a common (large) ESD clamp (after [15]).

Self protection of output drivers. Some output drivers are designed for ESD self-protection without special ESD protection elements. Previous investigations on VDMOS output drivers [16, 24–26] showed the activity of parasitic bipolar transistors, which limit effectively the voltage at the output pad.

System level ESD protection

A careful design of systems consisting of PCBs, integrated circuits, discrete components, I/O-connectors etc. is necessary to achieve high ESD robustness of the total system. A lot of effort is made to withstand with on-chip ESD protection the system level ESD stress [27]. At system level sensitive connector pins often need to be protected by additional discrete ESD protection components, which are soldered to the PCB (e.g. transient voltage suppressors (TVS) or filters) [28]. These discrete protection components need to respond fast enough and their trigger voltage must be smaller than the trigger voltage of the protection elements of the ICs – otherwise the energy of the ESD pulse is dissipated in the integrated circuit rather than in the discrete protection elements.

System level ESD tests are usually done with an “ESD-gun” [29], which generates pulses with a two-peak waveform (IEC ESD pulse [30]). A sharp high peak is followed by a slower HBM-like peak [31]. For preliminary tests at wafer-level the effect of application PCBs can be modeled with a human metal model (HMM) networks [15]. During plug-in of cables interface pins are often exposed to discharge of cables. This type of ESD stress is described with the so called cable discharge event (CDE) [14].

ESD protection at production

The production and assembly of electronic systems are usually done in a well known ESD protected area (EPA) [15]. Excessive ESD stress is avoided by the use of conductive mats, wrists, ESD-boxes and controlled humidity. Typical ESD stress of human handling is modeled and tested with the human body model. The machine model is relevant for e.g. pick-and-place machines and the effect of slides for components in feeding systems are described with the charged device model.

ESD protection at the consumer

At the consumer the well controlled ESD protected area is left and electronic systems are exposed to unknown handling in an unknown environment. Consequently, implicit ESD protection is essential. Special attention has to be paid to the (few) exposed interface pins because charge equalization between two objects (e.g. plugs) occurs through the first connected contact – this should be the shield or ground. Therefore, longer pins for shield or ground are desired. Demonstrative examples are the widely used universal serial bus (USB) plugs. The first contact is usually the connection to the shield (see Figure 1.12a). Some memory modules omit the shield – then the longer ground and power pins are contacting first – see Figure 1.12b.

(a) (b)

Figure 1.12: USB plug (a) with shield contacting first and (b) longer power and ground pins.

ESD induced latch-up can be avoided by powering off before plugging. Controlled – and especially in winter increased – humidity reduces significantly the electrostatic voltages – see Table 1.1.

1.5 Latch-up in bulk CMOS circuits

An uncontrollable current flow in the power supply of an integrated circuit is called latch-up. Generally, latch-up leads to destruction of the circuit – unless the current is sufficiently limited by external devices. Latch-up occurs, if a conductive path in the power supply of a circuit (e.g. parasitic SCR structure or parasitic bipolar transistor) is activated. Triggering could be due to injection of positive or negative currents. If the holding voltage is below the supply voltage (see operating area in Figure 1.9), current flow occurs even after the end of the trigger pulse.

Latch-up is a continuing risk for bulk silicon CMOS integrated circuits[9] because unavoidable parasitic SCR structures are always present and consequently a potential risk for latch-up [4, 32–36]. Under certain circumstances they can be activated and lead to latch-up [34, 37, 38]. The triggering mechanisms are often substrate currents originating from overshoots due to impedance mismatch, coil discharge, electrostatic discharge or electrical over-stress events. The sensitivity of integrated circuits to electrical disturbances in operation is worse with scaling down due to the smaller feature size and the lowering of operating voltage. Therefore, nowadays a lot of effort is done to reduce substrate currents [23, 39–42] and to prevent latch-up [2, 4].

1.5.1 Latch-up types

Internal latch-up

Latch-up, which is triggered by injection of current directly to the terminals of the SCR is called *internal* latch-up (see left part and dashed arrows in Figure 1.13) [43]. Overshoots during gate switching of MOS transistors [44] could also lead to short injection currents.

External latch-up

In an *external* latch-up event, triggering of a parasitic SCR structure is caused by carriers injected from distant diffusions (substrate currents), which are connected to I/O pads (see solid arrows in Figure 1.13) [43]. These diffusions could be related to ESD protection elements or output drivers. Carriers reaching the bases of the parasitic SCR structure might activate it and cause latch-up.

[9] We have seen already four latch-up damaged notebooks and PCs during the last years – a result of the faster I/O ports with lower allowed parasitic capacitances.

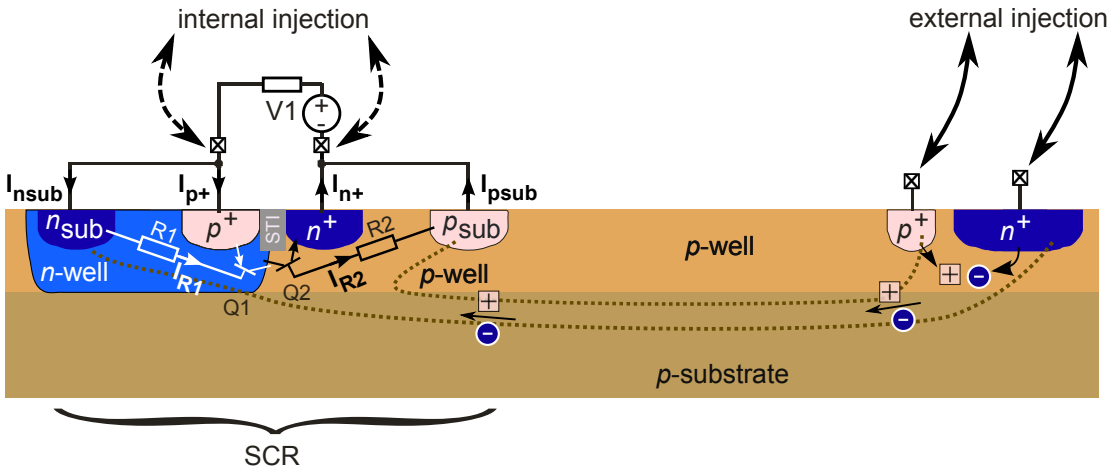


Figure 1.13: Schematic cross section showing on the left an SCR together with internal current injection at the p^+ and n^+ diffusions of the SCR (dashed arrows) and on the right external current injection (solid arrows). Carriers reaching the bases of the SCR might activate it and cause latch-up. In p substrate, minority carriers (electrons, ⊖) are shielded by majority carriers (holes, ⊞) [1].

Static latch-up

Triggering latch-up with constant current (or very low slew rates) is called *static* latch-up. A common test method is injecting constant current with positive and negative polarity into each pin of the device under test (JEDEC JESD78A specifies a trigger current higher than $I_{\mathrm{nom}} + 100\,\mathrm{mA}$).

Transient latch-up

Triggering latch-up with fast transients is called *transient* latch-up (TLU). Such pulses can be caused for instance by ESD events or rapid discharges of coils [4, 45–47]. Displacement currents could assist triggering of latch-up, consequently transient latch-up is very important for circuits with short rise times and high slew rates (e.g. digital circuits with $\mathrm{d}V/\mathrm{d}t > 1\,\mathrm{V/ns}$).

1.5.2 Latch-up protection in CMOS technology

Several approaches to prevent activation of parasitic SCR structures are proven. The measures comprise layout as well as materials (e.g. doping concentration), but the latch-up problem is not completely vanished in modern bulk CMOS devices. As a last resort the design could be processed in (the more expensive) silicon-on-insulator technology.

Distances

Latch-up robustness could be improved by increasing distances inside the parasitic SCR structure (e.g. bases) and by increasing the distance between injection source and parasitic SCR structure (see Figure 1.13).

Well resistances

The decrease of well and substrate resistances lead to higher latch-up immunity. This could be achieved by increasing the contact density in the wells or increasing the doping concentration in the wells. Lower well (base) resistance of the parasitic bipolar transistors results in lower voltage drop.

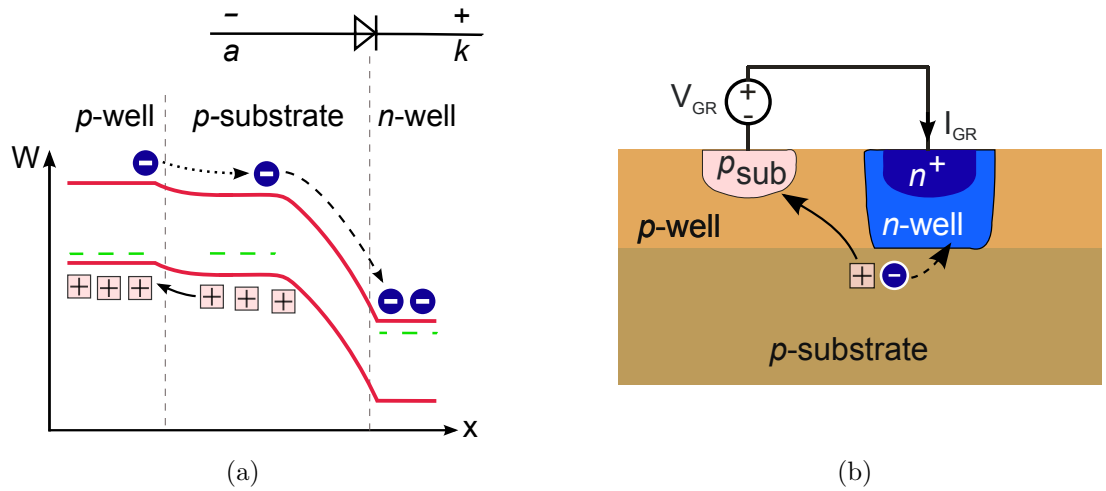
Guard-rings

Guard-rings for collection of excess carriers are widely used in CMOS and Smart Power technologies. Such guard-rings can be floating [39], (locally) grounded [40, 41] or biased [15]. Excess holes are collected by p guard-rings and excess electrons by n guard-rings. The principle of the collection of excess electrons with biased n guard-rings (GRs) for latch-up protection is shown in Figure 1.14. Excess electrons[10] ($\ominus$, minority carriers in p substrate) are collected by positive biased n wells (n guard-rings, see dashed arrow). Excess majority carriers ($\boxplus$, holes), which shielded these minority carriers, are released and collected by the p_{sub} contacts (p guard-rings, see solid arrow) [1]. The p_{sub} contacts are usually at lowest potential (ground). The intensive use of p guard-rings improves the substrate connection to ground and therefore reduces the distributed substrate resistance. Reverse biasing of the p substrate/n well junction cause a minority carrier concentration below the thermal equilibrium (see ellipse in Figure 1.15).

1.6 Electrical testing methods

Basic device characterizations are performed with DC measurements in the low current (low power) regime, where no significant self-heating occurs and no cooling is required. In the high current (high power) regime the devices are characterized with short pulses. Sufficient time for cooling of the sample after each stress pulse is ensured to avoid early

[10] E.g. injected electrons or optically generated electron-hole pairs.



(a) (b)

Figure 1.14: (a) Simplified schematic energy band diagram of the reverse biased p well / p substrate / n well junction showing the collection of carriers. Electrons (⊖) are collected by positive biased n wells (see dashed arrow). Holes (⊞) are collected by grounded p diffusions (see solid arrow). (b) Schematic cross section of a p guard-ring and an n well guard-ring in a p substrate wafer.

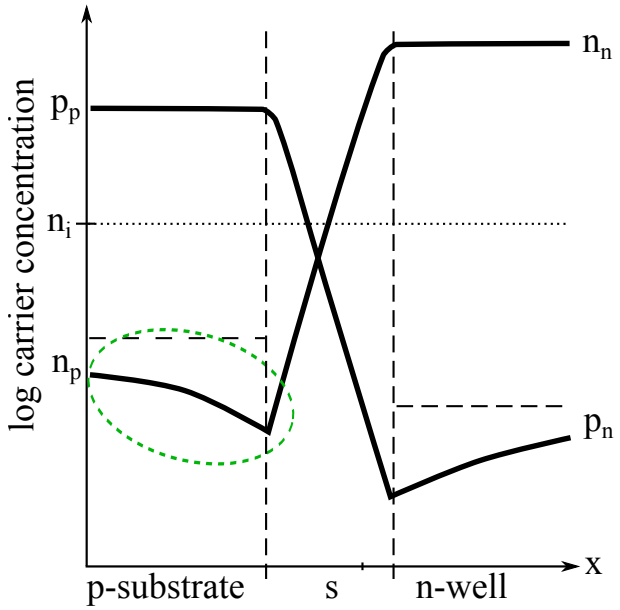


Figure 1.15: Schematic carrier concentration in reverse biased p substrate/n well junction (n guard-ring) showing reduction of minority carrier concentration (see ellipse) in p substrate (after [1]). The space charge region is denoted with "s", the electron (minority carrier) concentration in p substrate is denoted with "n_p" and the hole (majority carrier) concentration in p substrate is denoted with "p_p".

degradations due to excessive self-heating. The DC measurements (e.g. leakage currents) are performed with the *Keithley* source measure units *K2410* [48] and *K237* [49].

Different types of pulse generators are used for measurements of pulsed current-voltage (*I-V*) characteristics and for pulsed excitation during the TIM experiments. The devices are stressed by pulse generators, which provide (nearly) square current pulses. The voltage and current transients of each stress pulse are acquired with an oscilloscope and processed with the *Matlab* [50] program *tlpiv.m* [51] to get the pulsed *I-V* characteristics. The acquired voltage and current waveforms are averaged over a certain time interval. These averaged values $\overline{I}$ and $\overline{V}$ give one point in the pulsed *I-V* characteristics – see arrows in Figure 1.16. For a stress pulse amplitude sweep, the pulse current is increased in small steps, where several pulses can be applied at each stress level to reveal pulse-to-pulse instabilities.

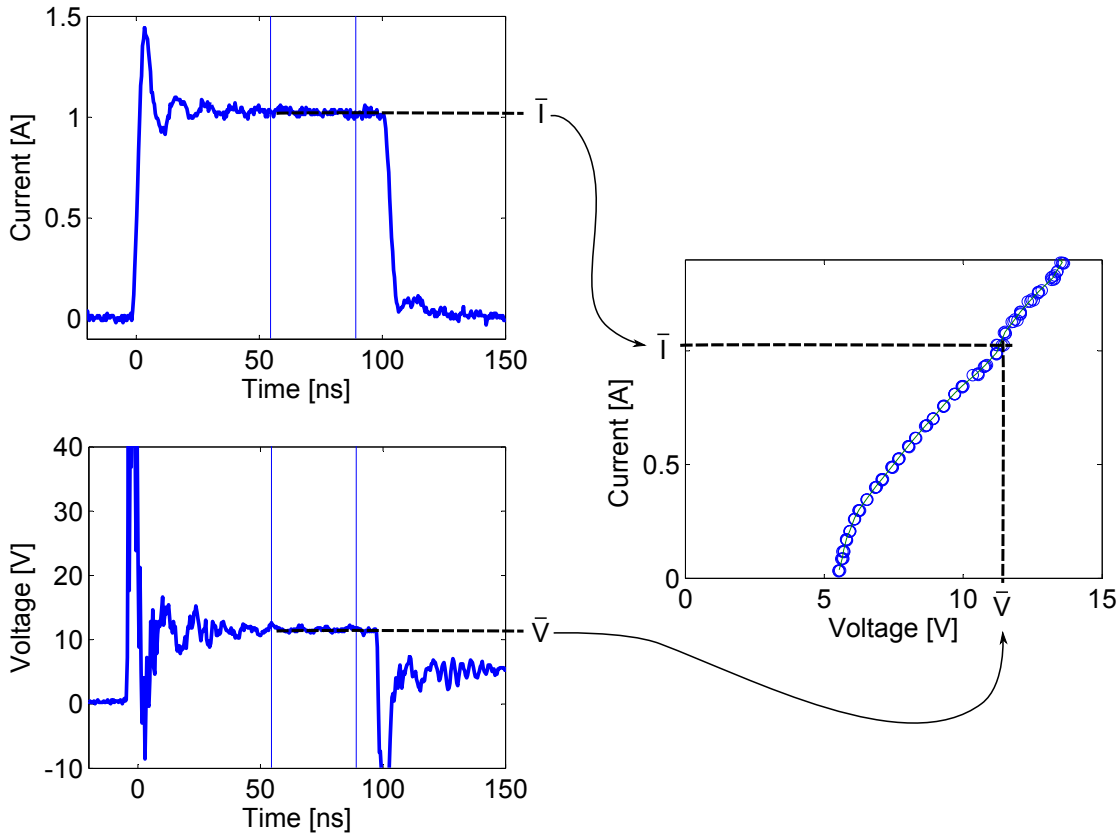


Figure 1.16: Creation of pulsed *I-V* characteristics. The averaged current and voltage values ($\overline{I}$, $\overline{V}$) give one point in the pulsed *I-V* characteristics.

1.6.1 Transmission line pulse generators

A useful approximation for HBM-ESD pulses is the pulse creation with a transmission line pulse generator (TLP), which schematic diagram is shown in Figure 1.17. Here, the generated square pulses are easy to reproduce and can reach rise times below 2 ns. A coaxial cable with 50 Ω characteristic impedance and length l according to the desired pulse duration T_p is used as transmission line, which is charged with the 10 MΩ resistor R_0 using the high voltage source V_0

$$l = \frac{v_\mathrm{p} T_\mathrm{p}}{2}. \tag{1.9}$$

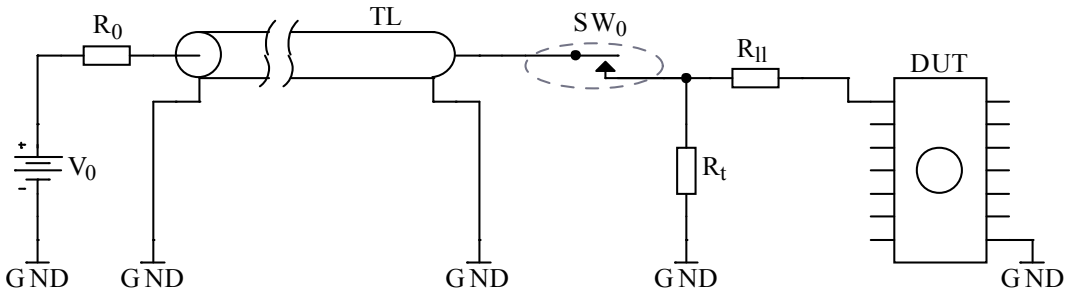


Figure 1.17: Pulse generation with a transmission line pulse generator. The load line resistance is determined with resistor R_ll. Resistor R_t is used for proper termination of the transmission line (TL).

When the reed relay SW_0 is closed, the voltage at switch SW_0 is halved[11], because of the potential divider of the internal impedance of the transmission line and the 50 Ω termination resistor R_t.

The imposed current on the DUT is determined by the load line resistor R_ll and the voltage V_0

$$I = \frac{1}{2}\frac{V_0}{R_\mathrm{ll} + R_\mathrm{DUT}} \simeq \frac{1}{2}\frac{V_0}{R_\mathrm{ll}}\,. \tag{1.10}$$

The current pulse stops, when the – on the open end[12] reflected – voltage wave in the transmission line returns to the switch. This issues the factor 1/2 in (1.9). With the propagation speed $v_\mathrm{p} \simeq 200 \cdot 10^6\,\mathrm{m/s}$ of the wave, the pulse duration is approximately 10 ns per meter transmission line. The disadvantage of a transmission line pulse generator is the fixed pulse duration – for each pulse duration a separate transmission line length is necessary.

[11] R_ll, which is usually much larger than 50 Ω, is neglected.
[12] R_0 with 10 MΩ is negligible.

1.6.2 Solid-state pulse generators

Solid-state pulse generators have the advantage of adjustable pulse duration, but often the drawback of longer rise time compared to TLP-systems. For currents up to 2 A the programmable solid-state pulse generator *HP8114A* from *Agilent* is used [52]. It provides output voltages from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$ into $50\,\Omega$ with a rise time of 7 ns. The baseline option allows biasing of the output in the range of $\pm 30\,\mathrm{V}$.

For higher stress currents the gate of a special solid-state switch is controlled with a digital delay and pulse generator (*DG535* [53]). The SV4000-*p* modulator from *DEI* [54] is used as high voltage switch, which is powered by a *Glassman* high voltage source [55] (Figure 1.18).

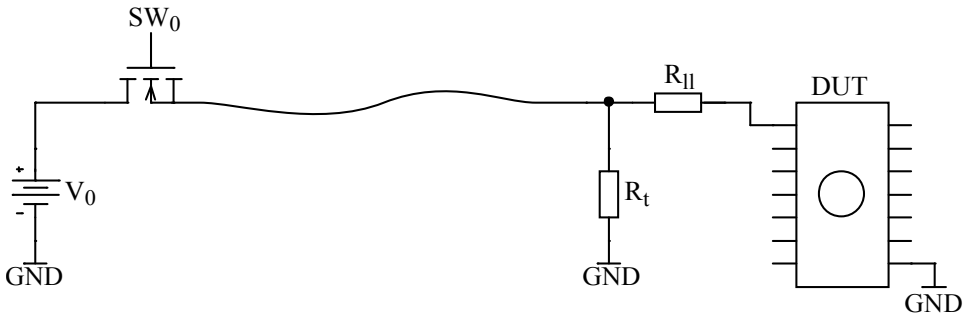


Figure 1.18: Pulse generation with a solid-state switch (SW_0). The load line resistance is determined with resistor R_{ll}. Resistor R_{t} is used for proper termination of the coaxial cable.

This solid-state switch is capable to switch up to 4 kV with minimal 150 ns pulse duration. The current through the DUT, which is limited by the load line resistor R_{ll}, is

$$I = \frac{V_0}{R_{\mathrm{ll}} + R_{\mathrm{DUT}}} \simeq \frac{V_0}{R_{\mathrm{ll}}}\,. \tag{1.11}$$

The termination-resistor R_{t} prevents reflections from the DUT back to the solid-state switch.

1.7 Optical investigation method

The optical investigation method is based on monitoring transient refractive index changes of silicon due to variations of temperature and carrier concentrations. This non-destructive investigation method uses optical interferometers and is called transient interferometric

mapping method (TIM) [56, 57]. This technique is a powerful tool to analyze internal temperature and free carrier distribution in ESD protection devices [58–60] and power devices on bulk silicon [61] or SOI substrates [62]. Triggering homogeneity, current flow instability [63] and current filamentation [26, 64, 65] have been investigated in ESD protection devices and circuits with nanosecond time and micrometer space resolution. Other non-destructive optical investigation methods like free carrier absorption, internal laser deflection, photon emission (EMMI), time resolved photon emission (TRE), seebeck effect imaging (SEI), optical beam induced resistance change (OBIRCH), and pulsed optical beam induced current (P-OBIC) are reviewed by *R. Thalhammer* in [66] and *F. Essely* in [67].

The refractive index n describes the ratio of the speed of light in free space c_0 and in a medium c [68]

$$n = \frac{c_0}{c} = \frac{\sqrt{1/(\mu_0\epsilon_0)}}{\sqrt{1/(\mu_0\mu_r\epsilon_0\epsilon_r)}} = \sqrt{\mu_r\epsilon_r}\,. \tag{1.12}$$

μ_0 and ϵ_0 are the permeability and permittivity of free space, μ_r and ϵ_r are the relative permeability and permittivity of the medium. Refractive index variations influence the speed – and consequently the phase – of optical probing beams.

The absorption coefficient of silicon depending on wavelength and temperature is shown in Figure 1.19a [69]. The diagram shows that silicon gets transparent for infrared (IR) light with a wavelength longer than 1.27 µm. For the optical investigations an infrared laser with a wavelength of 1.31 µm is used. The wavelength λ in a medium is given by Equation (1.13), where f is the frequency of the used laser source.

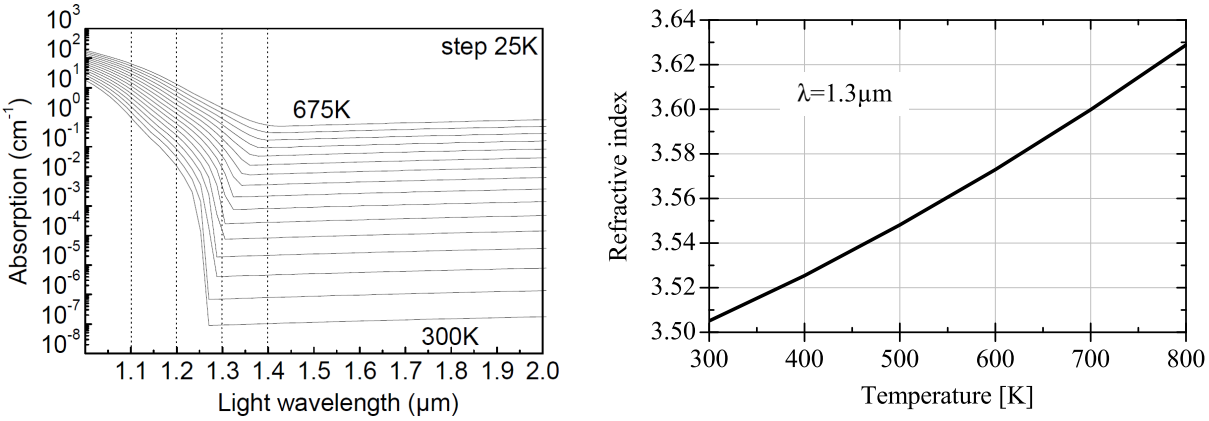
$$\lambda = \frac{c_0}{fn} = \frac{\lambda_0}{n} \tag{1.13}$$

The local temporal change of refractive index of silicon Δn is described as the difference of the stressed (n_{str}) and the initial situation (n_0)

$$\Delta n(\vec{r}, t) = n_{str}(\vec{r}, t) - n_0(\vec{r}, t_0). \tag{1.14}$$

The refractive index of silicon depends on temperature by the thermo-optical effect [70] and on the excess carrier concentration by the plasma optical effect [56, 58, 71]. Thus, the local variation of the refractive index is composed of a thermo-optical component and a plasma-optical (free carrier) component

$$\Delta n = \Delta n_{th} + \Delta n_{fc}. \tag{1.15}$$



(a) (b)

Figure 1.19: (a) Silicon absorption coefficient depending on wavelength and temperature [69]. (b) Refractive index of silicon depending on crystal temperature for a wavelength of $\lambda = 1.3\,\mu\text{m}$.

1.7.1 Contribution of the thermo-optical effect

The refractive index dependency of silicon on crystal temperature is investigated in [70]. Figure 1.19b shows the temperature dependency of the refractive index in silicon[13] for a wavelength of $\lambda = 1.3\,\mu\text{m}$. The change of the refractive index Δn_{th} depends on the temperature dependent $\frac{\mathrm{d}n}{\mathrm{d}T}$ and the temperature change ΔT

$$\Delta n_{\text{th}}(\vec{r}, t) = \frac{\mathrm{d}n}{\mathrm{d}T} \Delta T(\vec{r}, t). \tag{1.16}$$

The temperature change is the difference of the temperature distribution $T(\vec{r}, t)$ at instant t and the initial temperature distribution $T(\vec{r}, t_0)$

$$\Delta T(\vec{r}, t) = T(\vec{r}, t) - T(\vec{r}, t_0). \tag{1.17}$$

The thermo-optic coefficient of silicon is $\frac{\mathrm{d}n}{\mathrm{d}T} = 1.93 \cdot 10^{-4}\,\mathrm{K}^{-1}$ for temperatures around 320 K. In contrast, the thermo-optic coefficient for silicon dioxide is one decade lower ($10^{-5}\,\mathrm{K}^{-1}$).

[13] The refractive index of silicon dioxide at 1.5µm wavelength is around 1.45.

1.7.2 Contribution of the plasma-optical effect

A concentration change[14] of electrons ΔN_n and holes ΔN_p influences the refractive index (Δn_fc) due to the plasma-optical effect as shown in Figure 1.20 [71].

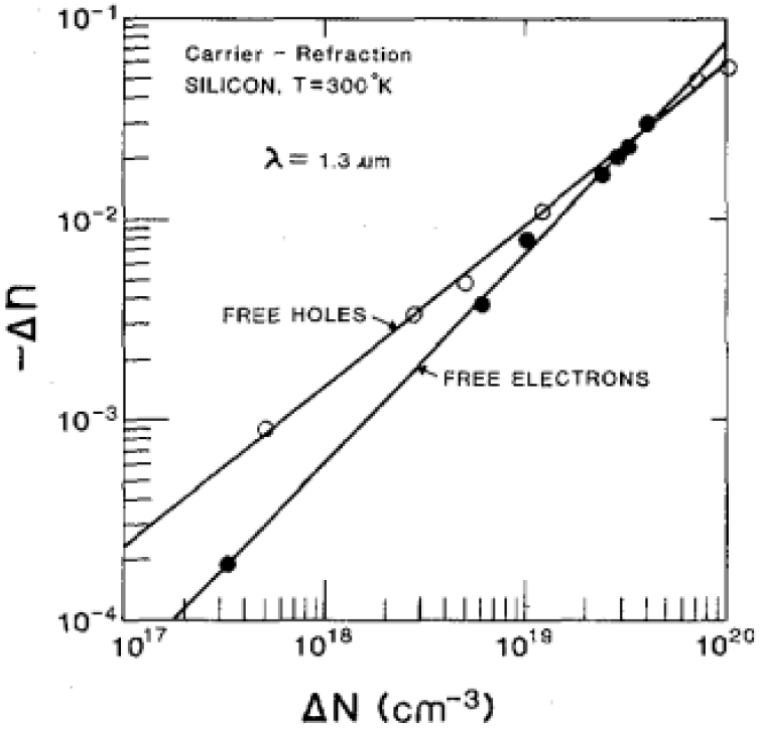


Figure 1.20: Carrier refraction in Silicon for $\lambda = 1.3\,\mu\mathrm{m}$ [71].

The relation of the carrier concentration change to the refractive index change is described with

$$\Delta n_\mathrm{fc}(\vec{r},t) = k_\mathrm{n}\Delta N_\mathrm{n}(\vec{r},t)^\alpha + k_\mathrm{p}\Delta N_\mathrm{p}(\vec{r},t)^\beta. \tag{1.18}$$

The concentration change of electrons is the deviation from the static electron concentration n_e

$$\Delta N_\mathrm{n}(\vec{r},t) = n_\mathrm{e}(\vec{r},t) - n_\mathrm{e}(\vec{r},t_0). \tag{1.19}$$

The concentration change of holes is the deviation from the static hole concentration p_h

$$\Delta N_\mathrm{p}(\vec{r},t) = p_\mathrm{h}(\vec{r},t) - p_\mathrm{h}(\vec{r},t_0). \tag{1.20}$$

For a wavelength of $\lambda = 1.3\,\mu\mathrm{m}$ the approximated parameters are $\alpha = 1.05$, $\beta = 0.805$,

[14] To distinguish the carrier concentration change from the refractive index n, it is denoted with ΔN.

$k_\mathrm{n} = -7.6 \cdot 10^{-23}\,\mathrm{cm}^3$ and $k_\mathrm{p} = -4.9 \cdot 10^{-18}\,\mathrm{cm}^3$. For charge neutrality[15] ($\Delta N_\mathrm{n} = \Delta N_\mathrm{p}$) holes have the dominant effect on the refractive index. Remark that *drift current* does not change the carrier concentration ($\Delta N = 0$) and so $\Delta n_\mathrm{fc} = 0$ (but it could cause heating).

1.7.3 Optical phase shift

The refractive index variations cause an optical phase shift $\Delta\varphi$ of a probing laser beam, which passes the active region of a DUT. The beam is reflected at the metalization layers and passes again the active region (see Figure 1.21). The optical phase shift of the reflected beam can be transformed with interferometers to amplitude variations, which can be measured with photodetectors or cameras.

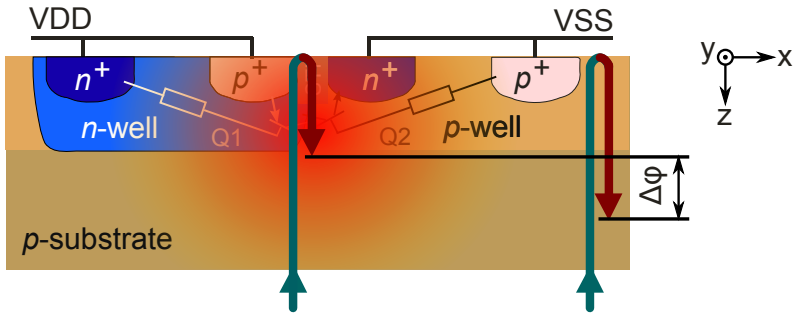


Figure 1.21: Cross section of DUT with incident laser beams and reflected laser beams. At hot silicon (red shaded) the reflected beam is delayed (increased refractive index).

The electric field of the reflected electromagnetic probe beam $\underline{\vec{E}}_\mathrm{p}$ can be described as one-dimensional transversal wave spreading in z direction [68, 72][16]

$$\underline{\vec{E}}_\mathrm{p}(z,t) = E_\mathrm{p0}\,\mathrm{e}^{\mathrm{j}(\omega_\mathrm{p}t - k_\mathrm{p}z + \varphi_0)}\vec{e}_\mathrm{p}. \tag{1.21}$$

$\vec{e}_\mathrm{p}$ is the polarization direction and E_p0 is the amplitude of the reflected probe beam, which might be modulated due to temporal change of light absorption. φ_0 is the zero phase angle, ω_p is the angular frequency of the probe beam and the corresponding wave number is

$$k_\mathrm{p} = 2\pi/\lambda_\mathrm{p}. \tag{1.22}$$

[15] Excess minority carrier concentrations are compensated (shielded) by majority carriers (quasi-neutrality) [1].
[16] Some publications and books denote the instantaneous phase inverted $\Phi = kz - \omega t + \varphi$ [73].

The real part can be written in the form

$$E_{\mathrm{p}}(z,t) = \Re\big(E_{\mathrm{p0}}\,\mathrm{e}^{\mathrm{j}(\omega_{\mathrm{p}}t - k_{\mathrm{p}}z + \varphi_0)}\big) = E_{\mathrm{p0}}\cos(\omega_{\mathrm{p}}t - k_{\mathrm{p}}z + \varphi_0). \tag{1.23}$$

For calculation of the total optical phase shift of the probe beam (φ_{p}) with inhomogeneous refractive index distribution the product $k_{\mathrm{p}}z$ is replaced by an integral along the beam path $k_{\mathrm{p}}z \to \int k_{\mathrm{p}}(z)\,\mathrm{d}z$. This gives with (1.22) $\int \frac{2\pi}{\lambda_{\mathrm{p}}(z)}\,\mathrm{d}z$ and with (1.13) $\int \frac{2\pi}{\lambda_0} n(z,t)\,\mathrm{d}z$.

Using the change of the refractive index (1.14) and the zero phase angle results in

$$\varphi_{\mathrm{p}}(t) = \int \frac{2\pi}{\lambda_0}\Delta n(z,t)\;\mathrm{d}z + \int \frac{2\pi}{\lambda_0} n_0(z,t_0)\;\mathrm{d}z - \varphi_0. \tag{1.24}$$

In this notation a longer optical path (increasing refractive index) causes a positive phase of the probe beam (φ_{p}). Equation (1.24) expresses the influence of the refractive index changes (Δn), the initial refractive index (n_0) and the zero phase angle (φ_0) to the optical phase of the probe beam. To simplify further notations the initial refractive index and the zero phase angle are combined to $\varphi_{\mathrm{p}}(t_0)$

$$\varphi_{\mathrm{p}}(t) = \Delta\varphi_{\mathrm{p}}(t) + \varphi_{\mathrm{p}}(t_0). \tag{1.25}$$

This gives with Equation (1.21) for the probe beam at the photodetector

$$\underline{E}_{\mathrm{p}}(z,t) = E_{\mathrm{p0}}\,\mathrm{e}^{\mathrm{j}\left(\omega_{\mathrm{p}}t - \varphi_{\mathrm{p}}(t)\right)} = E_{\mathrm{p0}}\,\mathrm{e}^{\mathrm{j}\left(\omega_{\mathrm{p}}t - \Delta\varphi_{\mathrm{p}}(t) - \varphi_{\mathrm{p}}(t_0)\right)}. \tag{1.26}$$

The real part can be written in the form

$$E_{\mathrm{p}}(t) = E_{\mathrm{p0}}\cos\left(\omega_{\mathrm{p}}t - \Delta\varphi_{\mathrm{p}}(t) - \varphi_{\mathrm{p}}(t_0)\right). \tag{1.27}$$

The reflected probe beam passes again the silicon substrate with thickness l – consequently the phase shift is doubled

$$\Delta\varphi_{\mathrm{p}}(t) = 2\int_0^l \frac{2\pi}{\lambda_0}\Delta n(z,t)\;\mathrm{d}z. \tag{1.28}$$

A combination of (1.16) and (1.18) in (1.28) results in the total optical phase shift

$$\Delta\varphi(t) = \frac{4\pi}{\lambda_0} \int_0^l \left(\frac{\mathrm{d}n}{\mathrm{d}T} \Delta T(z,t) + k_\mathrm{n} \Delta N_\mathrm{n}(z,t)^\alpha + k_\mathrm{p} \Delta N_\mathrm{p}(z,t)^\beta \right) \mathrm{d}z. \tag{1.29}$$

The phase shift $\Delta\varphi$ in Equation (1.29) has a positive temperature related component $\Delta\varphi_\mathrm{th}$ and a negative free-carrier related (plasma-optical) component $\Delta\varphi_\mathrm{fc}$

$$\Delta\varphi = \Delta\varphi_\mathrm{th} + \Delta\varphi_\mathrm{fc}. \tag{1.30}$$

The phase shift due to the change of free carriers (plasma component) is calculated from Equation (1.29) for a homogeneous distribution along the z axis and charge neutrality ($\Delta N_\mathrm{n} = \Delta N_\mathrm{p}$). The phase shift curves are shown in Figure 1.22 up to the resolution limit of the later presented scanning TIM setup of ∼5 mrad.

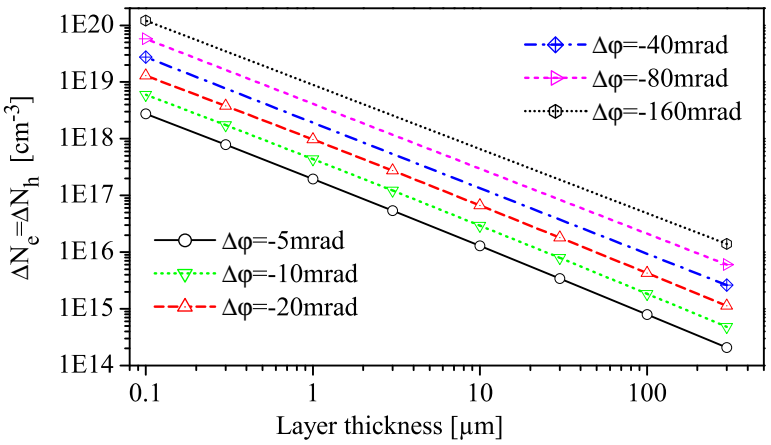


Figure 1.22: Phase shift of a homogeneous excess carrier concentration vs. layer thickness.

At high dissipated power the thermal contribution dominates the phase shift and the plasma-optical contribution can be neglected

$$\Delta\varphi'(t) = \frac{4\pi}{\lambda_0} \int \frac{\mathrm{d}n}{\mathrm{d}T} \Delta T(z,t)\, \mathrm{d}z. \tag{1.31}$$

In this case the phase shift in Equation (1.31) can be interpreted in a first approximation proportional to the stored energy in substrate[17]. The lateral two-dimensional (2D) energy

[17] Neglecting heat transfer through the surface, neglecting non-linearities etc.

distribution W_{2D} is

$$W_{2D}(x,y,t) = \int W(x,y,z,t)\,\mathrm{d}z = c_\mathrm{v} \int \Delta T(x,y,z,t)\,\mathrm{d}z. \tag{1.32}$$

The volume specific heat c_v for silicon is $1.63 \cdot 10^6\,\mathrm{JK^{-1}m^{-3}}$. Substitution of the integral of Equation (1.32) with a conversion of Equation (1.31) results in the two-dimensional energy distribution [58, 59]

$$W_{2D}(x,y,t) = \frac{\lambda_0 c_\mathrm{v}}{4\pi \frac{\mathrm{d}n}{\mathrm{d}T}} \Delta\varphi(x,y,t). \tag{1.33}$$

For moderate temperature variations and the shown (temperature dependent) coefficients a rough approximation of the two-dimensional energy distribution is

$$W_{2D}(x,y,t) \simeq 0.88 \Delta\varphi(x,y,t)\ [\mathrm{nJ/\mu m^2}]. \tag{1.34}$$

This approximation can be used for a rough estimation of the expected phase shift in a homogeneous area using the dissipated power $(V \cdot I)$, time (t) and size $(l \cdot w)$

$$\Delta\varphi(x,y,t) \simeq a \frac{V \cdot I \cdot t}{l \cdot w}. \tag{1.35}$$

The coefficient $a = 1.127 \cdot 10^{-3}\,\mathrm{m^2\,J^{-1}}$ is empirically decreased to consider slight heat diffusion to metal layers and to lateral side of real integrated circuits.

For short pulses and small temperature changes (adiabatic condition) the temperature profile for heat diffusion into silicon substrate with diffusion length L can be calculated with Equation (1.4). The phase shift is calculated with Equation (1.31) and results with

$$\int_0^\infty \mathrm{e}^{-z/L}\mathrm{d}z = L \tag{1.36}$$

to

$$\Delta\varphi'(t) = \frac{4\pi}{\lambda_0} \frac{\mathrm{d}n}{\mathrm{d}T} \Delta T_0 L. \tag{1.37}$$

Replacing the thermal diffusion length L with Equation (1.5) allows to express the bound-

ary temperature ΔT_0

$$\Delta T_0 = \frac{\Delta\varphi}{\frac{4\pi}{\lambda_0}\frac{\mathrm{d}n}{\mathrm{d}T}\sqrt{Dt}}. \tag{1.38}$$

The phase shift curves for adiabatic heat diffusion into substrate are shown in Figure 1.23 for various instants. For the phase resolution of the later described scanning TIM setup of ∼5 mrad the expected temperature resolution is in the order of 1 K.

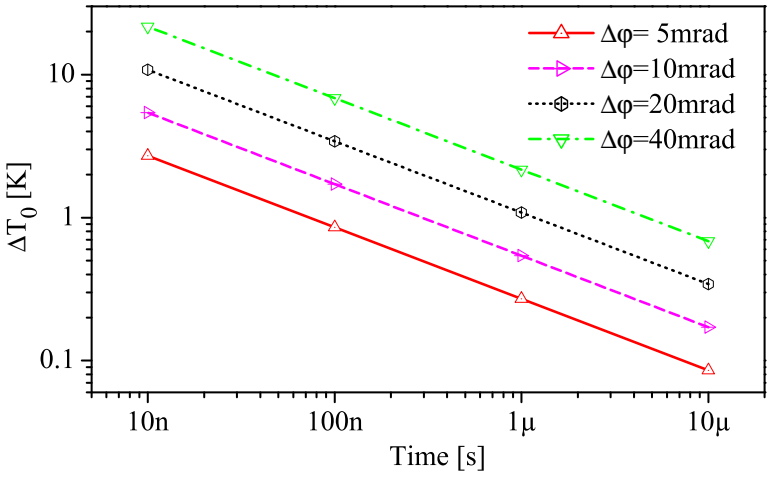


Figure 1.23: Phase shift for adiabatic heat diffusion in silicon vs. time.

Two complementary types of TIM methods are used to measure the optical phase shift: a scanning method (scanning TIM setup) – where whole transients with 3 ns time resolution are recorded at selected positions [74] and a holographic method (holographic TIM setup) [63] – where two interferogram images of the whole DUT can be obtained during a single stress pulse (5 ns exposure time). While the first method provides accurate information at dedicated positions of the scanning laser beam, the latter one acquires at once an overall view of the current flow in the whole device area. The obtained phase shift distributions usually can identify inhomogeneities in current flow and they can be used for calibration of TCAD (technology CAD, computer-aided design for semiconductor manufacturing technology) simulators at the chip designers. The scanning and the holographic transient interferometric mapping setups are described in Appendix A.

Chapter 2

Investigation of non-biased structures under ESD stress

For the multiple voltage requirements in BCD (combined bipolar, CMOS and DMOS) technology, low and high breakdown voltage ESD protection elements have to be designed in the same chip [75, 76]. Grounded gate (gg) NMOS protection devices are most popular elements for the low voltage ESD protection [12]. The homogeneity of current flow within single or multi-finger elements during the ESD pulse, i.e. the current to width scaling, is a major requirement to achieve high ESD robustness with different protection windows [77, 78]. It has been shown that the triggering uniformity of multi-finger gg-NMOS depends on pulse rise time and it is correlated with triggering homogeneity of single-finger devices [79–81]. Gate-coupled (gc) NMOS devices demonstrated a better trigger uniformity of multi-finger structures, as the activation (triggering) of intrinsic bipolar transistors is assisted by the NMOS drain currents [12, 77, 82].

Complex spatio-temporal dynamics of current distribution between two fingers of a vertical smart power DMOS device has been studied in [65]. Furthermore, some experimental evidence has been reported on pulse-to-pulse instabilities in current flow between different fingers in multi-finger gg-NMOS devices [20], but no direct observations of current sharing between the transistor fingers during ESD pulses have been reported. The TIM method has been used for verification of two-dimensional or three-dimensional simulation results in smart power bipolar devices [57, 83, 84], gg-NMOS devices [74] and for calibration of device simulation models at high currents and temperatures [85].

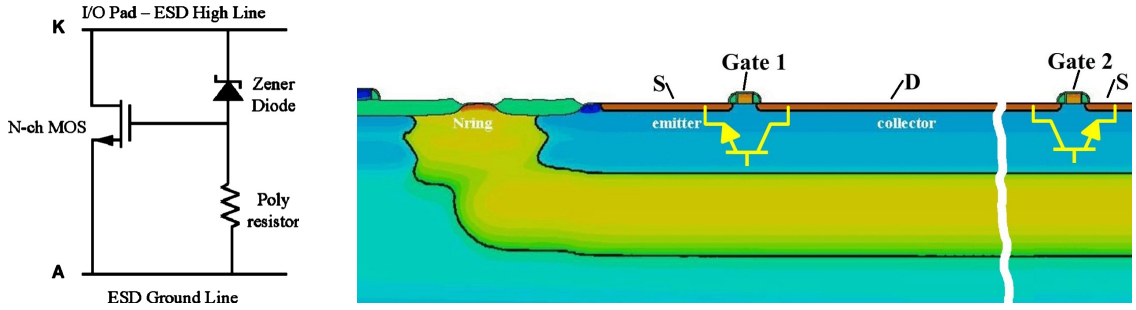
Investigations of triggering uniformity and current sharing under TLP stress of SOI multi-finger ESD protection structures provided by *Atmel* [86] are performed and the results are

presented in [87]. The outer fingers of the ESD protection devices are found to be inactive during reverse biased ESD stress. The TIM results were very relevant for improving two-dimensional TCAD simulations and optimizing the ESD protection devices.

The triggering uniformity as well as the scaling behavior of new single and multi-finger ESD protection structures in bulk silicon technology for ESD libraries will be investigated below. Observed pulse-to-pulse instabilities in device voltage and current sharing between the fingers will be analyzed in detail from the low currents up to the destruction level.

2.1 Description of the investigated devices

The investigated single and multi-finger 3.3V ESD protection devices are fabricated in 0.35 µm BCD6 bulk silicon technology at *ST Microelectronics* [88]. The circuit diagram of a gate-coupled single-finger NMOS device is shown in Figure 2.1a. The gate coupling is performed by a Zener diode and a resistor. The gate coupling circuit opens the channel of the NMOS transistor during an ESD event. This assists the activation of the intrinsic *npn* bipolar transistor and the ESD protection element goes to snap-back operation, where the voltage and the power dissipation are substantially reduced.



(a) (b)

Figure 2.1: (a) Circuit diagram of a gate-coupled single-finger NMOS device. The anode (A) of the ESD protection device is grounded and the cathode (K) is positively stressed. (b) Cross section with intrinsic bipolar transistors of two fingers of a multi-finger NMOS transistor. The structure is repeated for four, six and eight-finger devices.

More than 70 samples of gc-NMOS ESD protection structures with one to eight transistor fingers are systematically investigated. Devices with different number of fingers but with the same total width W_{tot} are investigated as well. The anode (A) of the ESD protection device is grounded and the cathode (K) is stressed. All measurements are performed at room temperature. The studied device types are listed in Table 2.1. The most important results are discussed below.

The cross section of two fingers of a multi-finger NMOS transistor with the intrinsic *npn* bipolar transistors is shown in Figure 2.1b. The NMOS fingers are embedded in a *p* well, which is surrounded by an *n* ring. The *n* ring is connected to drain. Devices with more than one finger have common drain contact in the middle of each double-finger. A schematic cross section of a six finger device is shown in Figure 2.2.

Device	Type	Total width	No. of fingers
ST-1	GCMOS	75 µm	2
ST-2	GCMOS	150 µm	2
ST-3	GCMOS	300 µm	4
ST-4	GCMOS	450 µm	6
ST-5	GCMOS	600 µm	8
ST-6	GCMOS	75 µm	1
ST-7	GCMOS	300 µm	2
ST-8	GCMOS	450 µm	2
ST-9	GCMOS without Zener	150 µm	2
ST-10	GCMOS without Zener	450 µm	6
ST-21	npn	150 µm	2
ST-22	npn	300 µm	4
ST-111	npn Lb=3 µm	300 µm	4
ST-112	npn Lb=3 µm	150 µm	2

Table 2.1: Studied types of ESD protection structures.

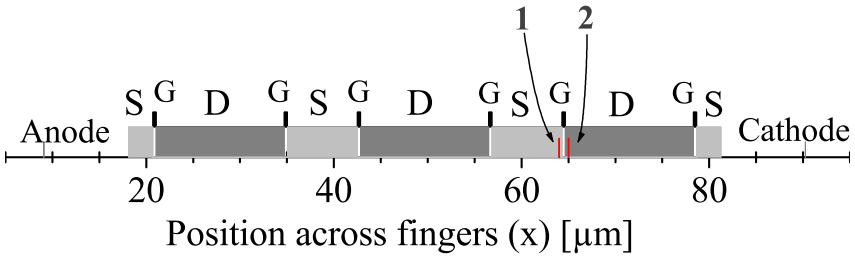


Figure 2.2: Schematic cross section of a six-finger NMOS transistor. Each double-finger has one drain (D) and two gates (G). At the left side is the anode pad and at the right side the cathode pad. "1" marks a point in the source (S) region ($x = 64\,\mu m$) and "2" a point in the drain region ($x = 65\,\mu m$).

2.2 Experimental details

2.2.1 Stressing scheme

A transmission line pulse generator (Figure 1.17) giving 100 ns square current pulses with 2.5 ns rise time is used for measurements of pulsed I-V characteristics and for pulsed excitation during the scanning TIM experiments. To get typical triggering behavior several devices of the same type (i.e. same number of fingers and W_{tot}) are investigated as well as a statistically large number of pulses is applied at the same current level in order to reveal multiple-voltage nature of pulsed I-V characteristics. The effect of the load line resistance is studied with several different load line resistors ($R_{\mathrm{ll}} = 50\,\Omega$, $500\,\Omega$, $1\,\mathrm{k}\Omega$ and $5\,\mathrm{k}\Omega$). The holographic TIM measurements are carried out with a solid-state switch as pulse generator (Figure 1.18) and a load line resistor of $R_{\mathrm{ll}} = 500\,\Omega$.

2.2.2 Optical methods

The silicon substrate of the samples is grinded and polished to get a sufficiently bright infrared image for optical investigations from the device backside. For the scanning TIM measurements the samples are glued and bonded to sample holders [16]. The repetition rate is set to 1 Hz to ensure cooling of the sample after each stress pulse.

The holographic (2D) TIM measurements are performed at a specially-designed wafer probe station [69], which allows simultaneous optical testing and electrical stressing of the samples by needle probes at wafer level.

The positions of the ESD failures are investigated from the back of the device with infrared microscopy using a *Vidicon* infrared camera with a spectral range of 400 nm to 1600 nm.

2.2.3 Device simulation

The device simulation is performed at *ST Microelectronics* and *University of Padova* [89]. Two-dimensional device simulation obtained by *Synopsis* TCAD tool *DESSIS* [90] is used to calculate the temperature and the excess carrier concentration. Using the *Synopsis* postprocessor *APEX* it is possible to calculate from the simulated data the thermal and excess carrier contributions to the optical phase shift as well as the total phase shift.

Figure 2.3 shows the circuit diagram for mixed-mode simulation of a two-finger device [91]. A resistor (R_1) at the drain of the first finger is introduced to consider small asymmetries

in the layout of the device. As shown later, this leads to a sequential triggering of the two intrinsic *npn* bipolar transistors in the device simulation.

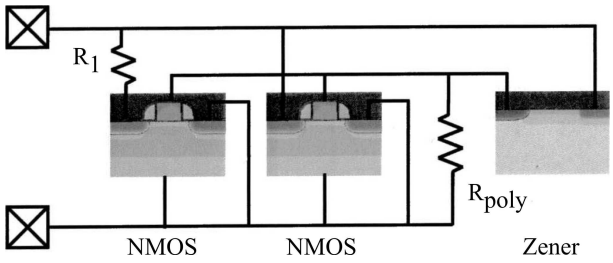


Figure 2.3: Circuit diagram for mixed-mode simulation of two-finger devices. A series resistor (R_1) at the drain of the first finger allows simulation of small asymmetries in the layout of the ESD protection device.

2.3 Electrical characterization

Electrical characterizations provide quick views to important device characteristics (i.e. breakdown voltage, snap-back voltage, destruction level).

2.3.1 DC characteristics

The measured DC characteristics of a two-finger device with total width of $W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$ are shown in Figure 2.4. It shows the breakdown voltage of the Zener diode at $V_{\mathrm{BD}} = 6\,\mathrm{V}$, the trigger voltage of the intrinsic (parasitic) bipolar transistor at $V_{\mathrm{T1}} = 9.4\,\mathrm{V}$, its trigger current at $I_{\mathrm{T1}} = 15\,\mathrm{mA}$ and the holding voltage of the device in snap-back operation at $V_{\mathrm{H}} = 5.4\,\mathrm{V}$. The simulation of the DC characteristics reproduces well the band to band tunneling ("1"), the break down of the Zener diode ("2"), the opening of the channel ("3") and the triggering of intrinsic *npn* bipolar transistor ("4"), which brings the device into snap-back operation ("5").

2.3.2 Pulsed *I*-*V* characteristics

The pulsed *I*-*V* characteristics are measured with up to 30 pulses for every stress level. The voltage and current waveforms are averaged over a limited time interval of a few nanoseconds at the end of each stress pulse, in order to reveal pulse-to-pulse instabilities in voltage and corresponding branches in *I*-*V* characteristics.

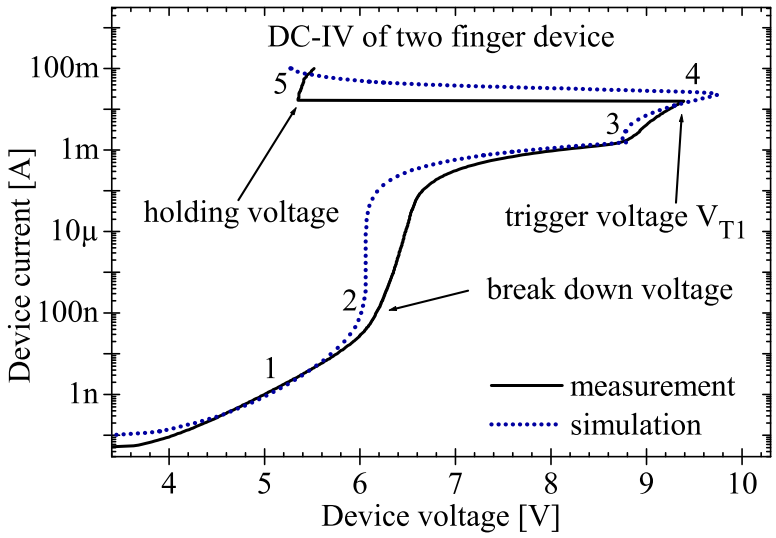


Figure 2.4: Measurement and simulation of DC characteristics of a two-finger ($W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$) device. The measured trigger voltage V_{T1} is 9.4 V.

Single and two-finger devices

The pulsed I-V characteristics of a single-finger device ($W_{\mathrm{tot}} = 75\,\mu\mathrm{m}$) measured with a load line resistance of $R_{\mathrm{ll}} = 1\,\mathrm{k}\Omega$ is shown Figure 2.5. The current is scaled to the device width. The TCAD simulation of a single-finger device ($W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$) shows a good agreement with experiments. Differences are visible at low currents (due to three-dimensional effects, which are shown later) and at high currents, due to overestimated temperature, which results in the onset of second breakdown around $12\,\mathrm{mA}/\mu\mathrm{m}$.

Figure 2.6 shows the pulsed I-V measurement of a double-finger device ($W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$) measured with $R_{\mathrm{ll}} = 1\,\mathrm{k}\Omega$. The gate coupling circuit opens the channels of all NMOS fingers. If the drain current of a particular finger reaches the trigger current level (I_{T1}) of its intrinsic bipolar transistor, then this bipolar transistor is activated – the finger is *triggered*. The triggering of the intrinsic bipolar transistor causes a drop in the device voltage and snap-back occurs. The fingers, which were not triggered, stay inactive until the voltage across the device reaches again the level for activation of the intrinsic bipolar transistors (V_{T1}).

The simulation shows a two times higher differential resistance for currents below 1 A. This corresponds to triggering of only one finger – the finger with the higher drain current (lower total resistance). Above 1 A the bipolar transistors of both fingers are triggered and a good agreement to the experiments is achieved until the (underestimated) second breakdown occurs.

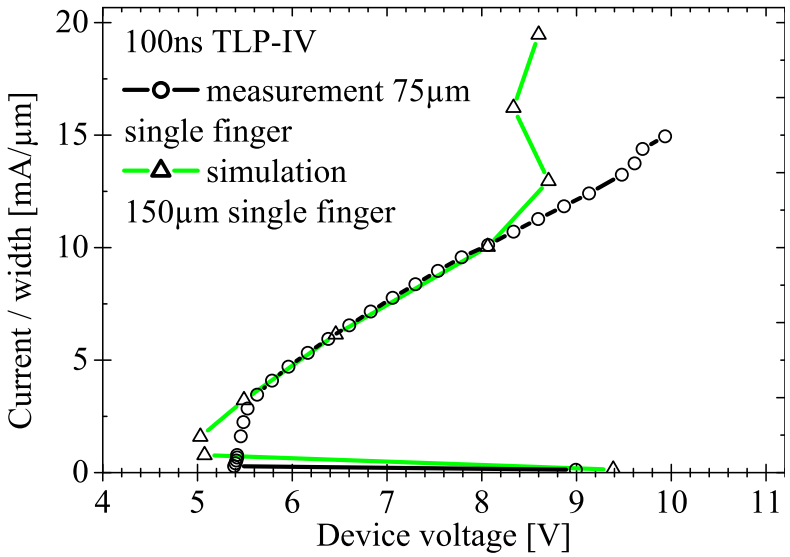


Figure 2.5: Pulsed I-V measurement of a single finger device with a total width of $W_{\mathrm{tot}} = 75\,\mu\mathrm{m}$ showing a significant kink around $3.5\,\mathrm{mA}/\mu\mathrm{m}$. The current is scaled to the device width. The simulation of a single finger device with $W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$ shows the same differential resistance per device width and too early second breakdown.

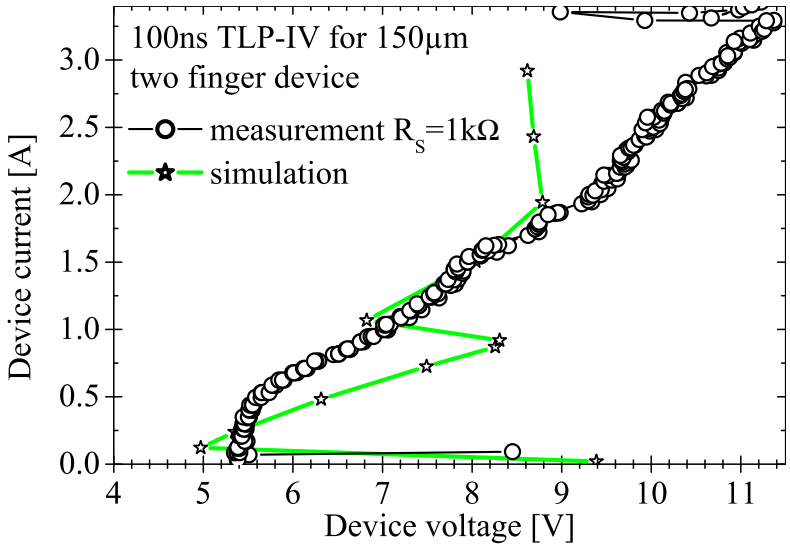


Figure 2.6: Measured and simulated pulsed I-V characteristics for a two finger device with a total width of $W_{\mathrm{tot}} = 150\,\mu\mathrm{m}$. The simulation shows a sequential triggering of the two fingers and the voltage drop due to second breakdown.

A detail of the pulsed I-V measurements for low currents of single, two and four-finger devices is shown in Figure 2.7. The current is scaled to the total device width. The I-V characteristics exhibit a significant kink at $J_{\text{kink}} \simeq 3.5\,\text{mA}/\mu\text{m}$, where the differential resistance changes from very small values ($\sim 0.35\,\Omega$ for $J < J_{\text{kink}}$) to much higher values ($\sim 4\,\Omega$) for $J > J_{\text{kink}}$ due to drain and source region series resistances. As shown later, this kink in the I-V characteristics is related to the change from an inhomogeneous current flow for $J < J_{\text{kink}}$ to a homogeneous one for $J > J_{\text{kink}}$.

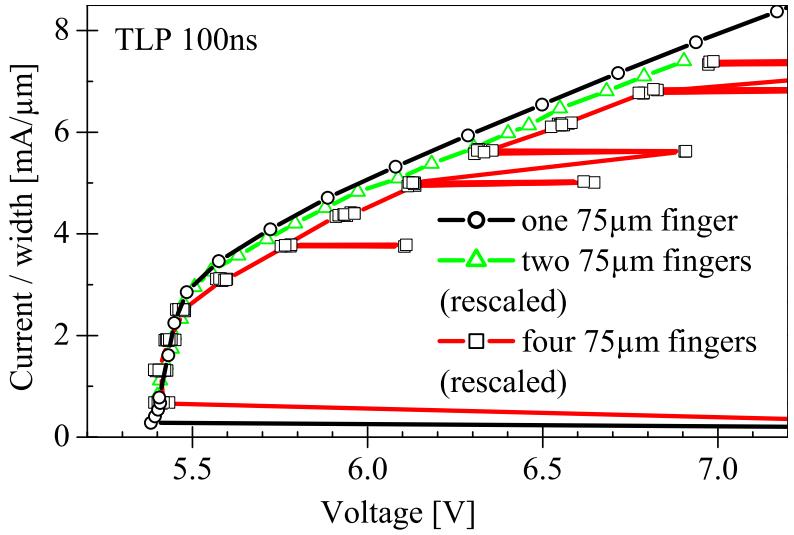


Figure 2.7: Low current pulsed I-V measurements of single, two and four-finger devices showing kinks when the full device area is active. The measurements are rescaled to the total width W_{tot}.

Four and more finger devices

In comparison to the double finger devices the high current I-V characteristics of multi-finger devices exhibit pulse-to-pulse instabilities for device voltages below the trigger voltage (V_{T1}). This results in several branches with well "*quantized*" differential resistances in the I-V characteristics. Example of such typical measurement on a six-finger device using $R_{\text{ll}} = 500\,\Omega$ is given in Figure 2.8. The lines indicate several differential resistances according to the number of triggered fingers. The different voltage states for the same current level correspond to a different number of triggered intrinsic bipolar transistors. However the triggered fingers stay always on during the current pulse (i.e. there are no voltage fluctuations during the pulse).

The effect of pulse generator load line ($R_{\text{ll}} = 500\,\Omega$, $1\,\text{k}\Omega$ or $5\,\text{k}\Omega$) on the I-V characteristics is investigated as well. Figure 2.9 shows the I-V characteristics measured by a $50\,\Omega$

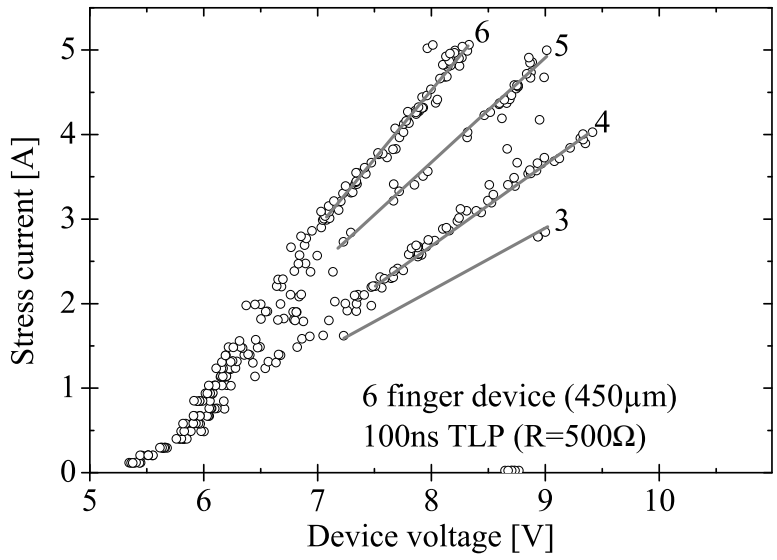


Figure 2.8: Pulsed *I-V* measurement of a six-finger device with $R_{\mathrm{ll}} = 500\,\Omega$. The lines indicate the slopes of differential resistances according to the marked number of triggered fingers.

system, where the instabilities in voltage are substantially reduced. Similar behavior is observed in devices with different number of fingers. The 50 Ω system has no current overshoots and consequently less instabilities and longer rise times.

Failure current

The scaling of the 100 ns TLP failure level is shown in Figure 2.10, where the total number of fingers is indicated. The failure criterion is a leakage current exceeding 100 nA at a device voltage of 4 V. The TLP failure current scales nearly linearly with the total device width and the failure level is at a current density of $J_{\mathrm{F}} \simeq 16\,\mathrm{mA/\mu m}$.

2.4 Internal device behavior

The internal distribution of temperature and injected (excess) carriers is analyzed with linear TIM scans along the device cross section, as well as along the width of the fingers. The measurements are performed under constant current TLP stress with a load line resistor of $R_{\mathrm{ll}} = 1\,\mathrm{k\Omega}$.

The phase shift waveforms at the source and the drain region of a six-finger device (see "1" and "2" in Figure 2.2) are shown in Figure 2.11 for a 100 ns 3.8 A pulse. The phase

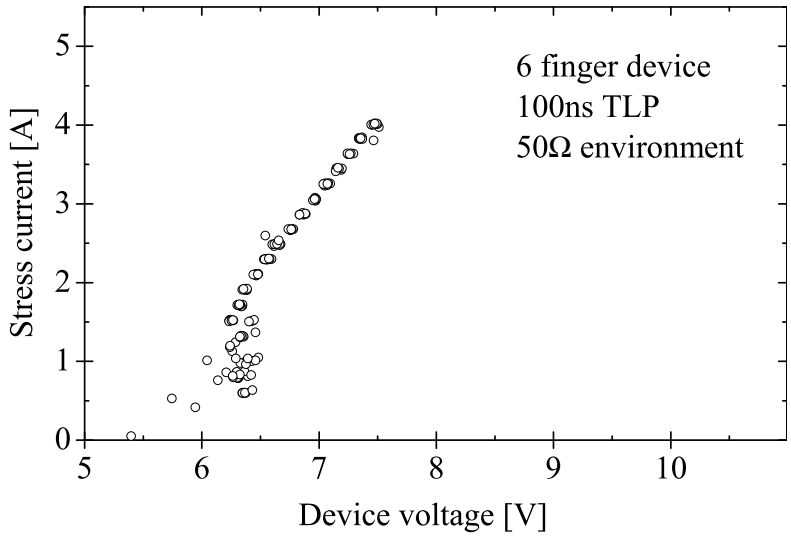


Figure 2.9: Pulsed I-V measurement of a six-finger device with $R_{\mathrm{ll}} = 50\,\Omega$.

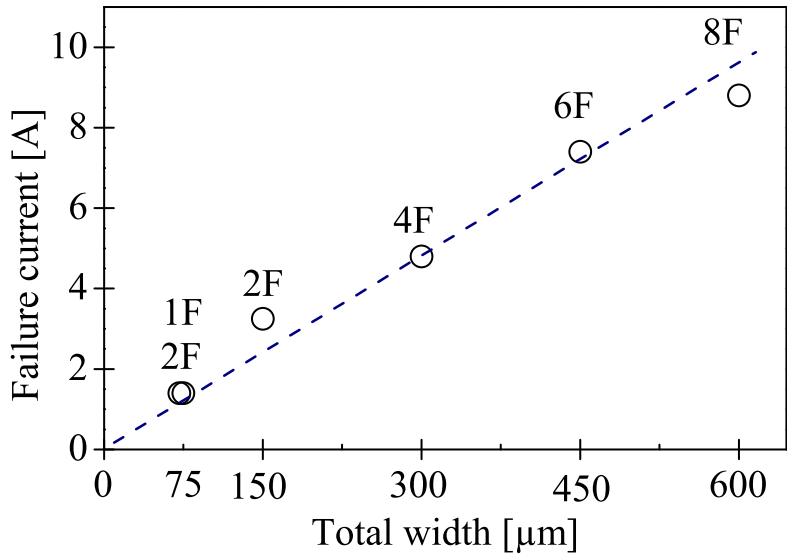


Figure 2.10: Scaling of the 100 ns TLP failure level. The failure level is around 16 mA/µm. Failure criterion is leakage current exceeding 100 nA at a device voltage of 4 V.

shift signal at the drain area increases during the stress pulse. The slope is proportional to the dissipated power ("1"). The phase measurement at the source area shows negative phase shift ("2") up to −0.16 rad during the stress pulse due to electron injection into the source region. Superimposed is the heating signal ("3"). At the end of the stress pulse the electron injection is stopped and the phase signal shows a sharp increase ("4") due to a lack of the negative phase contribution. After the stress pulse some temperature increase ("5") still occurs due to heat transfer from the hotter drain region. Exemplarily decomposed phase components (from a different experiment) are shown in Figure 3.17.

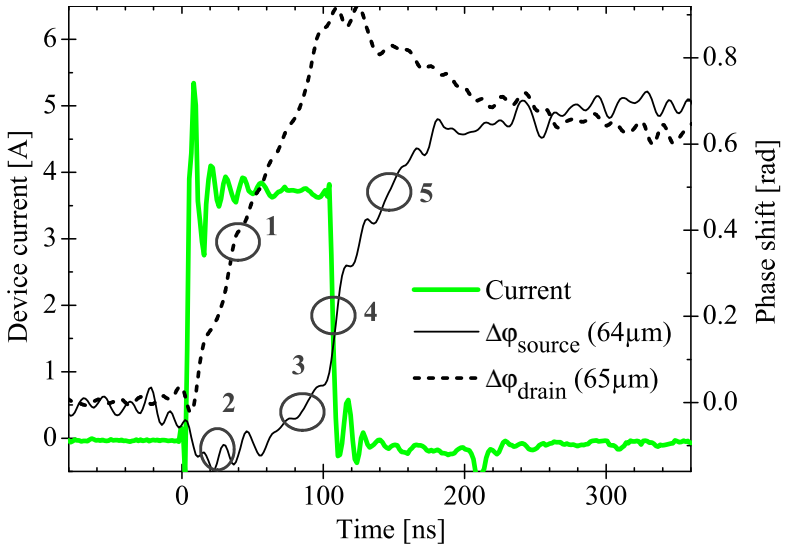


Figure 2.11: Phase shift measurement at the source and drain region of a six-finger device (see "1" and "2" in Figure 2.2) for a 100 ns 3.8 A pulse.

Triggering uniformity and current sharing between the fingers is studied by both scanning TIM and holographic (2D) TIM methods. Single fingers in multi-finger devices are scanned systematically. The phase distribution is measured at different current levels to investigate the device behavior at low, medium and high (destructive) stress pulses.

2.4.1 Inhomogeneous triggering

For total current densities below J_{kink} ($\sim 3.5\,\text{mA}/\mu\text{m}$) an inhomogeneous phase distribution along the fingers is observed. The phase measurements in Figure 2.12 show the current distributions at $t = 100\,\text{ns}$ for 0.1 A, 0.2 A and 1 A stress pulses. For $J < J_{\text{kink}}$ the current flow forms a large current filament centered in the middle of the device. The width of the filament at $I = 0.1\,\text{A}$ ($I = 0.2\,\text{A}$) is around 28 µm ($\sim 57\,\mu\text{m}$). The phase amplitude is nearly equal for 0.1 A and 0.2 A stress conditions indicating a nearly constant

current density of $\sim 3.5\,\mathrm{mA/\mu m}$ inside the filaments. Outside the filaments the current density is zero. The shape of a filament does not change significantly with time.

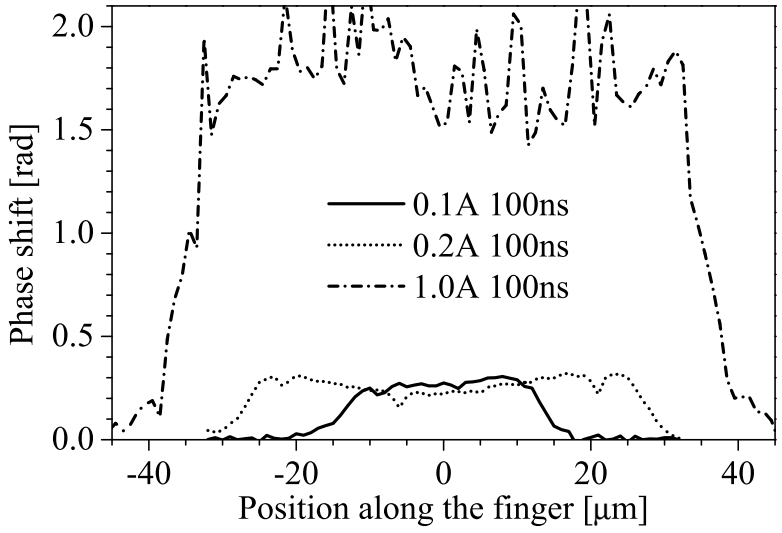


Figure 2.12: Measured phase distribution at $t = 100\,\mathrm{ns}$ along a $75\,\mu\mathrm{m}$ single finger device for 0.1 A, 0.2 A and 1 A 100 ns stress pulses.

As the stress current increases, also the device active area increases until the total device width is active at $I_{\mathrm{stress}} / W_{\mathrm{tot}} = J_{\mathrm{kink}}$, similar as in [92, 93]. This shows that the active width of the device is linearly proportional to the stress current. Such a device behavior of inhomogeneous current distribution results in nearly zero differential resistance in the pulsed I-V characteristics below J_{kink}. Some models of such I-V characteristics are given in [74, 94, 95]. When the device's active area reaches the total width of the device the current density starts to increase with increasing stress (see the curve at 1 A in Figure 2.12) and the I-V characteristics show a finite differential resistance.

The same experiments are performed for the multi-finger devices. The optical mapping shows similar results for stress currents below the I-V kink. The multi-finger device specific kink current (I_{kink}) is linearly increasing with the total device width.

2.4.2 Homogeneous triggering

The current is found to be distributed nearly homogeneously within the fingers for total current densities above J_{kink} ($\sim 3.5\,\mathrm{mA/\mu m}$).

Single and two-finger devices

The phase shift measurement across a single-finger device ($W_{\text{tot}} = 75\,\mu\text{m}$) is shown in Figure 2.13 at $t = 30\,\text{ns}$ during 1 A stress pulses. Most heating occurs at the drain side ("D") of the device, where the highest potential drop occurs. The simulated total phase shift, as well as its positive thermal and negative free-carrier components are also given in the Figure. The negative component peaks at the source side due to carrier injection in the forward biased base / emitter junction. From the small amplitude of the phase signal it can be also seen that the measured downward peak at the gate cannot be explained by the carrier injection and it must be an optical artifact. It could be due to light scattering at the gate edge [74] or light absorption at the polysilicon [96]. Phase averaging over the diameter of the scanning laser beam is used in order to model the measurement conditions, but the phase shift is still overestimated.

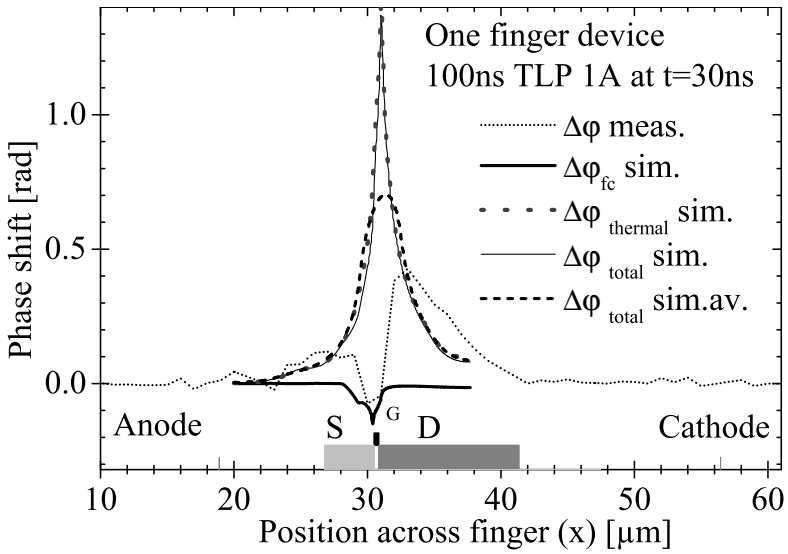


Figure 2.13: Phase shift measurement and simulation at $t = 30\,\text{ns}$ across a single-finger device with $W_{\text{tot}} = 75\,\mu\text{m}$ during 1 A stress pulses. The simulated thermal ($\Delta\varphi_{\text{thermal}}$) and free carrier ($\Delta\varphi_{\text{fc}}$) contributions are shown as well. The averaged signal is denoted by "av".

The phase shift measurement at $t = 90\,\text{ns}$ is shown in Figure 2.14 together with the corresponding TCAD simulations. Averaging of the simulated phase shift over the diameter of laser beam is necessary to get a satisfactory agreement with the measurements, but the phase shift is still a little overestimated. The simulated absolute surface temperature has a peak of 1150 K at 1 A. This temperature is likely overestimated, which is consistent with the underestimated simulated second breakdown in Figures 2.5 and 2.6.

The investigation of the current sharing in a double finger device during 2 A 100 ns TLP

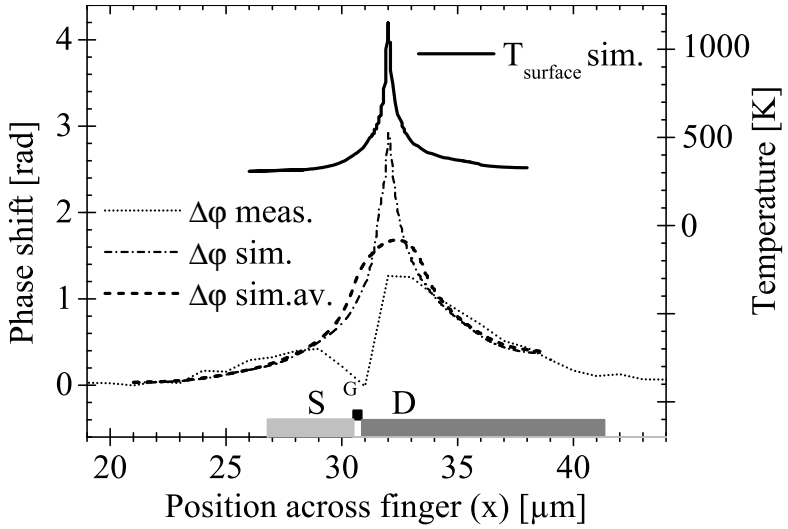


Figure 2.14: Phase shift measurement and simulation at $t = 90\,\text{ns}$ across a single-finger device with $W_{\text{tot}} = 75\,\mu\text{m}$ during 1 A stress pulses. The averaged signal is denoted by "av.". The simulated absolute surface temperature shows a peak of 1150 K.

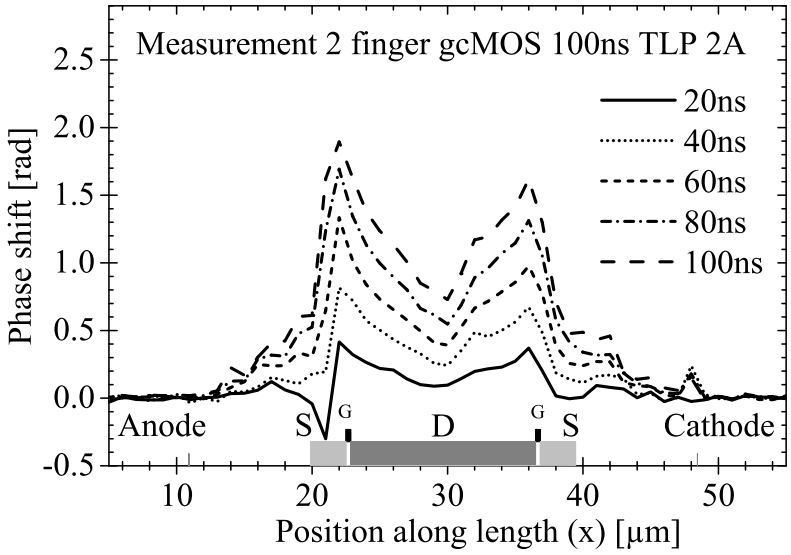
stress pulses shows overlapping phase shift peaks (see Figure 2.15a), giving thus a double peak distribution with the maxima at the drain edge of the channels. A slightly lower heating of the cathode side finger due a higher series resistance (R_1) in the layout is observed. Figure 2.15b shows the well matching phase shift simulation of the two-finger device, which confirms the lower heating of the cathode-side finger.

Four and more finger devices

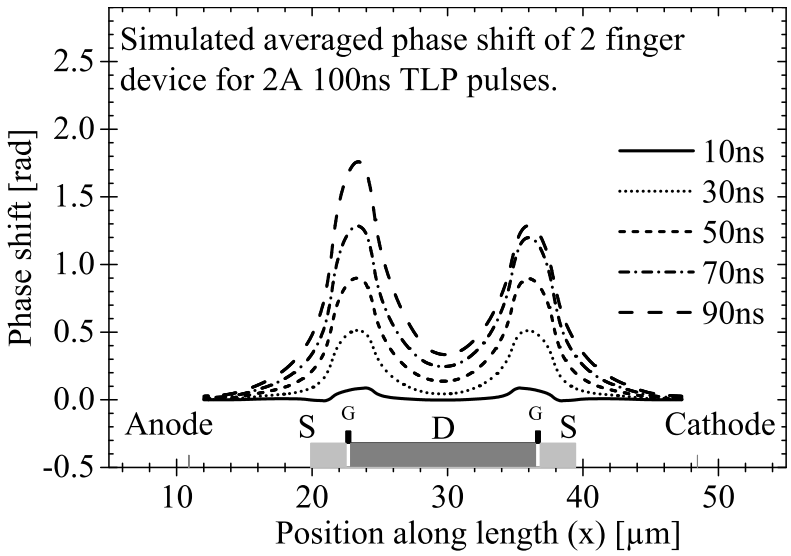
The repeating double peak distribution in the phase signal can also be distinguished in multi-finger devices. Figure 2.16a shows the phase shift scan across a six-finger device for $t = 20\,\text{ns}$ and $t = 100\,\text{ns}$ for 3.8 A 100 ns pulses. The averaged plot at $t = 20\,\text{ns}$ shows a strong negative phase shift at the inner sources due to high carrier injection. These positions are marked with "2" and "3" in Figure 2.16a. Figure 2.11 shows the phase shift in time domain at the source region ($x = 64\,\mu\text{m}$) compared to the drain region ($x = 65\,\mu\text{m}$).

In Figure 2.16a four data are given at $t = 100\,\text{ns}$ for each spatial position to visualize trigger instabilities (inactivity of fingers) at the first, fifth and sixth finger ("1", "4", "5"). The cathode side finger is less heated – similarly as in the two-finger device.

The phase shift scan along the width of the anode side finger (#1) is shown in Figure 2.16b. The observation of discrete levels in the measured total phase shift among the fingers is



(a)



(b)

Figure 2.15: (a) Phase shift measurement of two-finger device with $W_{\text{tot}} = 150\,\mu\text{m}$ during 2 A 100 ns TLP stress pulses. (b) Phase shift simulation of two-finger device with $W_{\text{tot}} = 150\,\mu\text{m}$ during a 2 A 100 ns TLP stress pulse. The lower heating of the cathode-side finger is due to a higher series resistance in the layout.

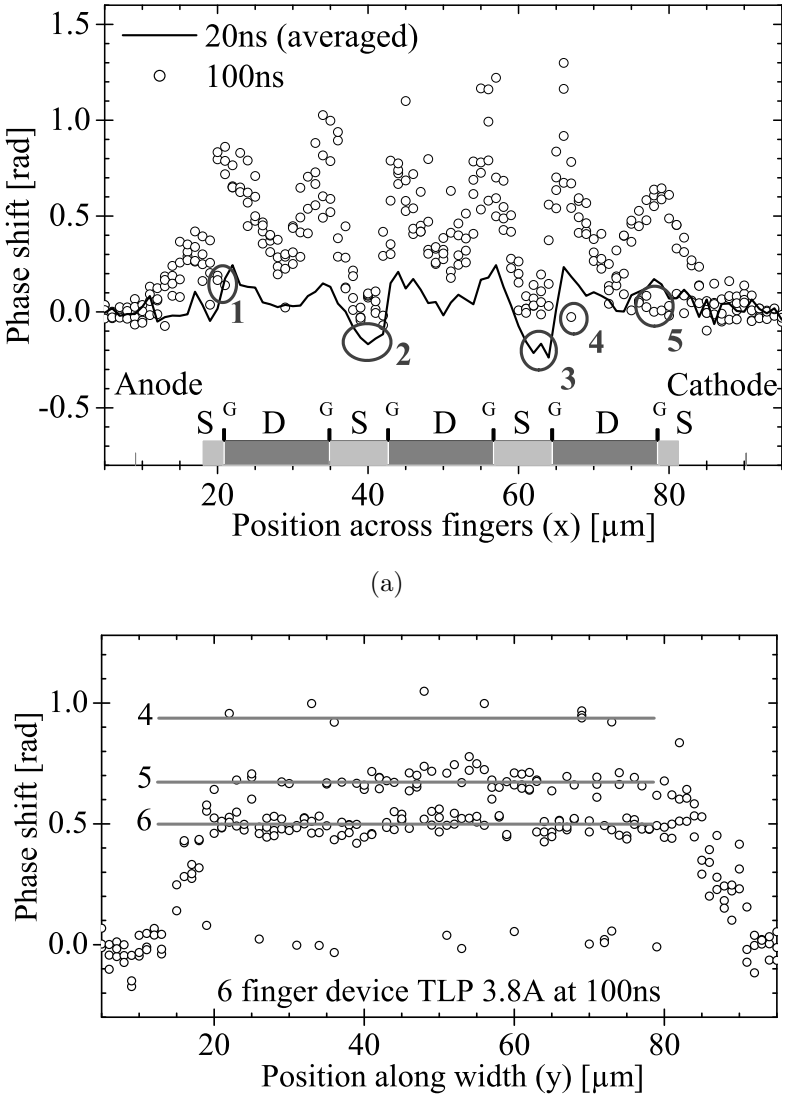


Figure 2.16: (a) Phase shift measurement for 100 ns 3.8 A TLP pulses across a six-finger device with $W_{\text{tot}} = 450\,\mu\text{m}$. (b) The phase shift measurement along the anode side finger of this six-finger device at $x = 21\,\mu\text{m}$ during 3.8 A 100 ns TLP stress pulses shows discrete phase levels for six, five and four triggered fingers. A phase shift around zero indicates that this finger is not triggered in that particular measurement.

due to a different number of triggered fingers (N_{TR}). Along the triggered fingers the current distribution is nearly equal.

The discrete levels of phase shift can be expressed similar to Equation (1.35) as

$$\Delta\varphi \simeq a\frac{N}{N_{\mathrm{TR}}}V_{\mathrm{NTR}}\cdot I\cdot t \tag{2.1}$$

with fitting coefficient a ($1.73 \cdot 10^5\,\mathrm{rad/J}$), total number of fingers N (6), number of triggered fingers N_{TR} ($4 \ldots 6$), device voltage for number of triggered fingers V_{NTR} (see Figure 2.8), device current I (3.8 A) and time t (100 ns).

The arrangements of the triggered fingers for the same current level are also systematically investigated using the holographic TIM method. Figure 2.17 shows holographic TIM images recorded at $t = 100\,\mathrm{ns}$ of 3.5 A pulses with 150 ns duration. The phase images show three observed particular distributions of current flow over the fingers – so called "*triggering patterns*". In Figure 2.17b all six fingers are active (bright). Five fingers are active in Figure 2.17c and only four fingers are active in Figure 2.17d. The fingers in the middle of the structure are always triggered and the finger at the cathode side is most unstable. This single shot measurements confirm, that the observed pulse-to-pulse instabilities in the number of triggered fingers are the origin of the voltage instabilities in the I-V characteristics of multi-finger devices (see Figure 2.8).

2.4.3 Destructive ESD pulses

The current distribution in the ESD protection structures is also investigated during destructive ESD pulses with 150 ns duration using the holographic TIM method with two instant imaging (two lasers are used to illuminate the device during a single stress pulse). Similar approach as in [69, 97] is used. To assure that the device destroys during a single stress pulse, the stress current is chosen above the 100 ns TLP failure current level. The maximum current of the used solid-state pulse generator is 12 A.

To confirm any failure the leakage current is measured before and after the applied stress pulse. Typical leakage current characteristics of a device before and after a destructive pulse are given in Figure 2.18. Three single-finger, eleven two-finger, five four-finger, ten six-finger and five eight-finger devices are investigated under destructive ESD stress pulses.

Figure 2.19a shows the holographic TIM phase map of an eight-finger device at time $t = 50\,\mathrm{ns}$ of a 12 A destructive stress pulse with 150 ns duration. All eight fingers are

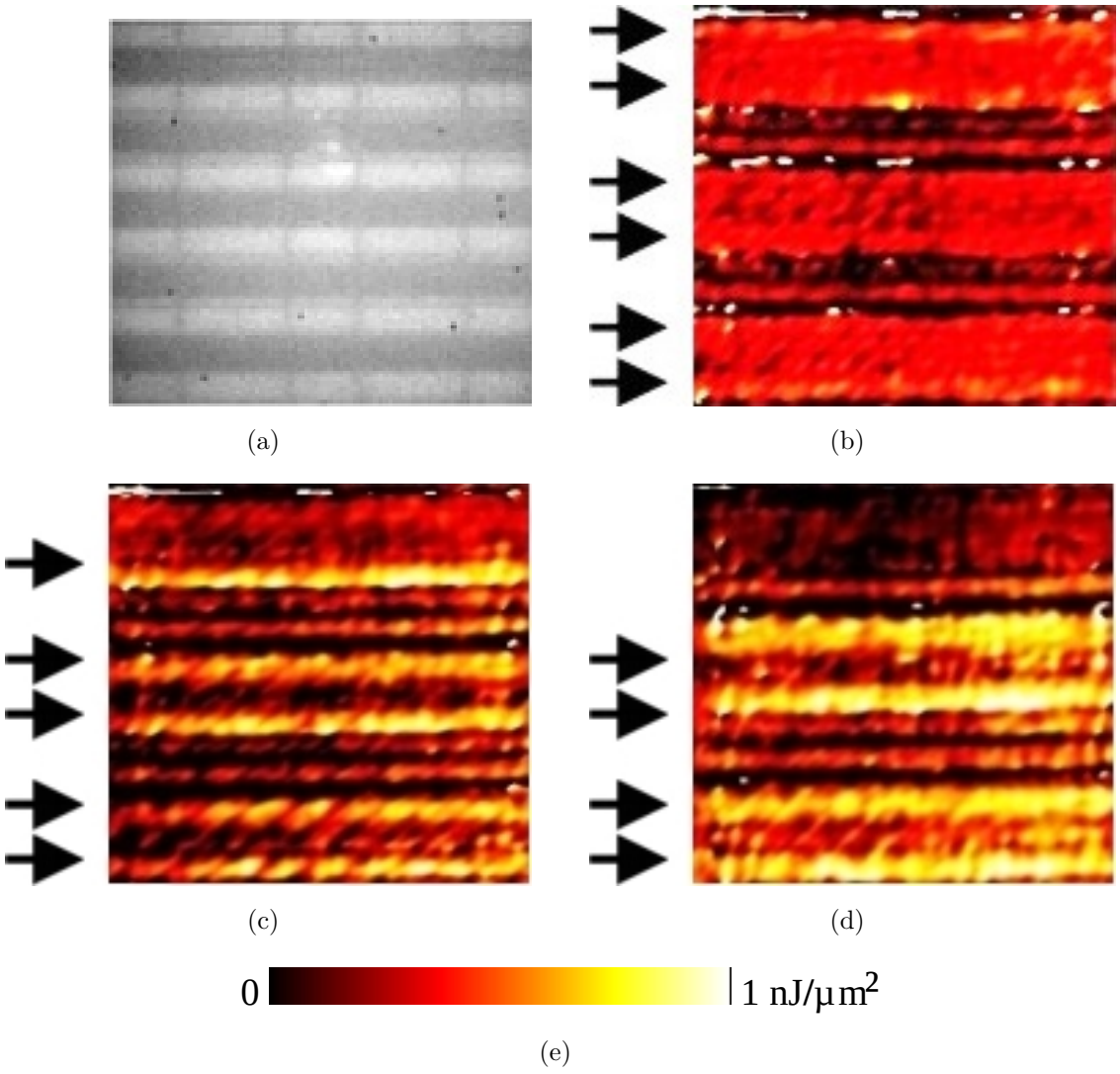


Figure 2.17: (a) Backside infrared image of a six-finger device. At the top side is the stressed cathode pad. The phase images of this device show three observed particular triggering patterns. The arrows indicate the triggered fingers. (b) All six fingers activated. (c) Five fingers activated. (d) Four fingers activated. (e) The measured phase shift is recalculated to thermal energy density. The holographic TIM images are recorded at $t = 100\,\text{ns}$ of 3.5 A 150 ns pulses. The width of each finger is 75 µm.

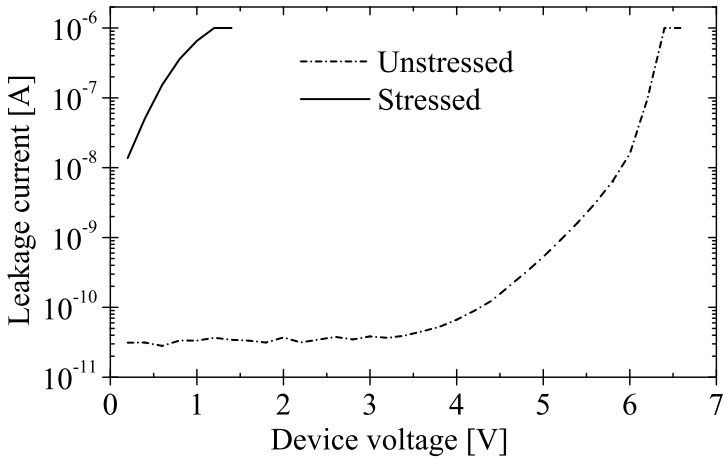
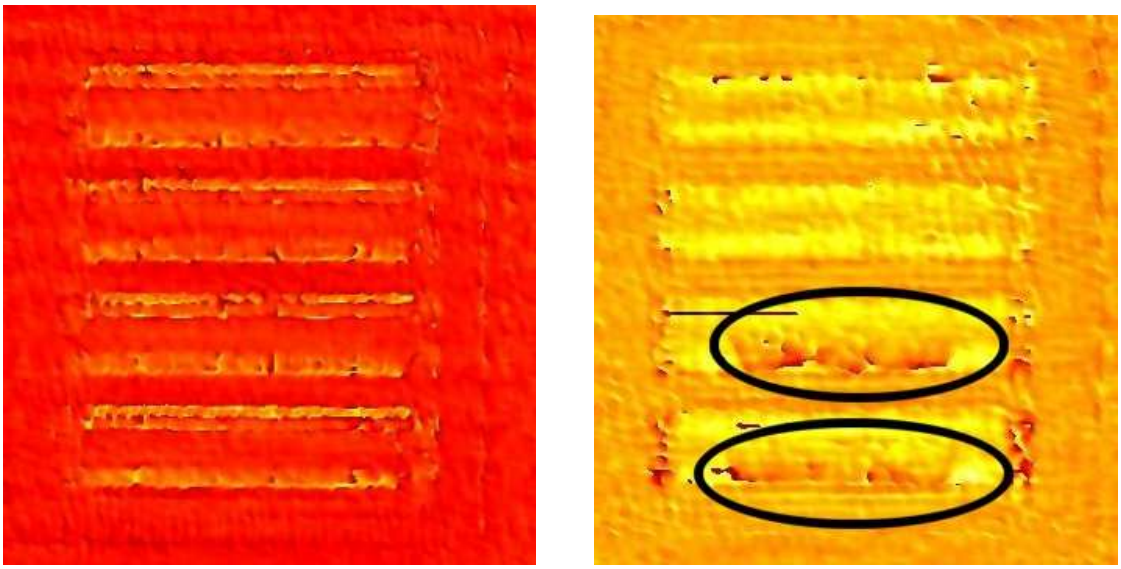


Figure 2.18: Leakage current measurement of a two-finger device before and after a 4 A destructive stress pulse (hard failure).

homogeneously triggered. At $t = 100$ ns an inhomogeneous phase distribution due to inhomogeneous current flow is observed in two fingers (marked by ellipses in Figure 2.19b). At these places the absolute value of the phase shift is difficult to extract because the intensity of the interferogram image is very low due to a locally decreased reflectivity [96]. It is supposed that either band to band absorption due to high temperature [97] or formation of black spots (indeed observed in failure analysis) before the imaging time at $t = 100$ ns are the origin of this effect. The measurements on devices with different finger number show qualitatively the same results.

2.4.4 Failure analysis

Figure 2.20 shows the infrared image from the back of an eight-finger device after a destructive 12 A stress pulse. There are two black spots (melted regions), which are marked with the large ellipse. The small ellipses indicate the position of a few black spots observed in other investigated devices. Most of the ESD failures of the investigated devices occurs at the anode (A) side of the device (grounded electrode), similarly as the position marked with the large ellipse. This agrees with the slightly higher heating of the anode side finger, observed in phase shift scanning measurements in Figure 2.15a.



(a) (b)

Figure 2.19: (a) Measured phase shift distribution at $t = 50\,\text{ns}$ of a destructive 12 A stress pulse shows that all eight fingers are active. (b) At $t = 100\,\text{ns}$ all fingers are still active, but an inhomogeneous phase distribution due to inhomogeneous current flow is observed in two fingers (see ellipses).

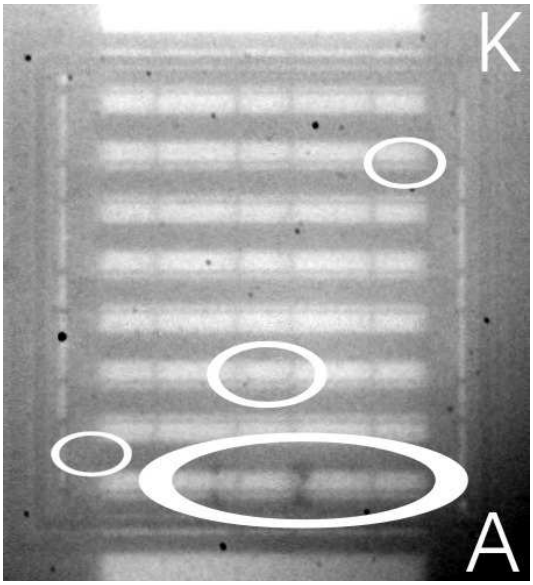


Figure 2.20: Backside infrared image of an eight-finger device after a destructive 12 A stress pulse showing two black spots (see large white ellipse). The small ellipses indicate few black spots of other samples. The most black spots of the investigated devices are located in the large ellipse.

2.5 Summary of ESD investigations

Pulse-to-pulse instabilities in the pulsed *I-V* characteristics of gate-coupled multi-finger NMOS ESD protection structures were explained by directly observed triggering patterns using the holographic TIM method. The different voltage branches in the pulsed *I-V* characteristics were caused by different numbers of triggered intrinsic *npn* bipolar transistors. The measured phase shift in single- and two-finger devices was compatible with the TCAD simulations. It was found that the central fingers of multi-finger devices were always activated, while the cathode side fingers behaved most unstably.

The instability phenomenon is not dangerous for the ESD robustness as the current is homogeneously distributed within the fingers at high currents and the instabilities cease for device voltages above the trigger voltage (V_{T1}) because all fingers become active. This explains the rough linear scaling of the 100 ns TLP failure current with the total device width. The ESD damage occurs mostly at the anode side of the device, which is consistent with the TIM observations at low currents.

Chapter 3

Latch-up investigations

While in the previous Chapter *non-biased* circuits were investigated, this Chapter focuses on *external* transient latch-up studies at *biased* CMOS circuits using a pulse generator, a guard-ring supply domain and a *floating* latch-up detector[1] (SCR) supply domain.

Latch-up may occur due to current injection directly at diffusions of an SCR structure (*internal* latch-up, see dashed arrows in Figure 1.13) [2]. For such internal latch-up studies ESD-like pulses are superimposed to a constant bias source to emulate ESD events at biased circuits. For ESD protection during the circuit operation, ESD protection devices have to fulfill requirements to avoid the latch-up during ESD surges, battery connection, etc. [98–100]. Investigations of multi-finger lateral DMOS clamps and SCRs provided by *X-FAB Semiconductor Foundries* [101] are performed and the results are presented in [102]. During latch-up, the current in the lateral DMOS clamps flows just in a single spot and the trigger position is random and independent on device type.

A more complicated situation appears, if latch-up occurs due to substrate currents, which are injected at junctions located in some distance from the triggered SCR structure (*external* latch-up, see solid arrows in Figure 1.13) [4, 103]. The use of multiple supply domains makes the situation even more complex. In order to provide appropriate latch-up protection concepts for various layouts, a fundamental understanding of the substrate current distribution is essential.

[1] The latch-up detector structure will be explained below.

3.1 External transient injection

External transient latch-up is investigated at specially designed CMOS test structures and commercial I/O cells. Based on the work of *K. Domański*, who performed two-dimensional TCAD simulations and basic electrical experiments on many different CMOS latch-up test structures [4], the excess carrier distribution is experimentally analyzed in selected samples using the transient interferometric mapping technique. As further stage of investigations, experiments with a *floating* latch-up detector (SCR) supply domain are performed to reflect real application conditions.

The test structures, which are most prone to latch-up (n and p wells of SCR facing to injector) were identified by *K. Domański*. He supposed a three-dimensional triggering mechanism. The orientations of the test structures are shown in Figure 3.1 and the corresponding latch-up trigger currents for 500 ns pulses are shown in Figure 3.2 [4]. These test structures could be simulated within a two-dimensional TCAD system only with significant simplifications. Three-dimensional simulations of these test structures would be very difficult and time consuming. Thus, excess carrier and heat spreading are analyzed by TIM experiments as function of time and position. The critical process of current crowding is qualitatively analyzed on chip-level and should explain the higher latch-up sensitivity in these test structures.

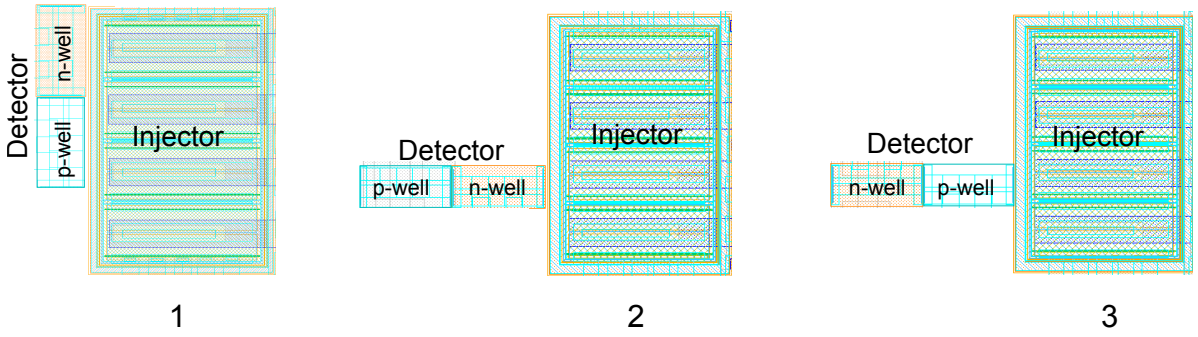


Figure 3.1: Top view of different test structures. (1) n and p wells of SCR facing to injector. (2) n well of SCR facing to injector. (3) p well of SCR facing to injector.

The impact of guard-ring biasing, guard-ring layout and type (n or p) on the substrate current distribution is investigated as well. The measurements are complemented with two-dimensional simulations of *K. Domański* to depict the current flow in the depth (z) of the structures[2].

[2] TIM shows only the refractive index changes, which are integrated along the depth.

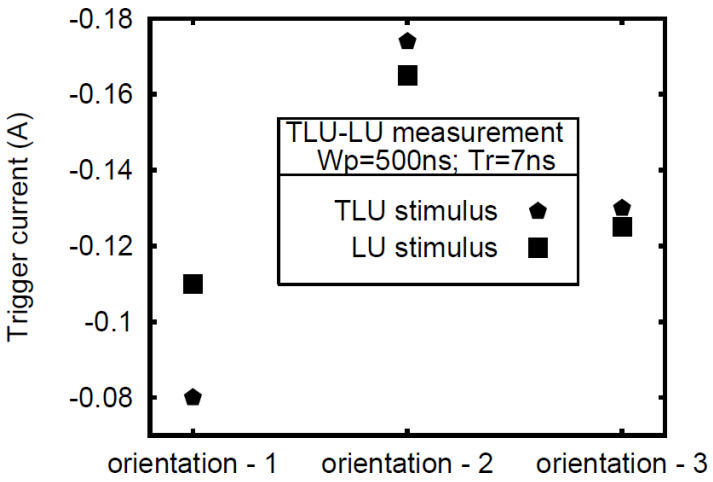


Figure 3.2: Latch-up sensitivity of different SCR orientations [4]: (1) n and p wells of SCR facing to injector. (2) n well of SCR facing to injector. (3) p well of SCR facing to injector.

3.1.1 Description of test structures and I/O cells

The test structures and I/O cells are processed in a p substrate dual-well 90 nm bulk CMOS technology at *Infineon Technologies AG* [104]. The n and p wells are 1 µm deep. The p well covers the whole wafer except the n well areas. The highly doped n^+ and p^+ implantations are approximately 100 nm deep. The diffusions are separated by 0.5 µm deep shallow trench isolations (STI). Table 3.1 gives an overview of the analyzed test structures and layout variations.

Latch-up detector structure

The parasitic SCR structure of a CMOS inverter is a latch-up sensitive structure, which can be used as latch-up detector (see Figures 1.1 and 1.2). The gates and drains of the inverter do not affect the SCR structure, thus they are omitted in design and simulation of the latch-up test structures.

The sensitivity of parasitic SCR structures depends on topology as well as on doping profiles. The *worst-case* design dimensions [4] (see Figure 3.3) are:

- minimum edge distance of p^+ contact to n well ($d_{\mathrm{p+}}$) and of n^+ contact to p well ($d_{\mathrm{n+}}$)
- maximal spacing of n_{sub} contact to p^+ contact (d_{nsub}) and of n^+ contact to p_{sub} contact (d_{psub})

Structure	width [µm]	gap [µm]	polarity	elec-trical	optical	short name
TLU-GR-2n	0.24	1	neg.	✓	✓	*small*
TLU-GR-2p	0.24	1	pos.	✓	✓	*small*
TLU-GR-4n	1	1	neg.	✓	✓	
TLU-GR-4p	1	1	pos.	✓	✓	
TLU-GR-11n*	2	10	neg.	✓		
TLU-GR-11p*	2	10	pos.	✓		
TLU-GR-12n*	2	20	neg.	✓		
TLU-GR-12p*	2	20	pos.	✓		
TLU-GR-13n*	2	40	neg.	✓	✓	*large*
TLU-GR-13p*	2	40	pos.	✓	✓	*large*
TLU-DET-5n	2	1	neg.	✓	✓	n well to inj.
TLU-DET-5p	2	1	pos.	✓	✓	n well to inj.
TLU-DET-6n	2	1	neg.	✓	✓	p well to inj.
TLU-DET-6p	2	1	pos.	✓	✓	p well to inj.
TLU-08-IO-D			neg.	✓	✓	*I/O cell*
TLU-09-IO4			neg.	✓	✓	I/O cell-4
TLU-09-IO5			neg.	✓	✓	I/O cell-5
TLU-10			neg	✓	✓	*d. trench*

Table 3.1: Studied types of latch-up test structures and I/O-cells with indicated guard-ring width and gap between second guard-ring and third guard-ring (or latch-up detector). Structures having a third guard-ring are denoted with *.

➢ smallest allowed area of contacts (d_c).

This worst-case SCR structure is implemented as latch-up detector, which is connected to a separate supply domain (VDD_{det} and VSS_{det}).

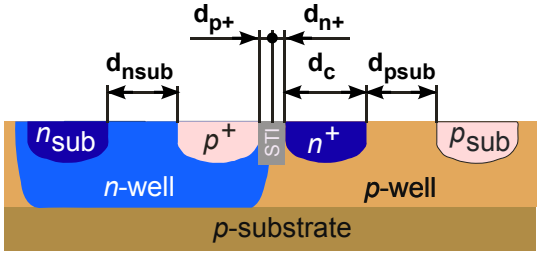


Figure 3.3: Most critical design dimensions of a parasitic SCR structure [4]. The equivalent circuit of the SCR structure is described in Figure 1.2.

Test structures for external latch-up investigations

The basic layout of the test structures is shown in Figure 3.4 and covers a latch-up detector (SCR structure), varying number of guard-rings and a carrier injector. The arrangement is varied with different injector distances and SCR orientations (see Figure 3.1).

Two variants which represent extreme cases of layout are described in detail. For cases having the latch-up detector structure placed in larger distances from the injector, a *large* test structure is chosen which has a second n^+ guard-ring and a third n^+ guard-ring, each 2 µm wide. The distance between the second and third n^+ guard-ring is 40 µm (see Figure 3.4). The second described layout variant has the latch-up detector structure placed next to the injector. It is represented by the *small* latch-up test structure which has the injector n^+ diffusion separated only by a first p^+ guard-ring and a second n^+ guard-ring, both 0.24 µm wide (see Figure 3.5).

For negative injection current (injection of electrons), a 120 µm wide grounded gate (gg) NMOS ESD protection device is used as carrier injector structure [45]. The four n^+ drain diffusion fingers of the ggNMOS transistor are connected to the injection pad.

The injector structure for positive current (injection of holes) is shown in Figure 3.5 and consists of an n well diode, where the anode (p^+ diffusion) is connected to the injection pad and the cathode to VDD. To collect the injected carriers n^+ and p^+ guard-rings (stripes) are placed as latch-up protection between carrier injector and latch-up detector structure.

The schematic cross section of the test structure for negative injection pulses is shown in Figure 3.6a. It shows on the left the latch-up detector structure with the parasitic *pnp*

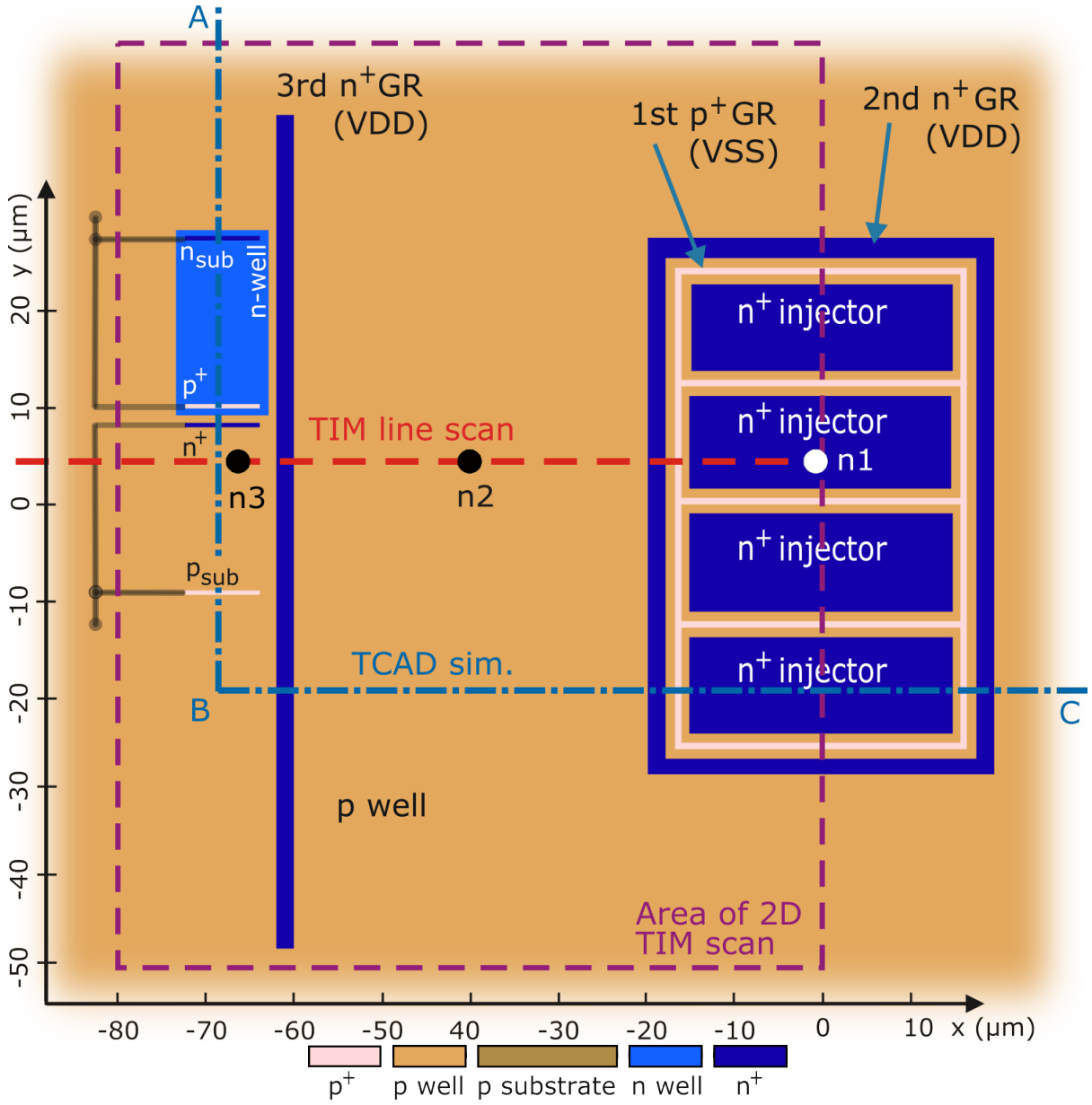


Figure 3.4: Top view of the investigated *large* latch-up test structure. From left to right: latch-up detector structure (SCR), n^+ guard-ring, injector with surrounding first p^+ and second n^+ guard-ring (width is 2 µm). The points n_1–n_3 correspond to $x = 0$, -40 µm and -66 µm. The dashed-dotted line marks the cross sections A–B B–C for the 2D TCAD simulations. The dashed line indicates the linear TIM scan and the dashed rectangle marks the area of the 2D TIM scans.

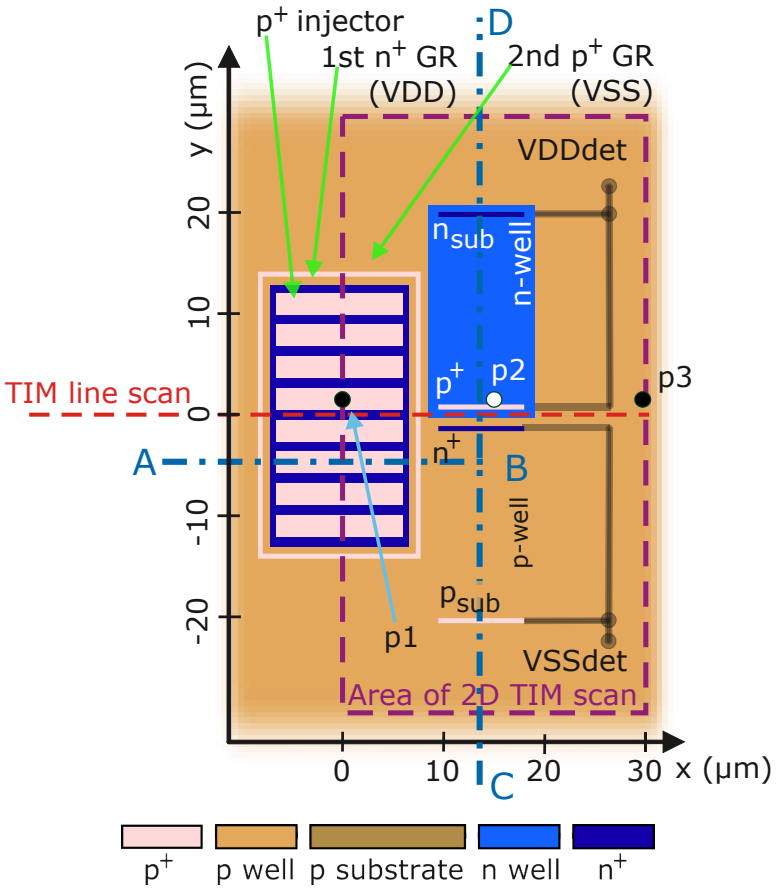


Figure 3.5: Top view of the investigated *small* latch-up test structure for positive injection pulses. From left to right: p injector (n well diode) with surrounding first n^+ and second p^+ guard-ring (width is 0.24 µm) and latch-up detector structure (SCR). The points p_1–p_3 correspond to $x = 0$, 15 µm and 30 µm. The dashed-dotted line marks the cross sections A–B B–D for the 2D TCAD simulations. The dashed rectangle indicates the 2D TIM scan area.

transistor (Q_1) and *npn* transistor (Q_2) and their corresponding base resistances (R_1 and R_2), third and second n^+ guard-ring, p^+ guard-ring, the injecting n^+ diffusion followed by p^+ and n^+ guard-rings. The injecting n^+ diffusion (emitter) forms with the grounded p well (first guard-ring, base) and biased n well (second guard-ring, acting as collector) an intrinsic *npn* transistor (Q_3).

The cross section of the test structure for positive injection pulses is shown in Figure 3.6b. It shows (reverse arranged) on the left the p^+ and n^+ guard-rings followed by the injecting p^+ diffusion, n^+ and p^+ guard-rings and the latch-up detector structure (Q_2, Q_1, R_2 and R_1). The injecting p^+ diffusion forms with the biased n well (first guard-ring) and grounded p well (second guard-ring) an intrinsic *pnp* transistor (Q_3).

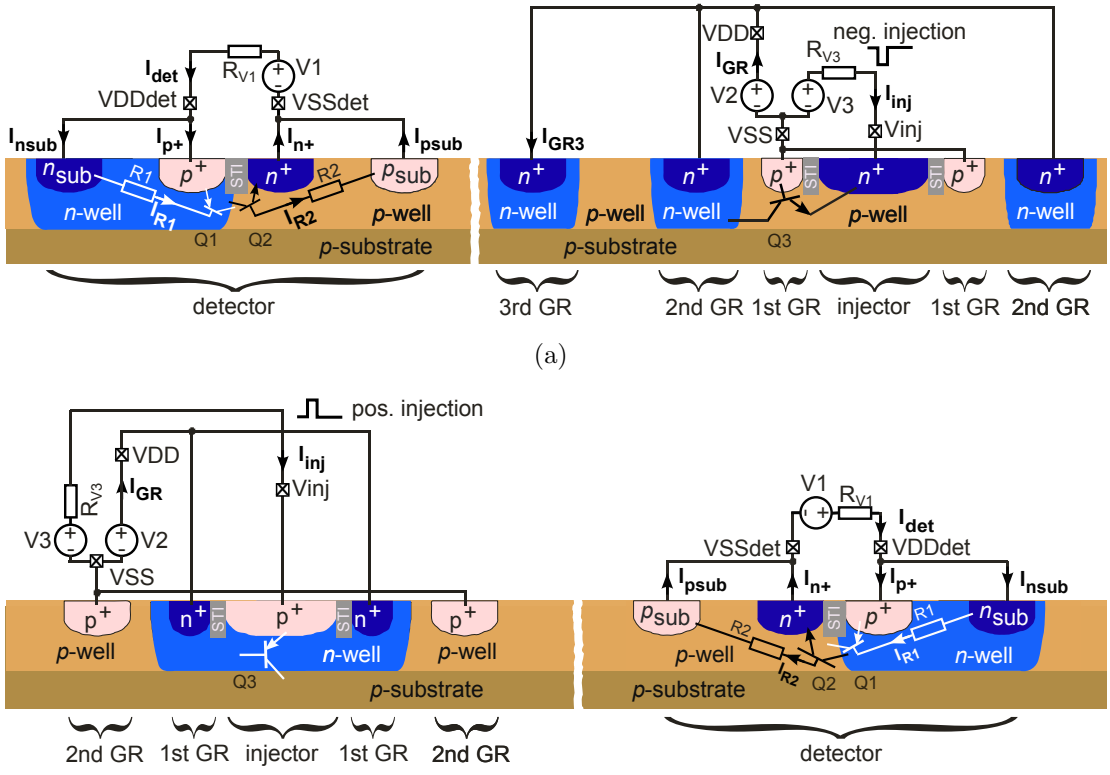
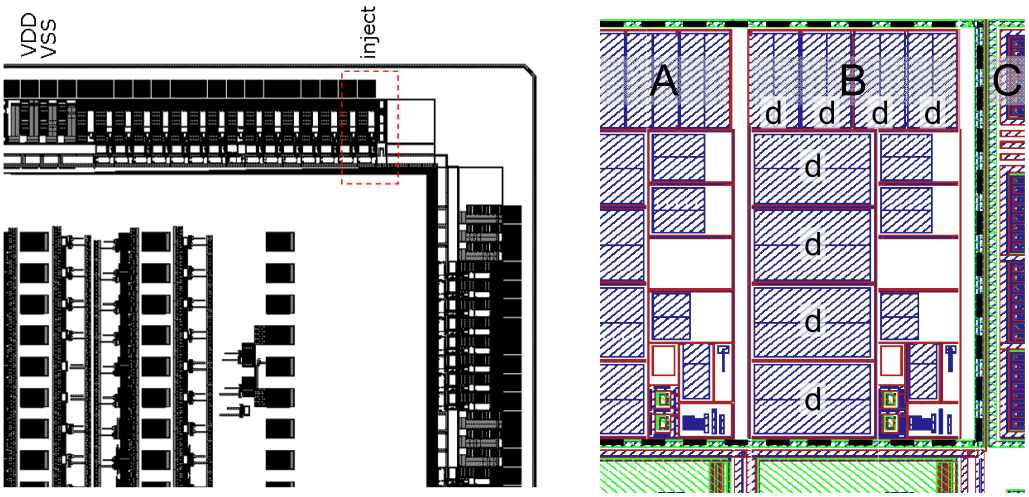


Figure 3.6: Schematic cross sections of the measured external latch-up test structures implemented in dual well technology [4]. Test structures are designed for (a) negative and (b) positive injection current. The cross sections are along A–B B–C in Figure 3.4 and A–B C–D in Figure 3.5.

Commercial I/O cells

Commercial I/O cells placed in an I/O pad frame are investigated. For these investigations a test chip without connected core logic is used (see Figure 3.7a).



(a) (b)

Figure 3.7: Top view of I/O cell test structures [105]. (a) I/O pad frame with investigated I/O cell ("inject"). (b) Investigated I/O cell "B" with neighboring cells "A" and "C". The thick dashed line (black) marks the surrounding n^+ guard-rings. The /// hatch pattern (blue) marks n^+ diffusions "d" at I/O pad (NMOS, ESD), *VSS* or *VDD*. The \\\ hatch pattern (green) marks n wells at *VDD* (n^+ guard-rings, n wells for PMOS transistors). The thin lines (red) mark p^+ guard-rings at *VSS*. The free area is p well.

Exemplarily, the top view of an injecting I/O cell "B" and its neighboring cells "A" and "C" is shown in Figure 3.7b [105]. The n^+ drain (or source) diffusions of blocked NMOS transistors and ESD structures are connected to the bond pad of the I/O cell (see "d"). The corresponding n^+ source (drain) diffusions are connected to *VSS* (*VDD*)[3]. Black dashed lines mark the n^+ guard-rings placed at top, bottom and right side. Other investigated I/O cells are presented in [106].

3.1.2 Experimental details and setup customization

Since there was no commercial transient latch-up test system for TIM scans available, the hardware and software of the scanning TIM setup are adapted to allow experiments with two power supply domains and application of short pulses for carrier injection.

[3] *Infineon Technologies AG* prohibited a more detailed publication of this I/O cell architecture.

Hardware

A transient latch-up setup, based on the experiments of *K. Domański* [4], is combined with the scanning TIM setup. The schematic diagram of the combined latch-up test system is shown in Figure 3.8. The automated setup provides possibility for recording voltage and current transients under transient latch-up as well as linear and two-dimensional scans from the device backside with the optical probing beam.

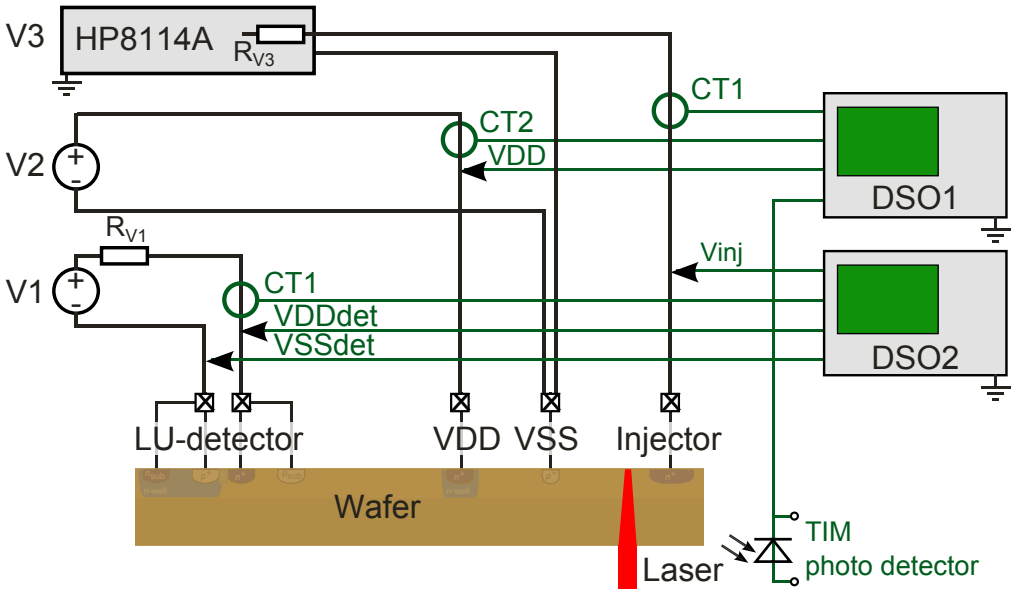


Figure 3.8: Schematic diagram of the combined transient latch-up and TIM system. The floating voltage source V_1 realizes a second supply domain for the latch-up detector (SCR).

For negative current injection, a solid-state pulse generator (*Agilent HP8114A*, 50 Ω output impedance) is connected to an n^+ diffusion and the transient latch-up pulse is generated by forward biasing a n^+/p well diode. The injection pulses can be varied in pulse width, polarity and amplitude (absolute value of output voltage). The slew rate is approximately 1 V/ns. One floating DC source (V_1) serves for the latch-up detector (SCR) supply domain (VDD_{det}) and one (V_2) as guard-ring supply (VDD). A current limiting series resistor ($R_{V1} = 33\,\Omega$) is introduced to avoid damage to the test structures during latch-up. Latch-up triggering is identified by monitoring the current flow through the latch-up detector structure after the end of the trigger pulse. The currents are measured using *Tektronix CT1* and *CT2* current transducers. For details of the transient latch-up setup is referred to [45–47].

For positive injection currents the transient latch-up setup is reconfigured for applying positive currents to a p^+/n well diode, the first n^+ guard-ring is attached to VDD, the

second and optionally the third p^+ guard-rings are connected to *VSS* (see Figure 3.6b).

Automation software

The *Labview* [107] control software *heterodyne.vi* [108] for the scanning TIM setup is enhanced for the use with two four-channel oscilloscopes. Latch-up is identified with cursor readouts and cleared by setting the bias voltages to zero.

TCAD Simulation

To provide also insight into the behavior in the third dimension (depth) of the structures, the experimental results are complemented with two-dimensional TCAD simulations of doping profiles, which were performed by *K. Domański* using the *Synopsis (medici)* tool *DESSIS* [90] at *Infineon Technologies AG* [4]. The phase shift was simulated by *DESSIS* postprocessor called *APEX*.

3.1.3 Investigation of negative carrier injection at test structures

Transient or static latch-up could originate from negative substrate currents (electrons, minority carriers), which are injected from n diffusions into p substrate. The influence of injection pulse amplitude, width, guard-ring bias and circuit topology on latch-up sensitivity is investigated for negative substrate currents. Electrons are injected by pulsing the injector (*Vinj*) pad (n^+) negative with respect to the *VSS* pad (p^+ guard-ring). The schematic cross section of the investigated structure is shown in Figure 3.6a. The n^+ guard-rings (*VDD* pad) are biased with 3 V. The latch-up detector supply domain (VDD_{det} and VSS_{det} pads) is biased with a floating 3 V DC source. The connections of the instruments to the latch-up test structure are shown in Figure 3.8. All experiments are performed at room temperature. The TIM method is used to trace the propagation of injected carriers in the substrate of the latch-up test structures.

Latch-up identification

The current and voltage transients for a −600 mA injection pulse of 1500 ns duration in a *large* test structure are shown in Figure 3.9. The used *Tektronix CT1* current transducer causes the slightly rising slope (“1”) of the actually square injection pulse.

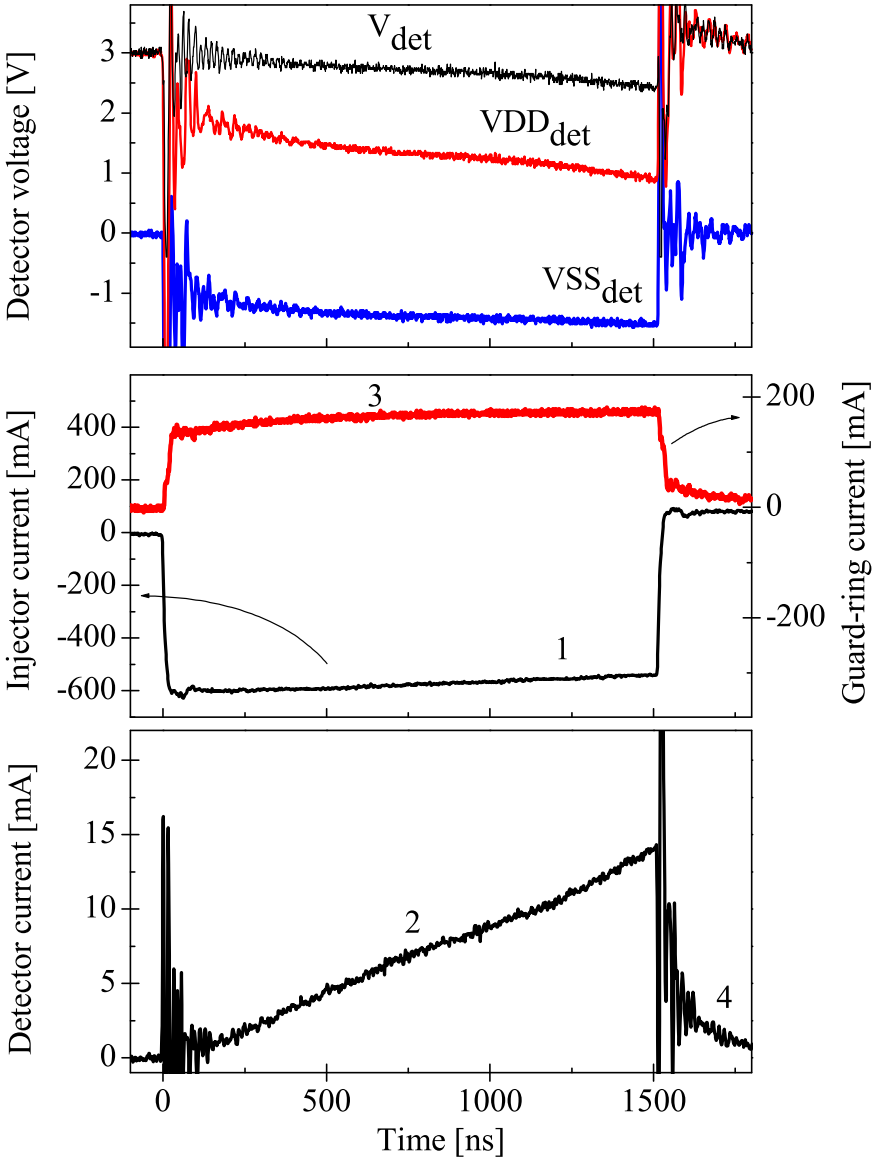


Figure 3.9: Electrical measurements on the terminals of the *large* latch-up test structure during injection of −600 mA. The current flow at the latch-up detector stops after the injection pulse, indicating no latch-up of the detector structure.

During the 1500 ns injection pulse, the currents at latch-up detector ("2") and guard-rings ("3") are continuously rising due to increasing concentration of carriers in substrate and consequently at the detector area (more on that later). The injected current causes a negative shift of the detector potentials VDD_{det} and VSS_{det}. The detector current flow stops after the 1500 ns injection pulse, indicating no latch-up of the detector structure ("4").

Figure 3.10 shows the comparison of the detector current transients of a non latching injection pulse (−600 mA) and a latching injection pulse (−650 mA). After the −600 mA injection pulse the detector current flow stops ("1"), indicating no latch-up of the detector structure. For the higher injection amplitude[4] (higher absolute value of current pulse), the parasitic SCR structure latches *during* the injection pulse (at $t = 1400$ ns). The latch-up event is visible as abrupt increase of detector current ("2"). In the latched state current flows self-sustaining through the detector structure – also after termination of the injection pulse (see detector current for −650 mA and $t > 1500$ ns, "3").

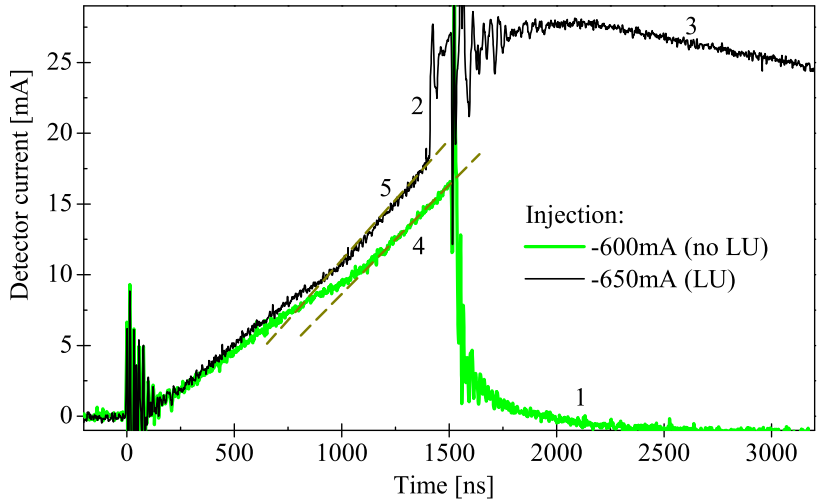


Figure 3.10: Detector current on the *large* latch-up test structure during injection of −600 mA ("1") and −650 mA ("3"). The abrupt increase of the detector current ("2") indicates latch-up of the detector structure.

The continuously rising detector current during the injection pulse could be explained[5] with a simplified flow of some representative electrons (⊖) and holes (⊞) in the top view of the test structure in Figure 3.11. The real density of majority carriers is several decades above the minority carrier concentration – see sketched carrier concentration for p substrate and n well in Figure 1.15.

[4] The circuit is most sensitive at the terminating edge of the injection pulse.
[5] This anticipated explanation is supported by subsequent measurement results and *SPICE* simulations.

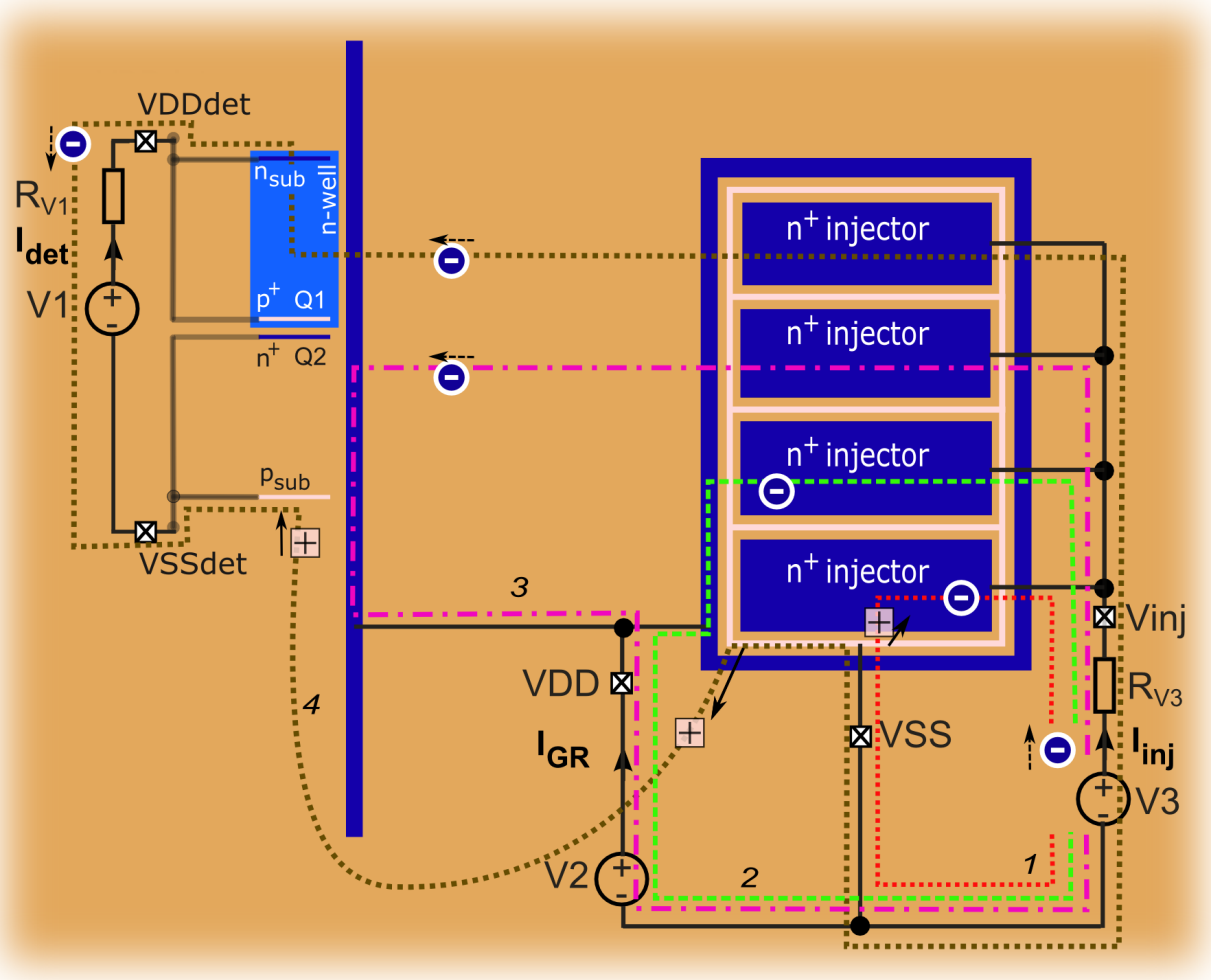


Figure 3.11: Simplified current flow in top view of the *large* test structure. Loop *1* shows (negative) charge flowing from pulse generator to injector, first guard-ring (p^+), *VSS* and back to pulse generator. Loop *2* shows charge flowing from injector to second guard-ring (n^+), guard-ring supply and back to pulse generator. Loop *3* is analogous, but with third guard-ring. Loop *4* shows charge flowing from injector to detector *n* well, detector supply V_1, *p* well, *VSS* and back to pulse generator.

Starting with slight negative injection, the pulse generator (V_3) injects electrons at *Vinj* pad and "takes" same amount of electrons from *VSS* pad[6] (see dotted loop "1"). This results in injected electrons at the n^+ diffusion and injected holes at the p^+ diffusion of the injector structure. The current flow within the schematic cross section (with rotated latch-up detector) is shown in Figure 3.12.

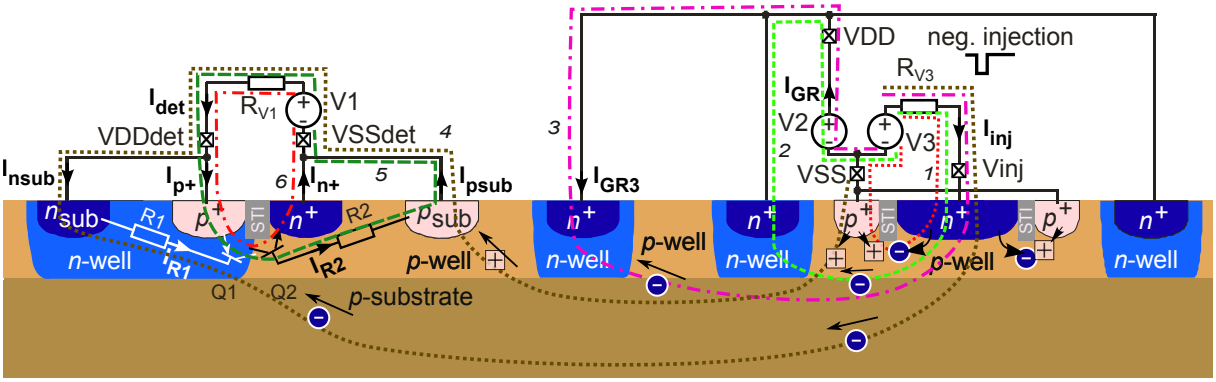


Figure 3.12: Schematic current flow during negative injection. Loop *1* shows (negative) charge flowing from pulse generator (V_3) to injector, first guard-ring (p^+), *VSS* and back to pulse generator. Loop *2* shows charge flowing from injector to second guard-ring (n^+), guard-ring supply (V_2) and back to pulse generator. Loop *3* is analogous, but with third guard-ring. Loop *4* shows charge flowing from injector to detector *n* well, detector supply V_1, *p* well, *VSS* and back to pulse generator.

For increasing current amplitude some electrons reach the second (n^+) guard-ring (see dashed loop "2"). The electrons move to *VDD* pad, guard-ring supply (V_2) and back to pulse generator (V_3). Next higher injection level is analogous, but with third guard-ring (see dash-dot loop "3").

A part of injected electrons diffuse deeper into substrate. Electrons which reach the detector *n* well (dotted loop "4") are collected by the detector supply V_1. This gives the dominant contribution to the measured detector current I_{det} for slight injection currents. Electrons move from detector supply V_1 to p_{sub} contact and recombine with holes[7]. This results in a hole flow in the extended *p* well towards the p_{sub} contact of the detector structure. This hole current flow is not visible in the TIM scans, because heating is negligible and *drift current* does not change the carrier concentration ($\Delta N = 0$) and so $\Delta\varphi_{\text{fc}}(t) = 0$. The holes are supplied from the p^+ diffusions of the injector, where they are generated[8].

[6] Charge conservation for pulse generator V_3. The guard-ring current is neglected for very slight injection.
[7] Charge conservation for detector supply V_1.
[8] Pulse generator "receives" electrons from *VSS* pad and guard-ring supply V_2.

If the electron current to the detector n well (across R_1) is high enough (voltage drop in the detector n well around $-0.6\,\mathrm{V}$), the *pnp* transistor Q_1 will be activated and current flows through the detector structure (dotted loop "5" in Figure 3.12). This gives an additional contribution to the total detector current (see increased slope of the detector current transients "4" and "5" in Figure 3.10). This means, a certain current at the detector supply V_1 is measured – but not same amount of current is flowing *through* the *pnpn* junction of the SCR structure (Q_1 and Q_2).

If the resulting hole current through the p well (R_2) causes a voltage drop around 0.6 V, the *npn* transistor Q_2 will be activated as well and the parasitic SCR structure will be triggered. This results in an abrupt increase of the total detector current (see "2" in Figure 3.10). Now both bipolar transistors are active and self-sustaining current flows through the latch-up detector (see loop "6" in Figure 3.12). The activation of transistor Q_2 keeps transistor Q_1 active and transistor Q_1 keeps transistor Q_2 active – latch-up occurs.

SPICE modeling of *large* latch-up test structure under negative injection

The different slopes of the detector current transients and the activation of transistors Q_1 and Q_2 are reproduced with *SPICE* simulations [17] of the simplified circuit diagram for the large latch-up test structure shown in Figure 3.13. The simulations give insight into the currents at the n_{sub}, p^+, n^+ and p_{sub} diffusions of the detector structure, which could not be measured explicitly at the test structures because the diffusions are connected at wafer-level to just two bond pads (VSS_{det} and VDD_{det}). For more detailed analysis elaborate three-dimensional TCAD simulations would be necessary[9]. The discrete components are chosen to fit the experiment as simple as possible. Real values (resistances, current gain etc.) differ and depend on doping concentrations, spacing etc.

The increasing carrier density in substrate is approximated with increasing amplitude of a time-dependent exponential current source[10] (I_{snw}), which is connected to the n well of the detector structure (R_1). The detector structure is modeled with resistors R_1 and R_2 (103 Ω), transistors Q_1 and Q_2 and voltage supply V_1 with series resistor R_{V1}. The resistors R_5 and R_6 represent parasitic resistances (4 Ω). The adapted transistor model parameters (modified *2N3906* and *2N3904* transistors) are shown in Listing 3.1. Diode $\mathrm{D}_{\mathrm{sn+}}$ (*1N4148* diode) represent the p substrate / n^+ junction and the resistors R_3 and R_4

[9] Test structures, where the wells of the detector structure are facing to the injector, cannot be reproduced satisfactory with two-dimensional TCAD simulations.

[10] The substrate current is turned off by switch S_1 in combination with voltage source V_2.

represent distributed substrate resistances of the *large* latch-up test structure.

Starting with low injection amplitudes the negative current of the current source I_{snw} flows to the detector n well, R_1, n_{sub} contact (I_{nsub}), detector supply V_1, p_{sub} contact (I_{psub}), R_6, R_4 and back to the current source (see dotted line "4" in Figure 3.13). The simulated current and voltage transients under a 1500 ns current pulse in Figure 3.14 show that this is the dominant contribution to the total detector current for low injection amplitudes (see "1").

With increasing injection amplitude the voltage drop at R_1 increases and the base / emitter voltage (V_{BEQ1}) of the *pnp* transistor Q_1 decreases. If this base / emitter junction is forward biased, additional current ($I_{\mathrm{p+}}$) flows at detector supply and a steeper slope ("2") appears at the detector current transient. If the resulting voltage drop at R_2 is high enough, the *npn* transistor Q_2 gets active as well and high current flows at the n^+ contact ($I_{\mathrm{n+}}$), too (see "3"). This results in an abrupt increase of the total detector current ("4"). Now both bipolar transistors are active and self-sustaining current flows through the detector structure.

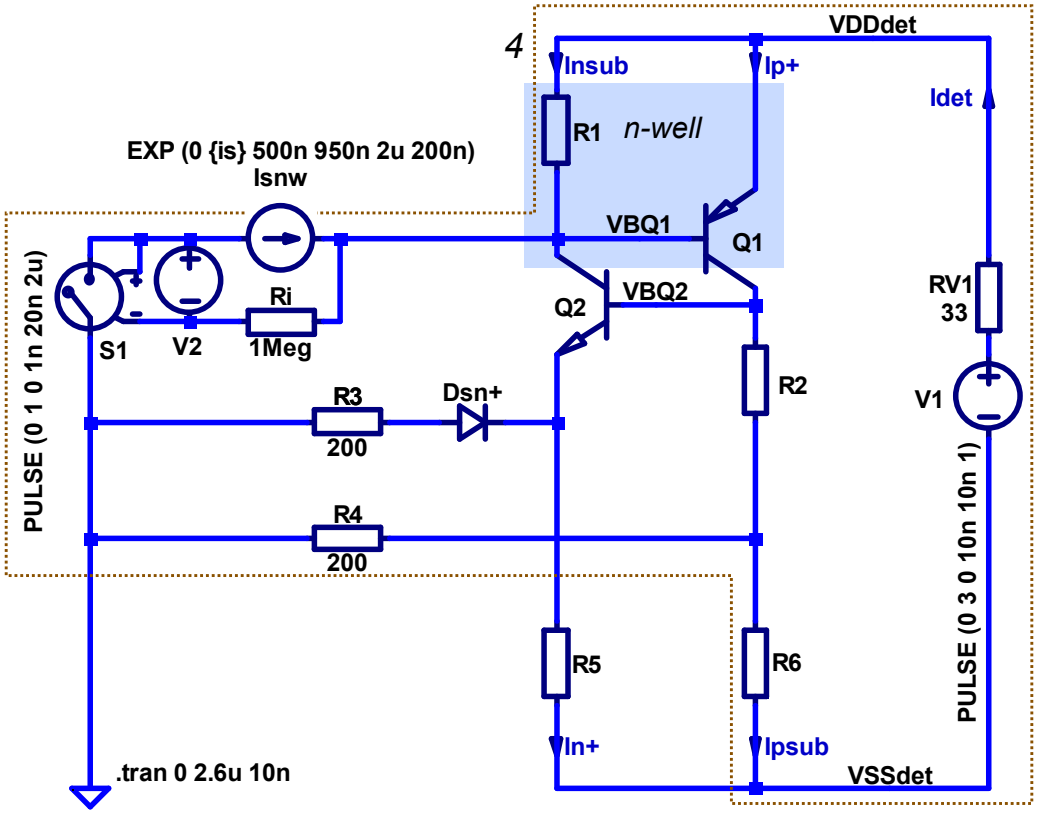


Figure 3.13: Simplified circuit diagram for *SPICE* simulation of the internal detector currents. The increasing carrier density in substrate is approximated with an increasing amplitude of a time-dependent exponential current source (I_{snw}).

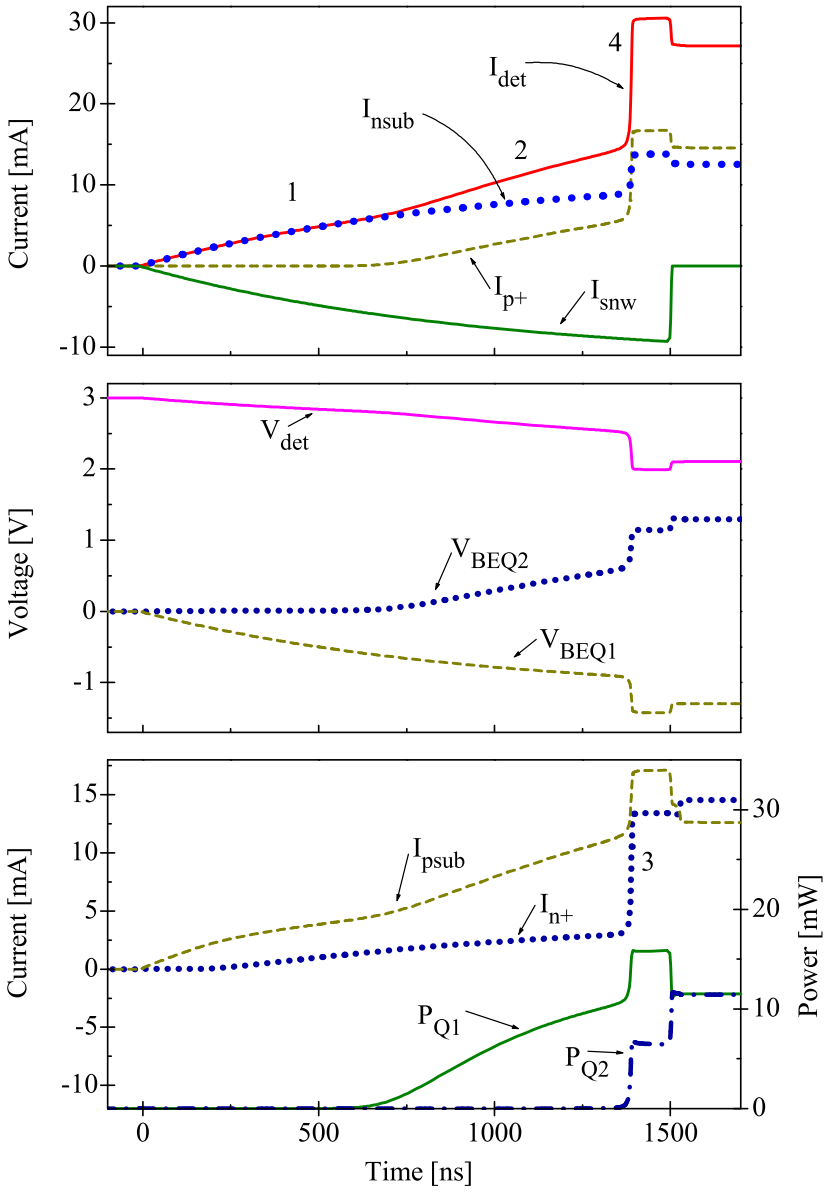


Figure 3.14: *SPICE* simulation of detector structure showing internal voltages and currents under a negative current pulse. After activation of transistor Q_1 transistor Q_2 gets active and latch-up occurs at $t = 1400\,\text{ns}$. Used amplitude parameter: ".param $is - 11.7\,\text{mA}$".

```
1 .model Q1 PNP (IS=1e-14 VAF=100 BF=50 ikf=0.4 xtb=1.5 BR=4
2 CJC=4e-12 cje=8e-12 rb=11 rc=11 re=38 TR=2.5e-9 tf=350e-12 itf=1
3 vtf=2 xtf=3 vceo=40 icrating=200m mfg=ifx)
4
5 .model Q2 NPN (IS=1e-14 VAF=100 BF=50 ikf=0.4 xtb=1.5 BR=4
6 CJC=4e-12 cje=8e-12 rb=11 rc=11 re=38 TR=2.5e-9 tf=350e-12 itf=1
7 vtf=2 xtf=3 vceo=40 icrating=200m mfg=ifx)
```

Listing 3.1: *SPICE* transistor models for the detector structure.

The simulations of the total transistor power (P_{Q1}, P_{Q2}) show that transistor Q_1 stays inactive for detector currents below ∼6 mA[11]. The amplitude parameter ".param *is* −2.5 mA" corresponds to the detector current caused by −200 mA injection. For the simulation slightly below latch-up, the parameter ".param *is* − 11 mA" is used and for latch-up ".param *is* − 11.7 mA" is used.

Trigger current characteristics for negative injection

The effect of the pulse width of the *external* injection source on the latch-up trigger current is investigated for *small* and *large* latch-up test structures. The latch-up trigger current is defined as the minimum amplitude of the external injection pulse, which is required to trigger latch-up in the detector structure[12].

The experimentally obtained latch-up trigger currents are summarized in Figures 3.15a and 3.15b for various injection pulse durations. The increase of pulse width results in a higher sensitivity for latch-up (lower amplitude of injection current triggers latch-up). In *small* test structures the latch-up trigger current shows a kink for pulses longer than approximately 300 ns. In contrast, the *large* test structures show stabilization of the trigger current level for pulses longer than ∼10 µs (see "A" and "B").

Excess carrier and heat spreading during negative injection

In order to focus on carriers originating from the injector – and not from the latched state of the detector structure (SCR) – most investigations are performed below latch-up condition. Negative injection pulses with 1500 ns duration and 200 mA amplitude (twice

[11] This explains, why in the later experiments no heating at the center of the detector structure is observed in *large* test structures for −200 mA injection, where the detector current stays even below 3 mA.

[12] Do not mix up with detector current at the trigger point of the SCR.

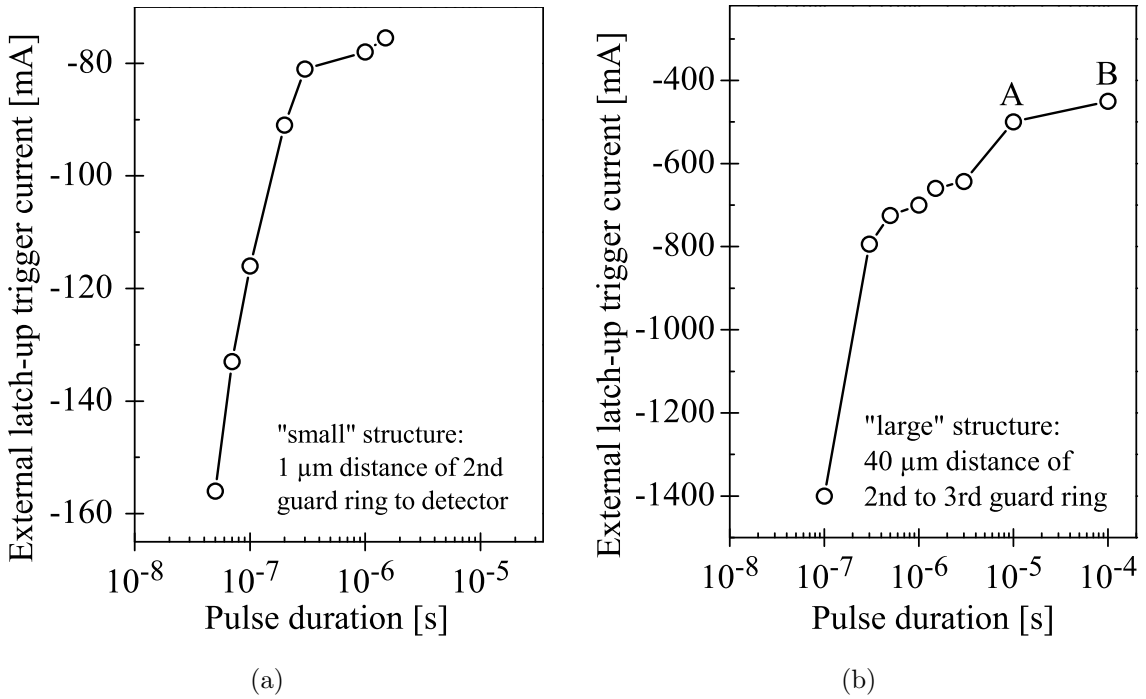


Figure 3.15: Effect of injection pulse duration on latch-up trigger current for the investigated test structures: (a) *small* (b) *large* test structure.

the JEDEC trigger current value [32]) are applied on *large* latch-up test structures. The current density at the 120 µm wide junction is $-1.66\,\mathrm{mA}/\mu\mathrm{m}$ and corresponds to the TCAD simulations of *K. Domański* [109]. The current and voltage transients for such a non-latching pulse are shown in Figure 3.16.

The TIM phase shift transient ($\Delta\varphi$) measured in the middle of the injector (at point n_1 in Figure 3.4) is shown in Figure 3.17. The phase shift is composed of a fast falling excess carrier component and a slowly rising thermal component. The phase shift $\Delta\varphi$ shows negative phase shift (dominant free carrier contribution) for $t < 1300\,\mathrm{ns}$. The thermal contribution increases with time and dominates later ($t > 1300\,\mathrm{ns}$) the total phase shift. The fast rising phase shift after the terminating edge of the injection pulse is caused by termination of carrier injection and recombination of carriers. Accordingly the negative free carrier contribution disappears. The decomposed thermal contribution $\Delta\varphi_{\mathrm{th}}$ and the free carrier contribution $\Delta\varphi_{\mathrm{fc}}$ are also sketched in Figure 3.17. The thermal contribution is assumed with a piecewise linear evolution. The free carrier contribution is calculated as difference of the total phase shift and the assumed thermal contribution ($\Delta\varphi_{\mathrm{fc}} = \Delta\varphi - \Delta\varphi_{\mathrm{th}}$).

At the position between second and third guard-ring (at point n_2 in Figure 3.4) a slower

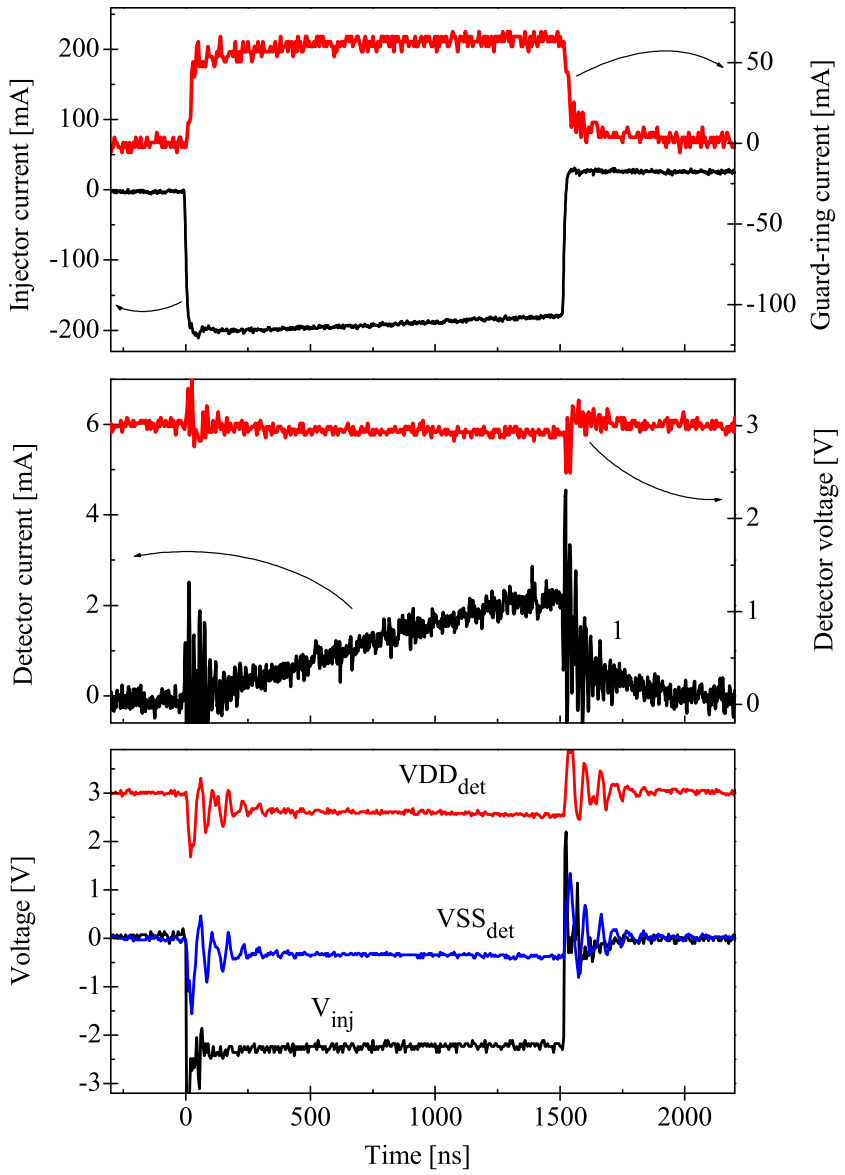


Figure 3.16: Electrical measurements on the terminals of the *large* latch-up test structure during injection of −200 mA. The current flow at the latch-up detector stops after the injection pulse, indicating no latch-up of the detector structure. The used *Tektronix CT1* current transducer causes the slightly rising slope of the actually square injection pulse.

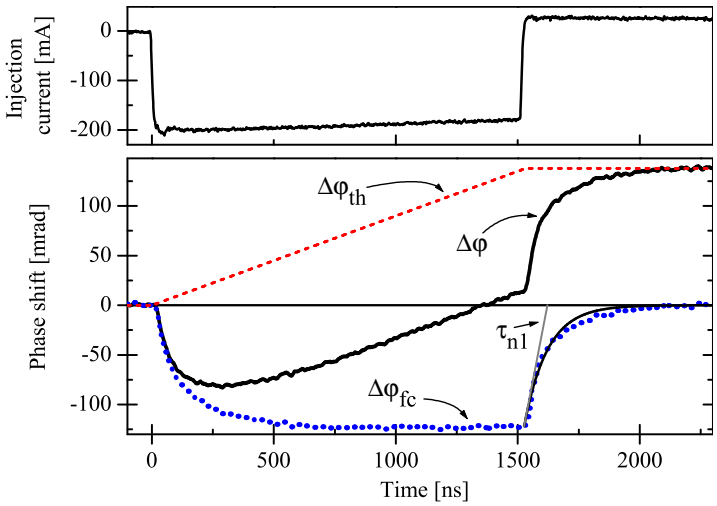


Figure 3.17: Decomposed phase shift components at the center of the injector (point n_1 in Figure 3.4) for $-200\,\mathrm{mA}$ injection. The measured phase shift $\Delta\varphi$ is composed of a thermal contribution $\Delta\varphi_{\mathrm{th}}$ and a (negative) excess carrier contribution $\Delta\varphi_{\mathrm{fc}}$. The dashed line shows schematically the assumed evolution of the thermal component. The dotted line represents the excess carrier contribution $\Delta\varphi_{\mathrm{fc}}$ as difference of the total phase shift and the assumed thermal contribution. Effective minority carrier lifetime $\tau_{\mathrm{n1}} \simeq 94\,\mathrm{ns}$ – see fitting line and tangent at the terminating edge.

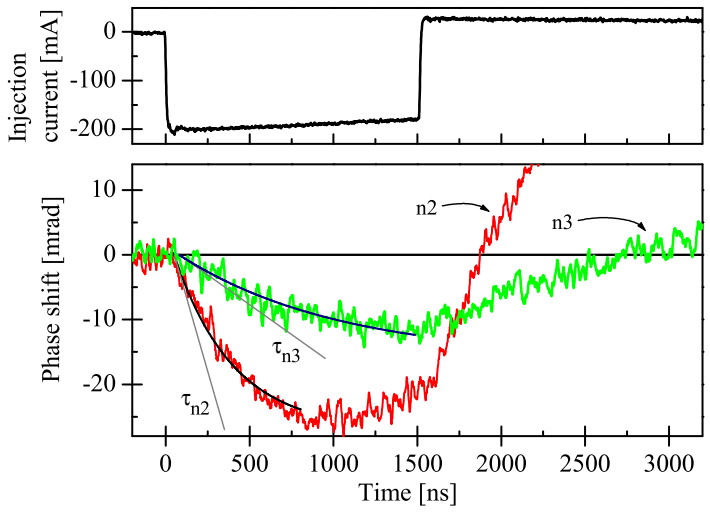


Figure 3.18: Phase shift measurements on the *large* latch-up test structure during negative injection at $-200\,\mathrm{mA}$. The phase shift transients n_2 and n_3 are taken from the corresponding points in Figure 3.4. Effective minority carrier lifetime $\tau_{\mathrm{n2}} \simeq 350\,\mathrm{ns}$ and $\tau_{\mathrm{n3}} \simeq 950\,\mathrm{ns}$ (see fitting lines and tangents).

saturation effect of the excess carrier contribution (negative phase shift) is observed (see curve n_2 in Figure 3.18). Curve n_3 shows the measured phase shift transient at the detector structure (point n_3 in Figure 3.4). It shows negative phase shift (excess carriers) up to 1.2 µs *after* termination of the injection pulse. This is consistent with the observed slow decrease of detector current after the injection (see "1" in Figure 3.16).

The minority carrier lifetime can be estimated from the phase shift transients. After the terminating edge of the injection pulse excess carriers decay exponentially ($e^{-t/\tau}$) with time constant (effective lifetime) τ. The phase shift $\Delta\varphi(t)$ (excess carrier contribution) after the terminating edge in Figure 3.17 is approximated with Equation (3.1) – see thin fitting line. This results in a minority carrier (electron) lifetime in the injector region of $\tau_{n1} \simeq 94\,\text{ns}$.

$$\Delta\varphi(t) = A\,e^{-\frac{t-t_1}{\tau_{n1}}} \quad \Big| \; _{t \geq t_1} \tag{3.1}$$

This value matches well to the electrical experiments of *K. Domański*, who observed an electron lifetime of $\tau_n \simeq 100\,\text{ns}$ in the base of the parasitic *npn* transistor [4].

At regions far from the injector slow heat diffusion is superposed, therefore the leading edge – where heating is still negligible – is taken for estimation of the minority carrier lifetime. This phase shift decay is modeled as

$$\Delta\varphi(t) = A(1 - e^{-\frac{t}{\tau}}). \tag{3.2}$$

This gives for position n_2 a minority carrier lifetime of $\tau_{n2} \simeq 350\,\text{ns}$ with the fitting coefficient $A = -27\,\text{mrad}$ (see thin fitting curve at line n_2 in Figure 3.18). The fitting curve at line n_3 implies a minority carrier lifetime of $\tau_{n3} \simeq 950\,\text{ns}$ and a fitting coefficient of $A = -16\,\text{mrad}$. This reflects a short effective minority carrier lifetime for near regions τ_{n2} due to high recombination rate (high doping concentration, nearby substrate contacts and guard-ring effects) and a long effective minority carrier lifetime for far regions τ_{n3} due to the low substrate doping concentration.

The phase shift measurement across the structure (along the dashed line in Figure 3.4) is shown in Figure 3.19 for several instants during injection. The lowest phase shift (highest excess carrier concentration) is observed at $t = 300\,\text{ns}$ at the center of the injector ($x = 0$). The phase shifts at first (GR1) and second (GR2) guard-rings increase due to heating (power dissipation). Outside the second guard-ring decrease of phase shift corresponds to increase of excess carrier concentration in substrate. High density of excess carriers (negative phase shift) is observed between second (GR2) and third (GR3) guard-ring. This indicates that guard-rings are not fully efficient and injected carriers diffuse below

them – see loop *3* and *4* in Figure 3.12.

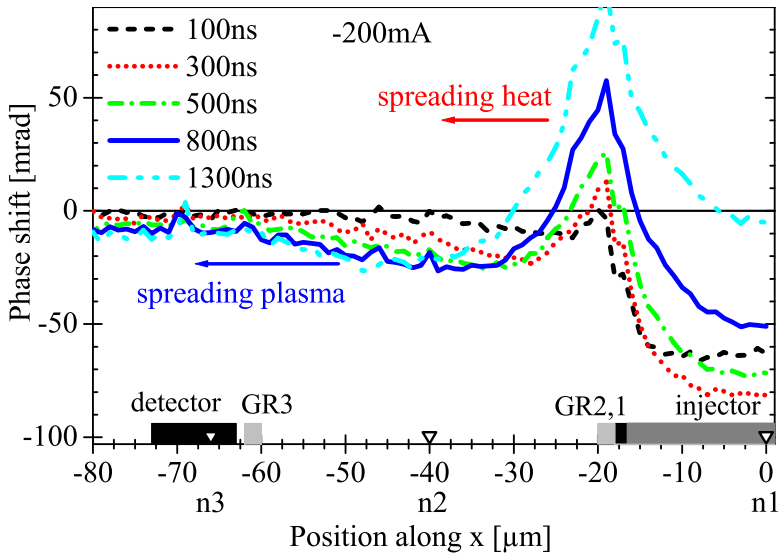


Figure 3.19: TIM scan at five instants of a −200 mA injection pulse on the *large* test structure. The scan is performed across the structure (along the dashed line in Figure 3.4). Decrease of phase shift during injection corresponds to increase of excess carrier density. Increasing phase shift indicates spreading of heat. The locations of the points n_1 – n_3 are marked with triangles.

Figure 3.20 shows phase shift snapshots of two-dimensional TIM scans at instants during (a–c) and after (d) the injection pulse. They show a laterally spreading front of excess carriers (negative phase shift) and a slower spreading heat front (positive phase shift) as partial top view. The scanned area is marked with the dashed rectangle in Figure 3.4.

Heat diffusion slowly increases the junction temperature of the 43 µm distant SCR and lowers its trigger current level [46]. The schematic heat diffusion in silicon for 3 µs (diffusion length ∼17 µm) and 10 µs (diffusion length ∼31 µm) pulses is sketched using Equation (1.4) in Figure 3.21. The increase of the junction temperature (see "1" in Figure 3.21) explains the significantly weaker trigger current of 10 µs ("A") and 100 µs ("B") pulses in Figure 3.15b.

Phase shift slightly below latch-up condition. Phase shift measurements during latch-up would be already influenced by additional carriers injected from the activated SCR[13]. Therefore, the phase shift is measured at −600 mA (slightly below latch-up condition) at the *large* latch-up test structure. In the detector region the phase shift decreases to roughly −20 mrad (see Figure 3.22). This is the latch-up critical phase shift for worst-

[13] The effect of the additional carriers from the SCR will be discussed in Section 3.1.4.

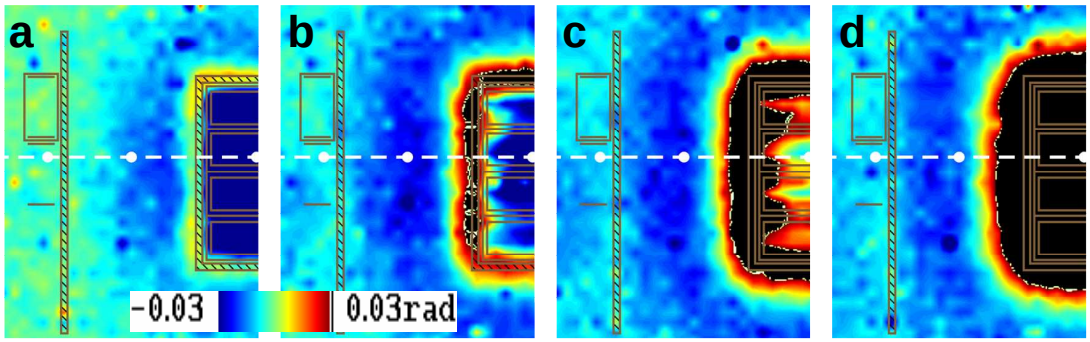


Figure 3.20: Two-dimensional TIM phase shift scan (interpolated, top view, see Figure 3.4 for labels) of the *large* test structure at (a) $t = 300\,\text{ns}$, (b) $t = 800\,\text{ns}$, (c) $t = 1300\,\text{ns}$, (d) $t = 1600\,\text{ns}$ (100 ns after the end of pulse) of a 1500 ns long injection pulse. The white dots indicate the points n_1–n_3 of the phase shift measurements in Figures 3.17 and 3.18. Black color indicates phase shift exceeding +30 mrad.

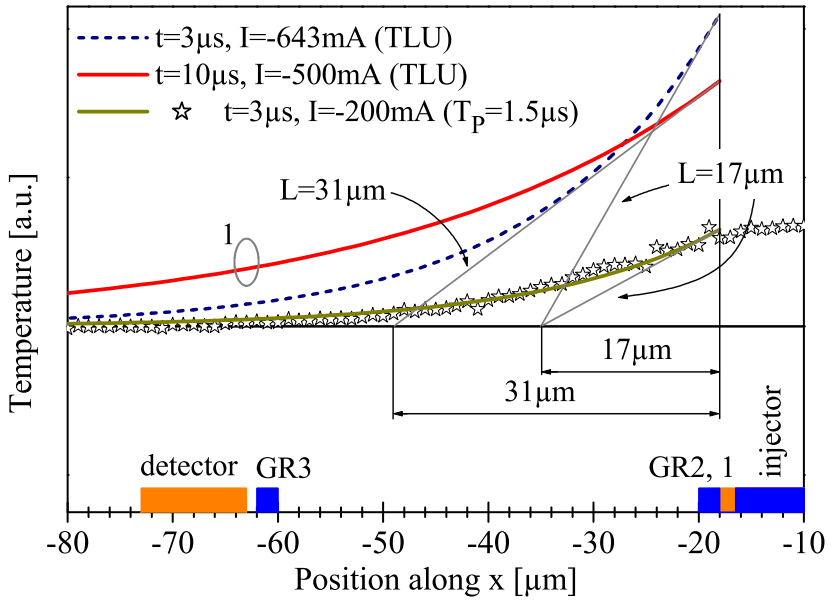


Figure 3.21: Schematic heat diffusion for 3 µs (diffusion length $L \simeq 17\,\mu\text{m}$) and 10 µs (diffusion length $L \simeq 31\,\mu\text{m}$) pulses. Symbols represent measured phase shift data at 3 µs and −200 mA (below latch-up condition).

case SCR structures in this 90 nm CMOS technology – any lower phase shift (higher excess carrier concentration) might cause latch-up.

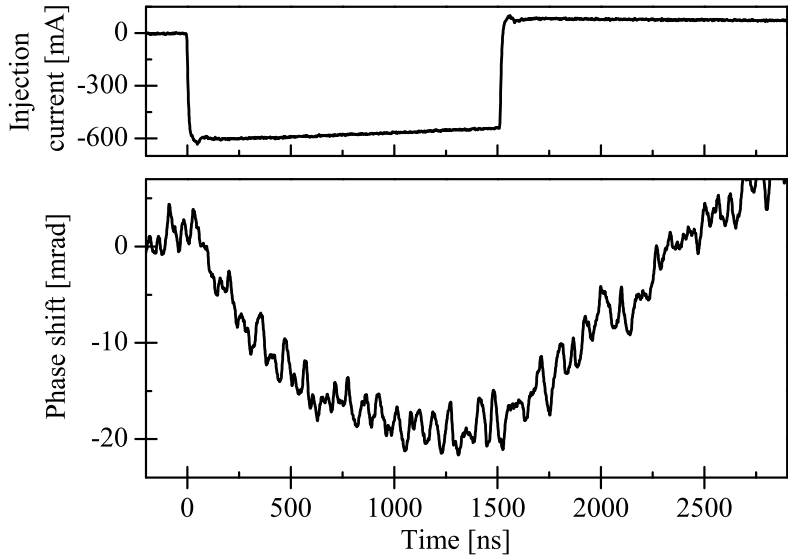


Figure 3.22: Phase shift measurement at the detector structure of the *large* latch-up test structure during negative injection close to latch-up (−600 mA) showing as latch-up critical phase shift roughly −20 mrad.

Effect of guard-rings on carrier spreading

The effect of 3 V biased guard-ring constructs on the penetration of excess carriers into latch-up sensitive regions is analyzed with −200 mA pulses. In the case of floating n^+ guard-rings, the first (p^+) guard-ring is the only terminal that allows current to flow back to the pulse generator (see loop *1* and *4* in the schematic current flow in Figure 3.12). In the case of biased guard-rings electrons in substrate are collected by n diffusions (see dashed arrow in Figure 1.14a and loop *2* and *3* in Figure 3.12).

The phase shift transients at the injector for floating and biased n^+ guard-rings are shown in Figure 3.23. Biasing reduces the excess carrier density (negative phase shift) and causes stronger heating (higher slope during injection).

At near regions (at position n_2) biasing reduces the excess carrier density (fitting coefficient A from −40 mrad to −27 mrad) and the minority carrier lifetime from ∼480 ns to ∼350 ns (see Figures 3.18 and 3.24). At far regions (at position n_3) biasing reduces the excess carrier density (fitting coefficient A from −22 mrad to −16 mrad), but similar minority carrier lifetime (∼950 ns) is observed (see Figure 3.25).

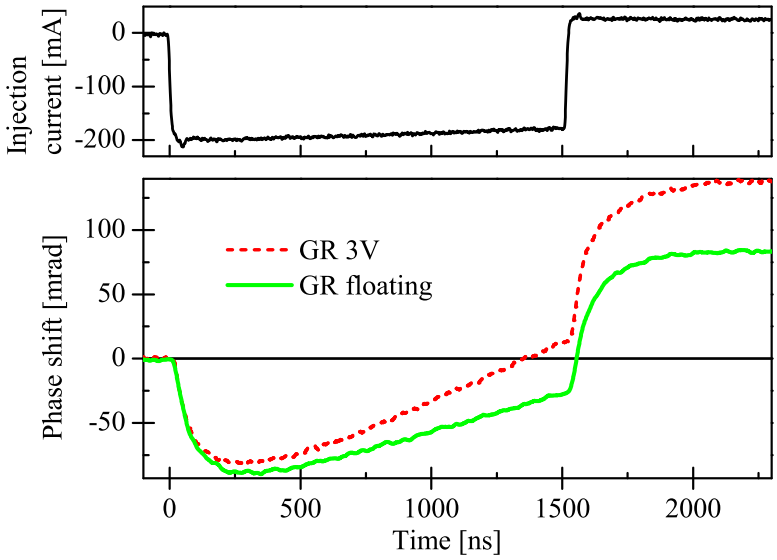


Figure 3.23: Phase shift measurements at injector (point n_1 in Figure 3.4) of the *large* latch-up test structure during negative injection at $-200\,\mathrm{mA}$ under floating and 3 V biased condition.

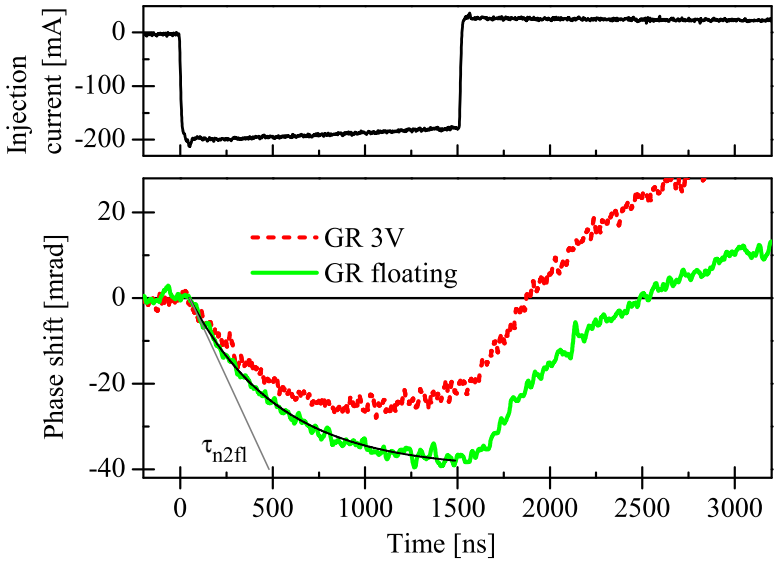


Figure 3.24: Phase shift measurements at point n_2 in Figure 3.4 of the *large* latch-up test structure during negative injection at $-200\,\mathrm{mA}$ under floating and 3 V biased condition. Effective minority carrier lifetime $\tau_{n2fl} \simeq 480\,\mathrm{ns}$ (see fitting line).

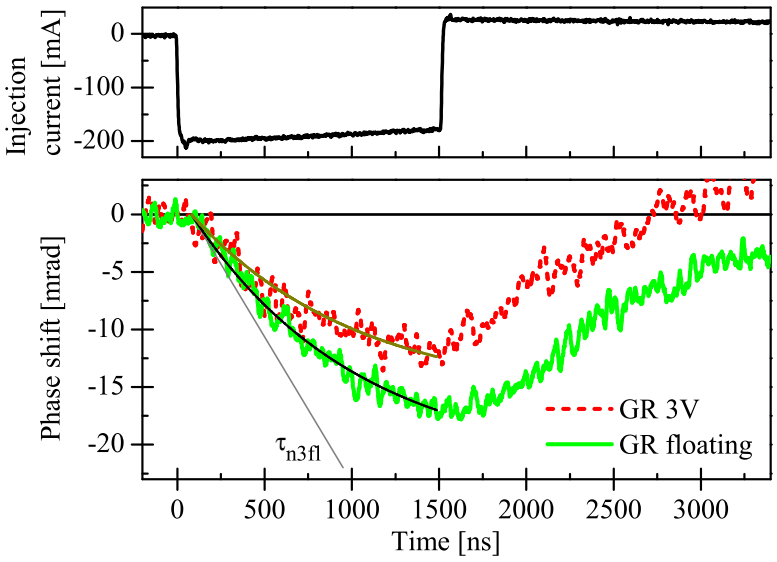


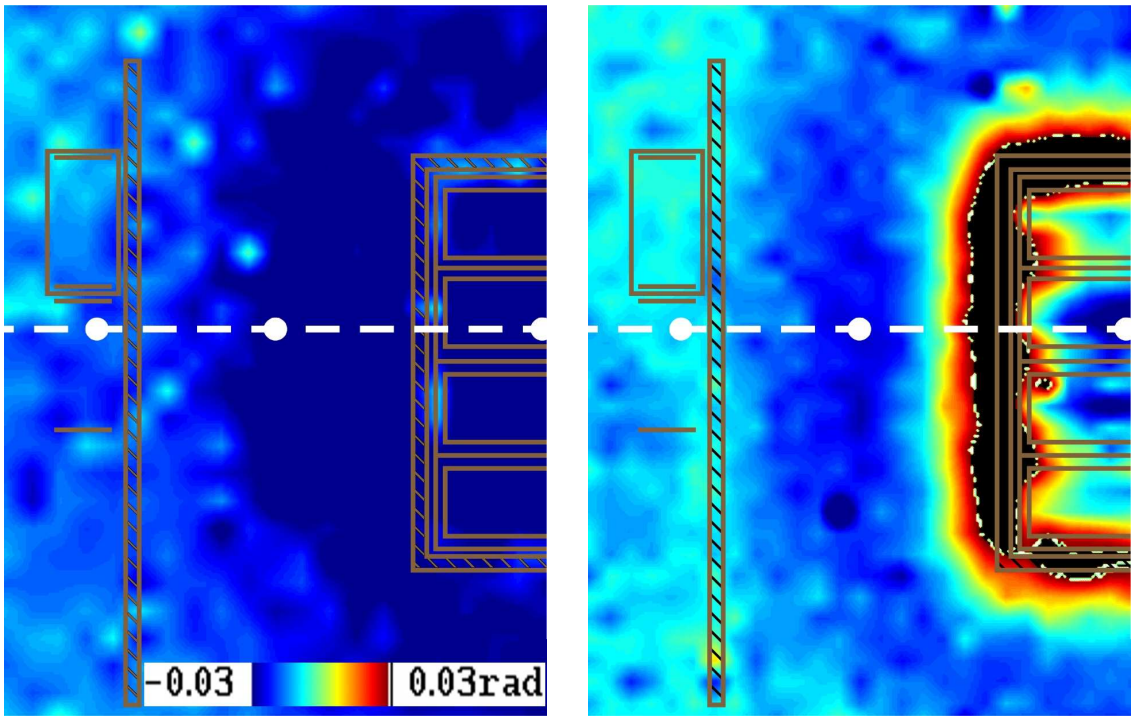
Figure 3.25: Phase shift measurements at detector structure (point n_3 in Figure 3.4) of the *large* latch-up test structure during negative injection at $-200\,\text{mA}$ under floating and 3 V biased condition. Effective minority carrier lifetime $\tau_{n3fl} \simeq 950\,\text{ns}$ (see fitting line).

The two-dimensional phase map at 1 µs is shown in Figure 3.26 for (a) floating and (b) biased n^+ guard-rings. The carrier diffusion process in substrate leads to a strong penetration of electrons (minority carriers) into lateral and vertical direction. Biasing of the n^+ guard-rings with 3 V significantly reduces the number of carriers traveling beyond the second (n^+) and third (n^+) guard-rings with respect to the floating case (see also the transients in Figures 3.24 and 3.25).

The comparison of the phase shift across the structure (along the dashed lines) for floating and biased case is given in Figure 3.27. It shows the reduction of excess carriers (see negative phase shift) traveling beyond the second guard-ring in the biased case.

For a first simple estimation of the carrier diffusion length during injection, the model of a one dimensional[14] *steady-state injection from one side* [5] – similar to the heat diffusion in Equations (1.2) and (1.4) – is fitted to the experimental data at $t = 1\,\mu\text{s}$. Two superimposed exponential decays – one representing a short diffusion length in a layer near the surface (dominating the near region) and one representing a long diffusion length in the low doped substrate (dominating the far region, see sketch in Figure 3.28) – are fitted with Equation (3.3) to the measured phase shift data $\Delta\varphi$ neglecting thermal (positive) contributions.

[14] The simulated electron concentration of this complex configuration with n and p guard-rings is shown later.



(a) (b)

Figure 3.26: Two-dimensional TIM phase shift scan (interpolated, top view – labels see Figure 3.4) of the investigated *large* latch-up test structure showing phase shift under negative current injection at $t = 1\,\mu s$. Blue color indicates negative phase shift corresponding to excess carrier concentration in substrate. The injected current is $-200\,mA$ and the guard-rings are (a) floating (carrier diffusion length dominating the near region $L_{1fl} = 23\,\mu m$), (b) biased with $VDD = 3\,V$ (carrier diffusion length dominating the near region $L_1 = 18\,\mu m$). Black color indicates phase shift exceeding $+30\,mrad$.

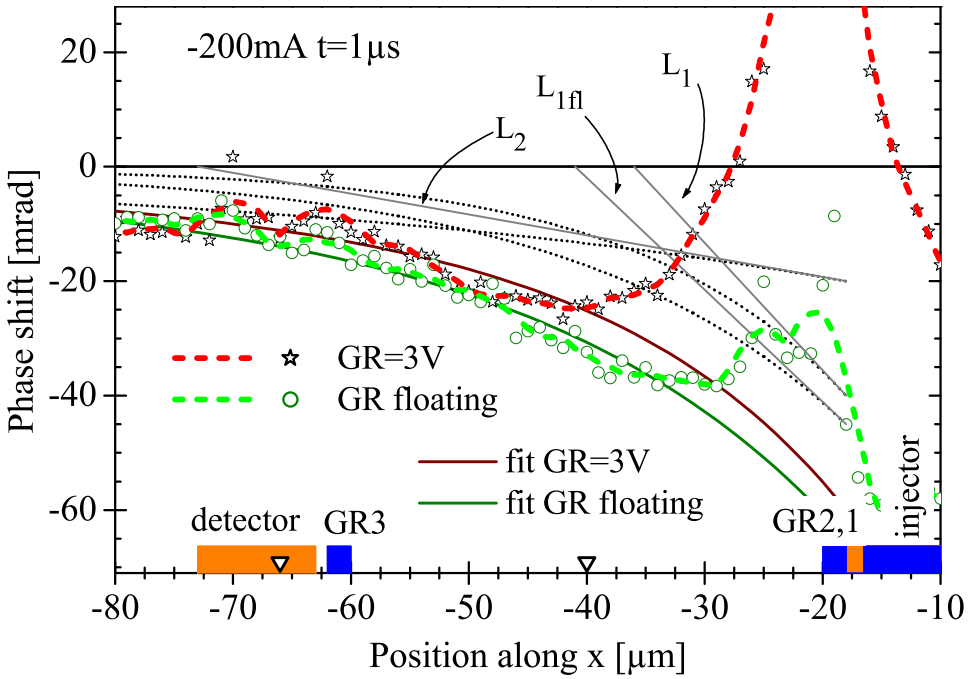


Figure 3.27: TIM measurement (represented by symbols) along the dashed lines of the 2D TIM pictures in Figure 3.26 at $t = 1\,\mu s$. The locations of the points n_2 and n_3 are marked with triangles. The diffusion length near the surface (dominating the near region) is $L_1 = 18\,\mu m$ for 3 V biasing (23 µm for floating guard-rings) and in the low doped substrate (dominating the far region) it is $L_2 = 55\,\mu m$.

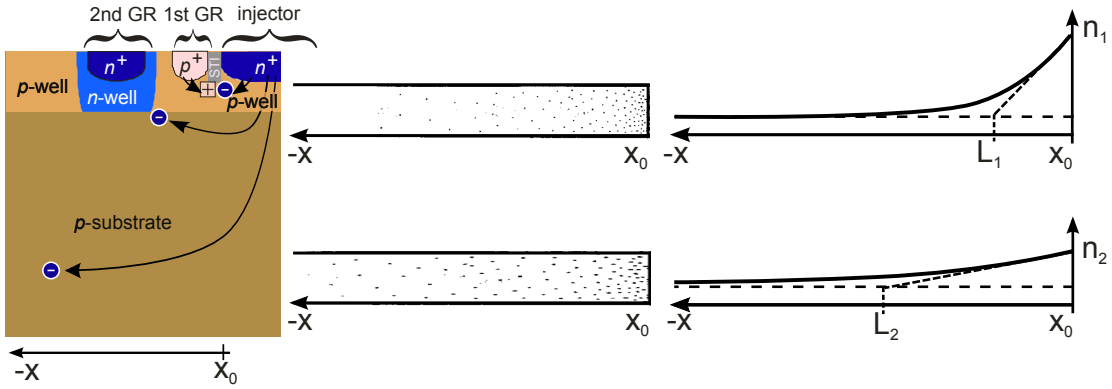


Figure 3.28: Schematic steady-state diffusion from one side (after [5]). Top: Short diffusion length L_1 in a layer near the surface (dominating the near region), which is affected by guard-rings and higher doped wells. Bottom: Long diffusion length L_2 in the low doped substrate (dominating the far region).

$$\Delta\varphi(x) = B_1\,\mathrm{e}^{\frac{x-x_0}{L_1}} + B_2\,\mathrm{e}^{\frac{x-x_0}{L_2}} \quad \Big|_{\,x\leq x_0\leq 0} \tag{3.3}$$

In the floating case the phase shift (carrier diffusion) is approximated in near region with the spatial decay constant (diffusion length) $L_{1\mathrm{fl}} = 23\,\mu\mathrm{m}$ and fitting coefficient $B_{1\mathrm{fl}} = -45\,\mathrm{mrad}$. The far region (within p substrate) is fitted with diffusion length $L_2 = 55\,\mu\mathrm{m}$ and coefficient $B_2 = -20\,\mathrm{mrad}$. The phase shift for biased guard-rings in near region is modeled with diffusion length $L_1 = 18\,\mu\mathrm{m}$ and fitting coefficient $B_1 = -40\,\mathrm{mrad}$.

The near region is characterized by substrate contacts and guard-rings (high doping concentration, high recombination rate, short effective lifetime). The far region is characterized by the long effective minority carrier lifetime in low doped p substrate. The excess carrier contribution from substrate would explain the observed slow phase shift decay at the injector in Figure 3.17 for $t > 1700\,\mathrm{ns}$.

Using Equation (3.4) with the nearly steady state diffusion length for near regions $L_{1\mathrm{fl}}$ and the lifetime τ_{n2fl} in near regions (point n_2) the diffusion coefficient for minority carriers (electrons) results in $D_\mathrm{n} = 11\,\mathrm{cm}^2/\mathrm{s}$ for the floating case and in $D_\mathrm{n} = 9\,\mathrm{cm}^2/\mathrm{s}$ for the biased case. For far regions the diffusion length L_2 and the lifetime $\tau_{\mathrm{n}3}$ result in a diffusion coefficient of $D_\mathrm{n} = 32\,\mathrm{cm}^2/\mathrm{s}$.

$$D = \frac{L^2}{\tau} \tag{3.4}$$

The mobility for electrons in p substrate can be calculated with the *Einstein* relation [1] in Equation (3.5), the Boltzmann constant $\mathrm{k_B}$, temperature T and electronic charge q.

$$\mu = D\frac{\mathrm{q}}{\mathrm{k_B}T}\ . \tag{3.5}$$

The resulting mobility and diffusion parameters for electrons[15] are summarized in Table 3.2. It shows 9 to 32 times higher diffusion coefficients for excess minority carriers than the thermal diffusion coefficient of silicon ($0.98\,\mathrm{cm}^2\mathrm{s}^{-1}$). Considering effective doping concentrations, these values are compatible with [1]. The different spreading of excess carriers and heat is clearly visible in the phase shift measurement in Figures 3.19 and 3.20.

[15] Minority carrier lifetime and diffusion length in plain p substrate (e.g. unprocessed wafer without any wells) will be much higher.

Region and guard-ring biasing	Lifetime τ_n [ns]	Fitting coefficient A [mrad]	Diffusion length L_n [µm]	Diffusion coefficient D_n [cm^2s^{-1}]	Mobility μ_n [$cm^2V^{-1}s^{-1}$]
near, GR floating	480	−40	23	11	426
near, GR 3V	350	−27	18	9	360
far, GR floating	950	−22	55	32	1230
far, GR 3V	950	−16	55	32	1230

Table 3.2: Parameters for negative injection with −200 mA (injected electrons) at near region (point n_2) and far region (point n_3) of a fully processed dual-well wafer. Guard-ring biasing reduces the fitting coefficient in near region about 33% and far region about 27%.

Comparison to TCAD simulations and discussion

In order to complete the picture of spreading carriers in the third dimension (depth) of silicon substrate[16], the experimental results are complemented with TCAD device simulations of a simplified two dimensional model performed previously at *Infineon Technologies AG* [4]. The two-dimensional TCAD simulations are performed along the cross sections A–B B–C in Figure 3.4[17]. Guard-ring biasing and injection current of the simulated structure is equivalent to the measurement conditions. The length of the injector and grounding (detector supply is not floating) are different. A current density of −1.66 mA/µm, which corresponds to −200 mA at a 120 µm wide junction, is applied to the injector pad (*Vinj*).

The snapshots of the calculated electron density under negative injection are shown in Figure 3.29. The arrangement is according to the schematic cross section in Figure 3.6a. The simulations show that the injected electrons spread deeply in substrate and avoid to enter the higher doped *p* well (0 to 1 µm depth) due to the potential difference (different doping concentrations) between *p* well and *p* substrate (see dotted arrow in Figure 1.14a). The static concentration of electrons in *n* wells is not visible in the TIM experiments, because the carrier density is constant and so the refractive index change $\Delta n(t) = 0$.

The sequence reflects the experimentally observed (lateral) spreading of carriers in the two-dimensional phase shift scans in Figure 3.20. In direct vicinity to the biased n^+ guard-rings (second and third), the electron concentration is lowered significantly. The n^+ guard-

[16] The TIM experiments represent the integrated refractive index changes along the depth (z) and their results are shown as *lateral* (top) view.

[17] Two-dimensional simulations require the rotation of the detector structure to the injector – otherwise three-dimensional simulations would be necessary.

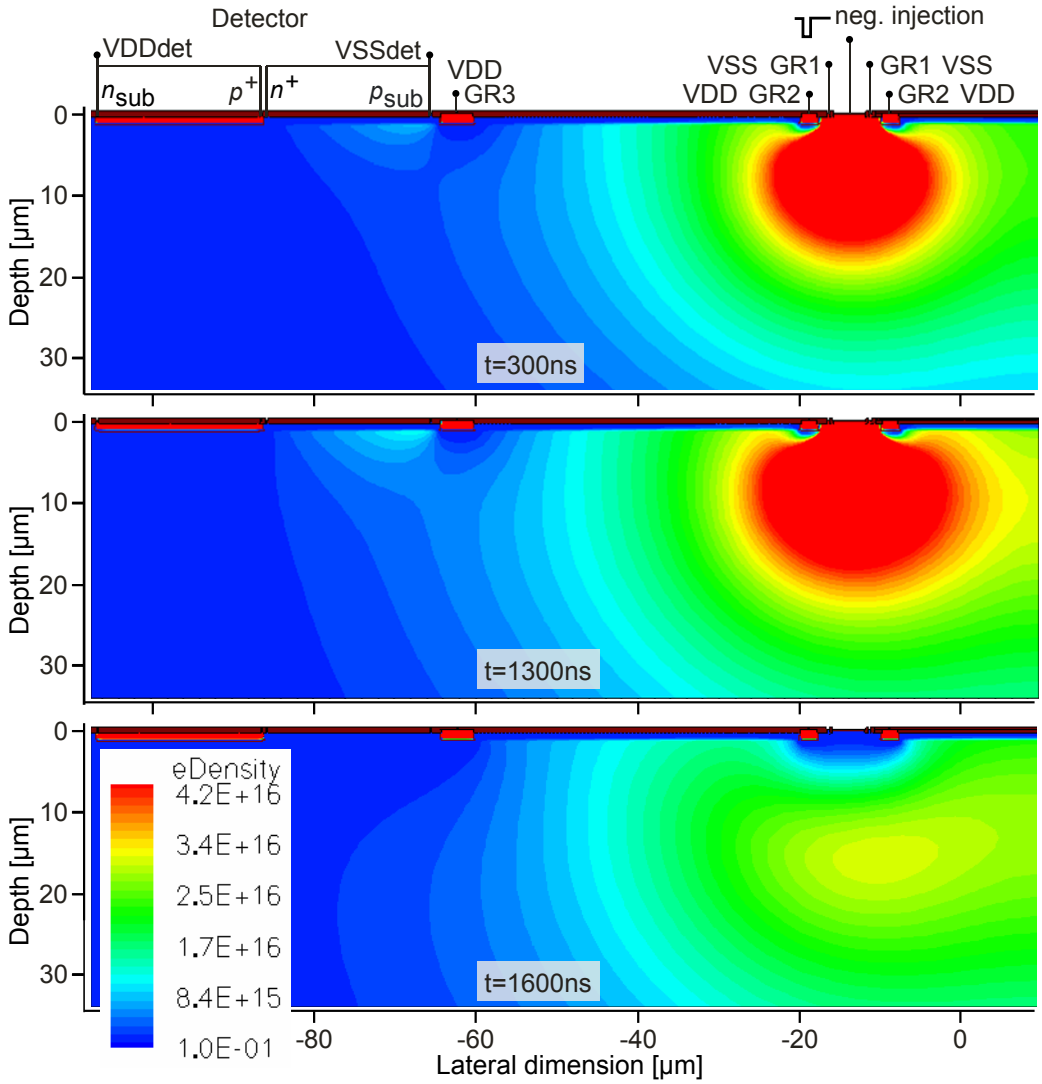


Figure 3.29: Two-dimensional TCAD simulation along cross sections A–B B–C (see Figure 3.4) of electron concentration (cm^{-3}) at $t = 300\,ns$, $1300\,ns$ and $1600\,ns$ of a $-1.66\,mA/\mu m$ ($-200\,mA$, non latching) injection pulse [4].

rings "collect" minority carriers (electrons) most effectively at the silicon surface up to a depth of approximately 6 µm. The decrease of the minority carrier concentration outside the space charge region of a reverse biased $p\,/\,n$ junction is sketched in Figure 1.15.

From the electron density the optical phase shift can be calculated with Equation (1.29). A simple approximation[18] at $x = -40\,\mu\text{m}$ with homogeneous carrier distribution of $1.7 \cdot 10^{16}\,\text{cm}^{-3}$ ($t = 1300\,\text{ns}$) for a depth of $z = 30\,\mu\text{m}$, assuming charge neutrality and neglecting heat results in a phase shift due to excess electrons of $-2.4\,\text{mrad}$ and due to excess holes of $-16.5\,\text{mrad}$ – totally $-18.9\,\text{mrad}$. This rough estimation is in good agreement with the measured phase shift at $x = -40\,\mu\text{m}$ in Figure 3.19. The calculated relation of excess carrier density, thickness and phase shift is shown in Figure 1.22.

In the injector area the electron density strongly decreases after the injection pulse due to collecting guard-rings and recombination. At $t = 1600\,\text{ns}$ still some remarkable electron concentration is present in substrate. Stored charge is also observed in the TIM experiments (curve n_3 in Figure 3.18 for $t > 1500\,\text{ns}$) and responsible for the slowly decreasing detector current after the injection in Figure 3.16.

The simulation of electron current density is shown in Figure 3.30. The overlaid flow

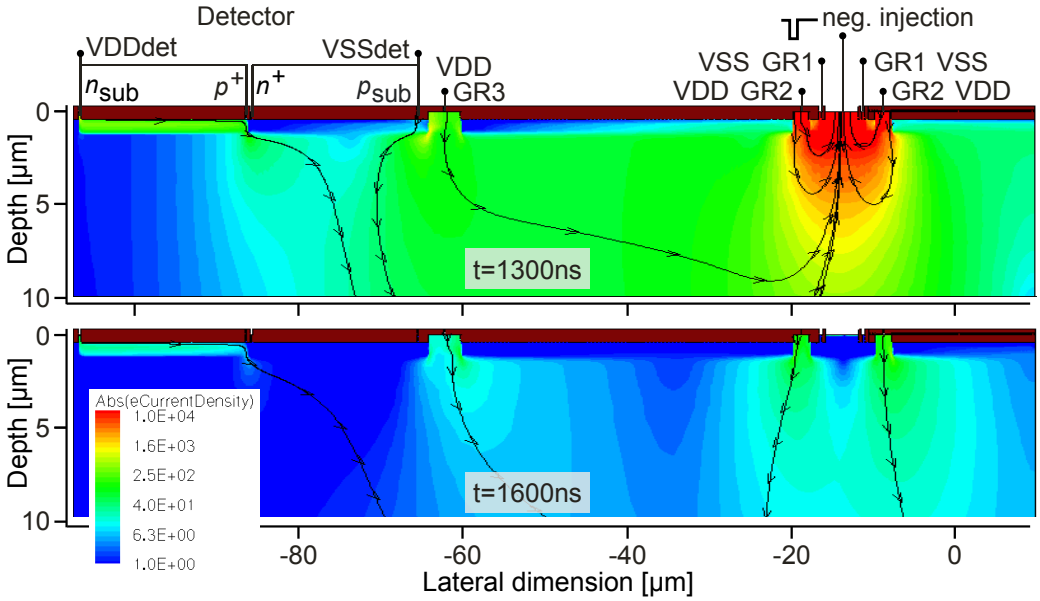


Figure 3.30: Two-dimensional TCAD simulation of electron current density (A/cm^2) with flow vectors during ($t = 1300\,\text{ns}$) and after ($t = 1600\,\text{ns}$) $-1.66\,\text{mA/µm}$ injection ($-200\,\text{mA}$, non latching) [106]. The flow vectors indicate direction of technical current flow.

vectors indicate the direction of *technical current flow*, which is in opposite direction of

[18] The simulated phase shift is shown later.

moving electrons[19]. The snapshot at $t = 1300\,\text{ns}$ shows the electron current density, which is highest between injector and second (n^+) guard-ring where the highest potential difference occurs. Beside the high electron current density in substrate, also high current density is observed at the third guard-ring and in the detector n well. The snapshot recorded 100 ns after the injection pulse ($t = 1600\,\text{ns}$) shows the electron current density originating from the collection of remaining excess electrons in substrate by the n wells of the guard-rings and the detector structure. This is also experimentally observed as slow decreasing guard-ring and detector current after the injection pulse in Figure 3.16.

The injected electron current is accompanied by hole current from the grounded p^+ terminals of the injector structure[20]. Further details about the two-dimensional TCAD simulations are shown in [109].

The phase shift components are calculated from TCAD data and compared with the experimental data (symbols) at $t = 1500\,\text{ns}$ in Figure 3.31. The lines show the two-dimensional TCAD simulation of the phase shift components [109]. The sum of the thermal ($\Delta\varphi_{\text{th}}$) and free carrier ($\Delta\varphi_{\text{fc}}$) contribution gives the total phase shift ($\Delta\varphi$). The simulation shows less free carrier contribution in far regions, which is related to the simplifications of the two-dimensional model.

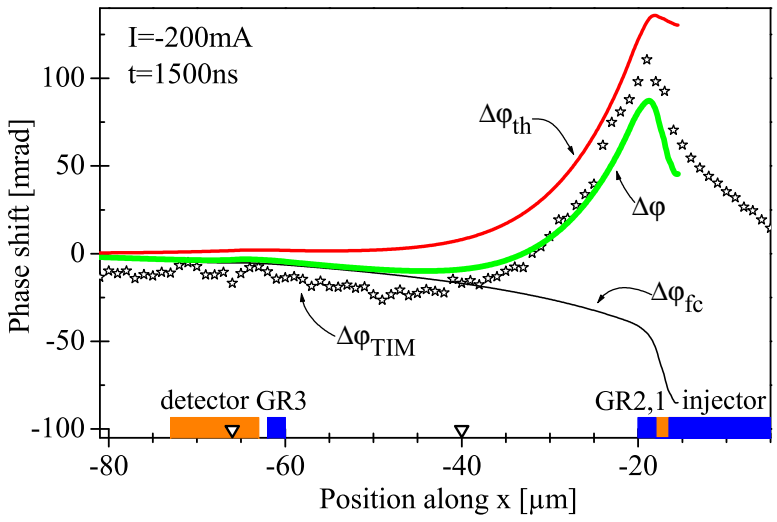


Figure 3.31: Phase shift comparison of TIM scan (symbols) and 2D TCAD simulation (lines) at $t = 1500\,\text{ns}$ during $-200\,\text{mA}$ injection on the *large* test structure [109]. The simulated total phase shift $\Delta\varphi$ is given by a thermal contribution $\Delta\varphi_{\text{th}}$ and a (negative) free carrier contribution $\Delta\varphi_{\text{fc}}$.

[19] The flow vectors represent only directions and not quantitative current densities.
[20] The direction of current flow at p_{sub} contact depends on the conditions at the detector potentials (floating voltage source or fixed at 0 V and 3 V).

3.1.4 Investigation of positive carrier injection at test structures

Transient or static latch-up could originate also from positive substrate currents (holes, majority carriers) injected from p^+ diffusions into p substrate. The influence of injection pulse amplitude, width, guard-ring bias and circuit topology on latch-up sensitivity is investigated for positive injection currents. Holes are injected by pulsing the injector pad (p^+) positive with respect to the *VSS* pad (p^+ guard-ring). The schematic cross section of the investigated structures is shown in Figure 3.6b. The n^+ guard-rings (*VDD* pad) are biased with 3 V. The latch-up detector structure (VDD_{det} and VSS_{det} pads) is biased with a floating 3 V DC source. All experiments are performed at room temperature. The TIM method is used to trace the propagation of excess carriers in the latch-up test structures.

Exemplary the experimental investigations of the more sensitive structures are shown. The experimental results are complemented with two dimensional TCAD simulations of a simplified layout performed by *K. Domański* [4] to gain insight also into the behavior in the third dimension (depth) of the structures.

Latch-up identification

The current and voltage transients for a positive 191 mA injection pulse[21] of 1500 ns duration on a *small* test structure are shown in Figure 3.32. During the injection pulse negative guard-ring current is flowing and the latch-up detector current is slightly negative ("1") – this will be explained later. The latch-up detector current flow stops after $t =$ 1800 ns ("2"), indicating no latch-up of the SCR structure.

If the injection current is slightly higher, the SCR latches *after* the terminating edge of the injection pulse[22] and current flows self-sustaining through the detector structure. Figure 3.33 shows the current and voltage transients for a latching 197 mA injection pulse, where the latch-up current in the detector structure settles around 20 mA ("1"). In the latched state the detector voltage drops to approximately 2.2 V ("2").

[21] The used *Tektronix CT1* current transducer causes the falling slope ("3") of the actually square injection pulse.

[22] Only latch-up *after* the terminating edge of the injection pulse is observed (test structures for negative injection may latch already during the injection pulse).

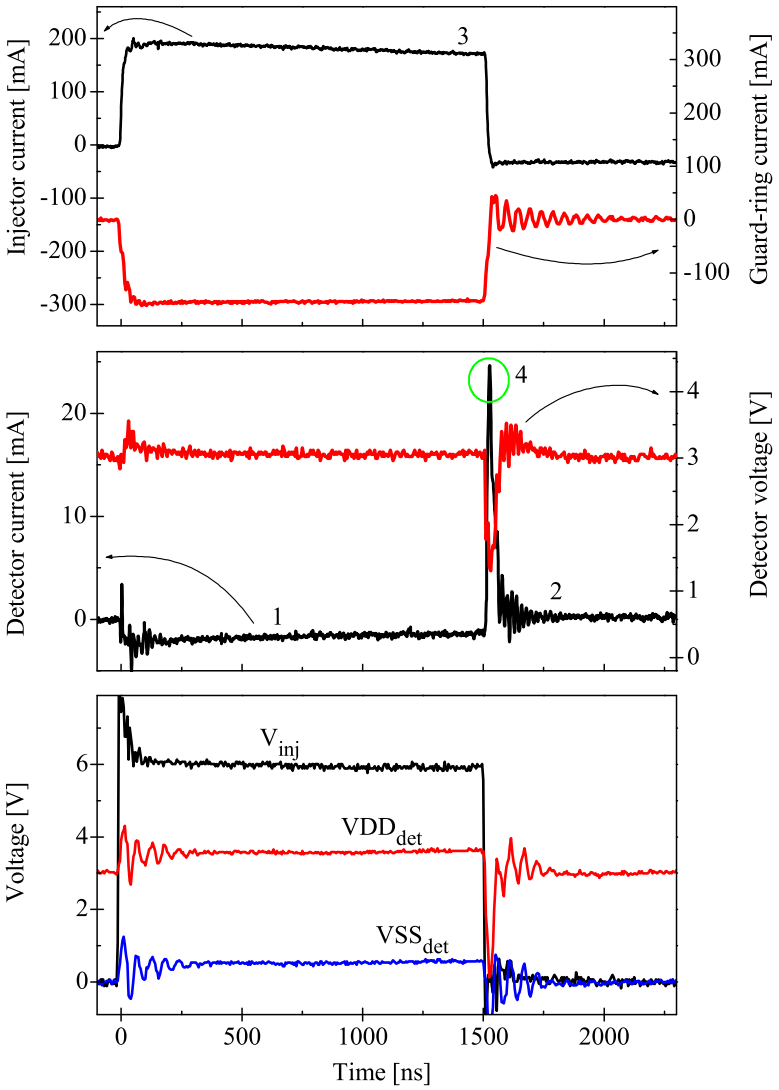


Figure 3.32: Current and voltage transients on the terminals of the *small* latch-up test structure (Figure 3.5) during positive 191 mA injection. The detector current flow stops after the injection pulse – indicating no latch-up (see "2").

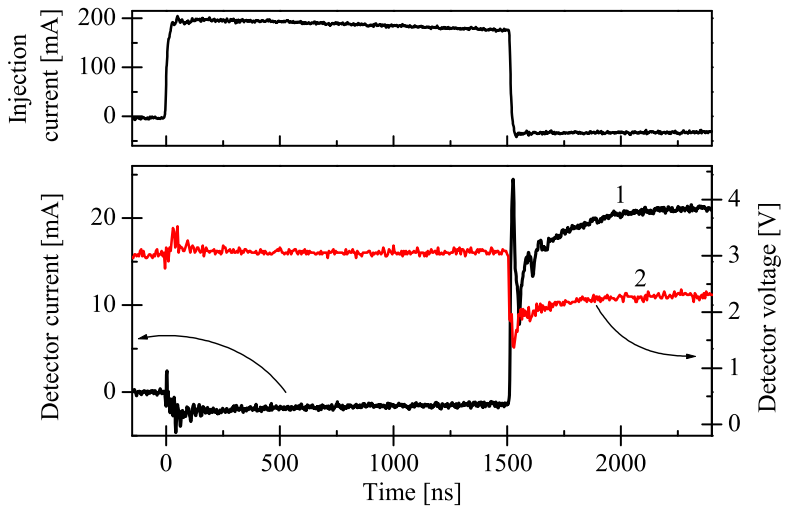


Figure 3.33: Current and voltage transients on the terminals of the *small* latch-up test structure (Figure 3.5) during positive 197 mA injection. The detector structure latches after the injection pulse (see "1").

Trigger current characteristics for positive injection

The effect of injection pulse width on *external* latch-up trigger current[23] is investigated for *small* and *large* latch-up test structures.

The experimentally obtained *external* latch-up trigger currents are summarized for *small* test structures in Figure 3.34 for various injection pulse durations. The increase of pulse width results in a higher latch-up sensitivity (lower injection current triggers latch-up). The latch-up trigger current stabilizes for pulses longer than ∼3 µs. For pulses shorter than ∼50 ns no latch-up is observed. The trigger current characteristics indicate values roughly 2–3 times higher compared to the corresponding negative injection current (compare graphs in Figures 3.15a and 3.34).

In contrast, the *large* structures could not be latched with positive injection pulses in this configuration. Similar structures used for negative injection are easily triggered to latch-up under analogous conditions, as shown in Figure 3.15b.

Excess carrier and heat spreading below latch-up condition

Excess carrier distribution and heat spreading during positive injection current is investigated with optical TIM experiments to explain the differences to negative substrate currents. In order to focus on carriers originating from the injector structure – and not

[23] Minimal *external* injection current which triggers latch-up.

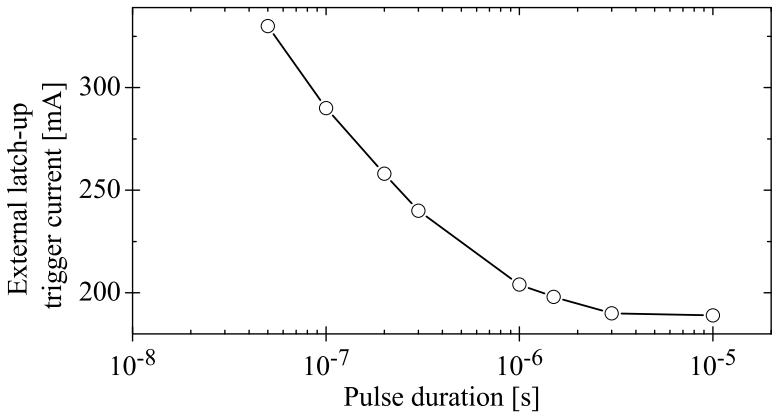


Figure 3.34: Effect of injection pulse duration on positive *external* latch-up trigger current for the investigated *small* test structures. For the details of test structure topology refer to Figures 3.5 and 3.6b.

from the latched state of the detector structure (SCR) – most optical investigations are performed below latch-up condition. The *small* latch-up test structures are investigated under 1500 ns injection pulses shown in Figure 3.32.

The phase shift transient measured in the middle of the injector structure is shown in curve $\Delta\varphi$ in Figure 3.35. It is composed of a thermal contribution $\Delta\varphi_{\mathrm{th}}$ and a (negative) excess carrier contribution $\Delta\varphi_{\mathrm{fc}}$. The dashed line shows the assumed evolution of the thermal component. The dotted line represents the excess carrier component as difference of the total phase shift and the assumed thermal contribution ($\Delta\varphi_{\mathrm{fc}} = \Delta\varphi - \Delta\varphi_{\mathrm{th}}$). The thermal contribution $\Delta\varphi_{\mathrm{th}}$ increases with time and lasts slightly longer than the injection pulse[24]. The higher injection voltage and the smaller area of the positive injector structure lead to higher local power density (temperature) and consequently to a higher slope of the thermal component (compare curve $\Delta\varphi_{\mathrm{th}}$ in Figures 3.35 and 3.18).

The fast rising phase shift at the pulse end is caused by recombination of carriers and decay of their negative phase shift contribution – similar as observed for negative injection. The phase shift decrease after the injection pulse is caused by cooling (decrease of thermal contribution). The estimation of the minority carrier lifetime (holes in the n well) with the fitting line of the free carrier component $\Delta\varphi_{\mathrm{fc}}$ at the terminating edge gives an effective lifetime of $\tau_{\mathrm{p}} \simeq 25$ ns. This short minority carrier lifetime is related to the layout (nearby n^+ and p^+ implantations) and the high doping concentration of the n well. In the injector region the effective lifetime of excess carriers during positive injection is nearly four times shorter than during negative injection.

[24] This is caused by heat transfer from hotter regions.

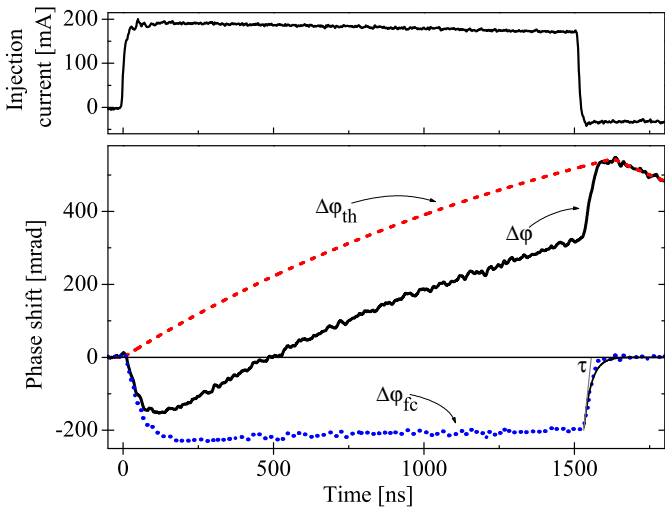


Figure 3.35: Decomposed phase shift components of a 1500 ns 191 mA current injection pulse at the center of the injector of the *small* (positive) latch-up test structure. The measured phase shift $\Delta\varphi$ is composed of a thermal contribution $\Delta\varphi_{\mathrm{th}}$ and a (negative) free carrier contribution $\Delta\varphi_{\mathrm{fc}}$. The dashed line shows the assumed evolution of the thermal component. The dotted line represents the difference of the total phase shift and the assumed thermal contribution. Effective minority carrier lifetime $\tau_{\mathrm{p}} \simeq 25\,\mathrm{ns}$ – see thin fitting line at the terminating edge. After the terminating edge of the injection pulse slight heating occurs due to heat transfer from hotter regions.

At positions further from the injector structure (positions p_2 and p_3) only positive phase shift is observed in Figure 3.36. Negative phase shift is clearly visible for analogous *external* negative injection current (see curves n_2 and n_3 in Figure 3.18).

The phase shift measurement across the structure (along the dashed line in Figure 3.5) is shown in Figure 3.37 for several instants during injection. The highest excess carrier concentration (lowest phase shift) is observed at the center of the injector structure ("1"). The excess carrier concentration vanishes at the edges of the injector. This is in agreement with [33], where it was found that excess holes are present only close to the injector structure and most of injected holes are captured by the p^+ guard-rings. The thermal contribution to the phase shift increases with time and heat propagates from the injector to lateral side. Further, the TIM scan shows significant heating at the edge of the detector structure ("2"). More information about this activity of the detector structure will be shown later.

Excess carriers could not be measured with TIM outside the first (n^+) guard-ring. *Drift current* to the second (p^+) guard-ring does not change the carrier concentration ($\Delta N = 0$) and so $\Delta\varphi_{\mathrm{fc}}(t) = 0$ (but it can cause heating). The TIM scan indicates that the lateral diffusion of excess carriers during positive injection must be very short.

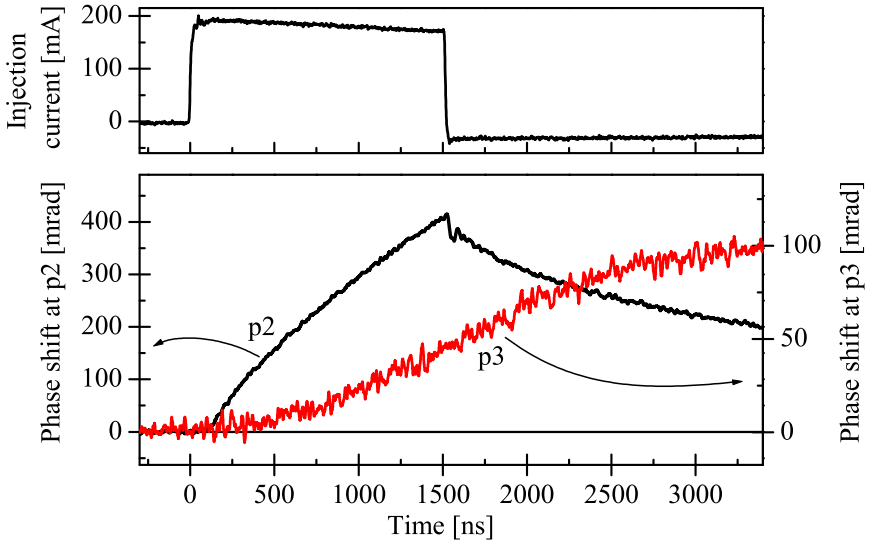


Figure 3.36: Phase shift measurements on the *small* latch-up test structure during positive injection, which are recorded at points p_2 and p_3 of Figure 3.5.

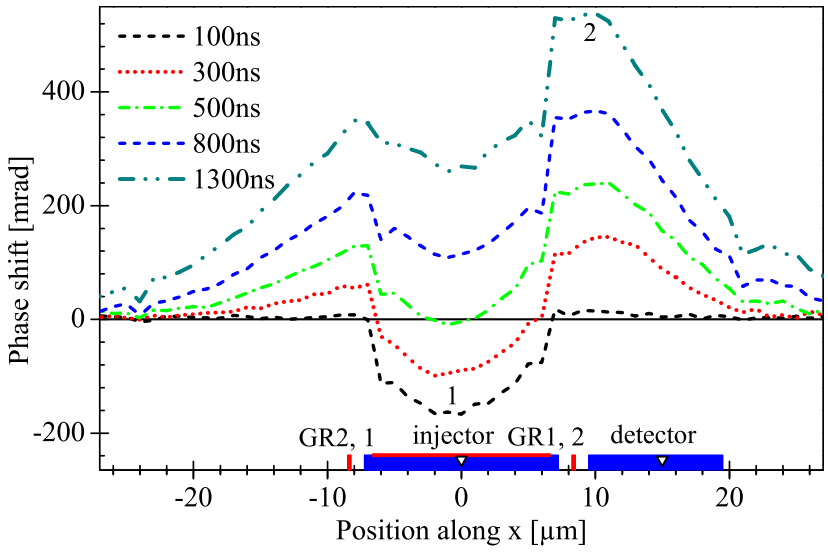


Figure 3.37: TIM scan with schematic cross section of the *small* positive test structure. No excess carriers (negative phase shift) outside the injector-*n* well could be measured. Significant heating ("2") occurs at the detector structure. Labels are shown in Figure 3.5.

A disturbance of charge neutrality by excess majority carriers (excess holes) in p substrate decays with the spatial decay constant (*Debye length*) L_{Dp}. For substrate doping concentrations around $10^{15}\,\mathrm{cm}^{-3}$ the Debye length is $L_{\mathrm{Dp}} \simeq 120\,\mathrm{nm}$ [1] and the diffusion coefficient of holes in Figure 3.38 [1] is $D_{\mathrm{p}} \simeq 10\,\mathrm{cm}^2/\mathrm{s}$.

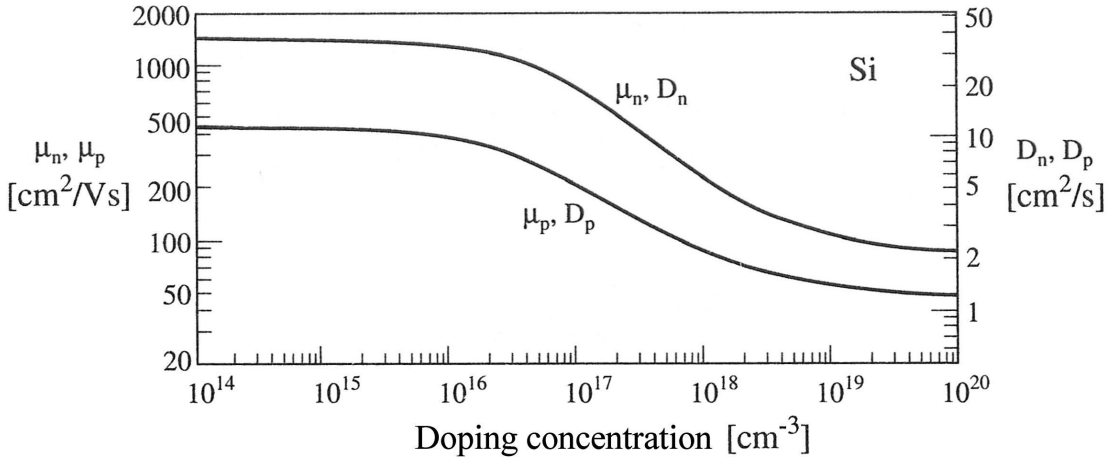


Figure 3.38: Diffusion coefficient D_{p} (D_{n}) and mobility μ_{p} (μ_{n}) of holes (electrons) in silicon vs. donor density [1].

The dielectric relaxation time[25] for majority carriers is calculated with

$$\tau_{\mathrm{dp}} = \frac{L_{\mathrm{Dp}}^2}{D_{\mathrm{p}}} \tag{3.6}$$

and results in $\tau_{\mathrm{dp}} \simeq 14\,\mathrm{ps}$. This is four decades shorter than the minority carrier lifetime in p substrate.

The diffusion length of minority carriers (excess holes) in the n well could not be measured by TIM experiments, because of the limited lateral free area[26] in the n well of the injector structure (see top view in Figure 3.5). Thus, the diffusion length is evaluated from the measured lifetime, the effective doping concentration and the diffusion coefficient. The lifetime in Figure 3.35 of $\tau_{\mathrm{p}} \simeq 25\,\mathrm{ns}$ can be related with Figure 3.39 [110] to an effective doping concentration of $\sim 2 \cdot 10^{19}\,\mathrm{cm/s}$. This doping concentration is related in Figure 3.38 to a diffusion coefficient of $D_{\mathrm{p}} \simeq 1.2\,\mathrm{cm}^2/\mathrm{s}$. The diffusion coefficient and the lifetime yield with Equation (1.5) to a diffusion length of holes in the n well of $L_{\mathrm{p}} \simeq 1.7\,\mu\mathrm{m}$.

Figure 3.40 shows two-dimensional phase shift snapshots of the test structure at four instants. The free carrier contribution is limited to the area of the injector structure (see

[25] $\tau_{\mathrm{d}} = \epsilon/\sigma$.

[26] For qualitative estimation of the diffusion length the lateral free space should be roughly five times larger than the diffusion length.

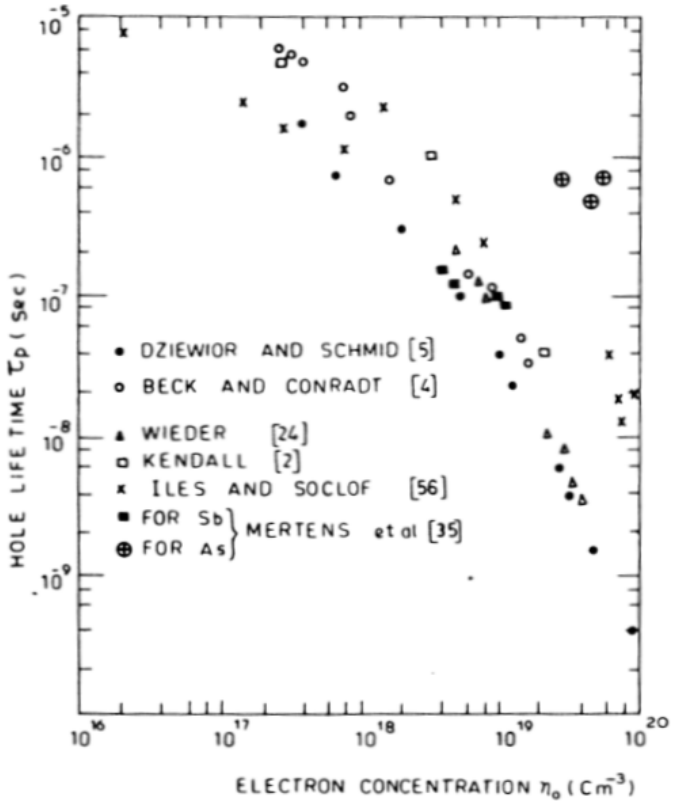


Figure 3.39: Lifetime τ_p of holes in n type silicon vs. donor density [110].

negative phase shift in Figure 3.40a). No excess carriers could be detected outside the first (n^+) guard-ring, only the spreading heat front with strong heating at the middle of the detector structure can be recognized at later instants.

The observed heating at the detector structure must be caused by significant power dissipation and consequently high current flow in the SCR – apparently higher current than measured in Figure 3.32 (which is even negative). A rough estimation of the required current (power) for a homogeneously distributed phase shift of 300 mrad in an area of $10\times10\,\mu\mathrm{m}$ at $t = 800\,\mathrm{ns}$ gives with Equation (1.35) a detector current of approximately 11 mA.

The discrepancy of high power dissipation in the SCR and negative detector current is explained with the schematic current flow in Figure 3.41. Starting with small positive injection currents (I_inj), the pulse generator (V_3) injects holes at the p^+ diffusion connected to the *Vinj* pad and same amount of electrons flows at the *VSS* pad[27]. The injected holes recombine with electrons at the forward biased p^+/n well junction in the injector structure. The electrons are supplied from the guard-ring supply (V_2) – resulting in negative

[27] Charge conservation for pulse generator V_3.

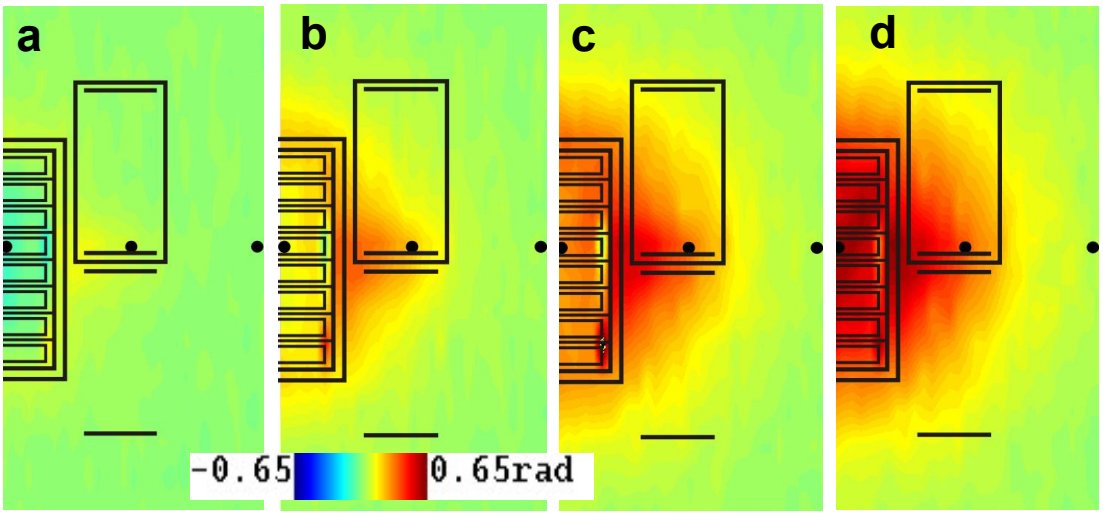


Figure 3.40: Two-dimensional TIM phase shift scan (interpolated, top view – see Figure 3.5 for labels) of *small* latch-up test structure at (a) $t = 300\,\text{ns}$, (b) $t = 800\,\text{ns}$, (c) $t = 1300\,\text{ns}$, (d) $t = 1600\,\text{ns}$ (100 ns after the end of pulse) of a 1500 ns long injection pulse. The black dots mark the points p_1–p_3 of the phase shift transients shown with the corresponding current waveforms in Figures 3.35 and 3.36.

guard-ring current I_{GR} (see dotted loop "1"). The current flow within the schematic cross section is shown in Figure 3.42. The rotated cross section of the detector structure should indicate equal distance of the injector structure to the n well and p well of the detector structure.

For increasing currents the parasitic *pnp* transistor Q_3 injects holes into substrate (see dashed loop "2"). For a 191 mA injection pulse the collector current (hole current) is around 36 mA (see injector and guard-ring currents in Figure 3.32). Some holes are collected by the second (p^+) guard-ring and this current flows back to the pulse generator. A part of injected holes move deeper into substrate. Holes which reach the p base of transistor Q_2 flow in the extended p well back to the second (p^+) guard-ring (see dash-dot loop "3"). Transistor Q_2 will be activated as soon as the voltage drop in the p well (R_2) is around 0.6 V.

For high injection currents, the injecting *pnp* transistor Q_3 operates in saturation regime and the local substrate potential (collector potential) increases above the guard-ring voltage of 3 V. If the local substrate potential is even higher than the potential of the detector n well, forward biasing of this junction occurs (see dotted loop "4" in Figure 3.42) and current flows from the injector to the detector n well (see also the shifted detector potentials of the measurements in Figure 3.32). The saturation of transistor Q_3 and the forward biasing of the p substrate / detector n well junction are sketched in the schematic energy

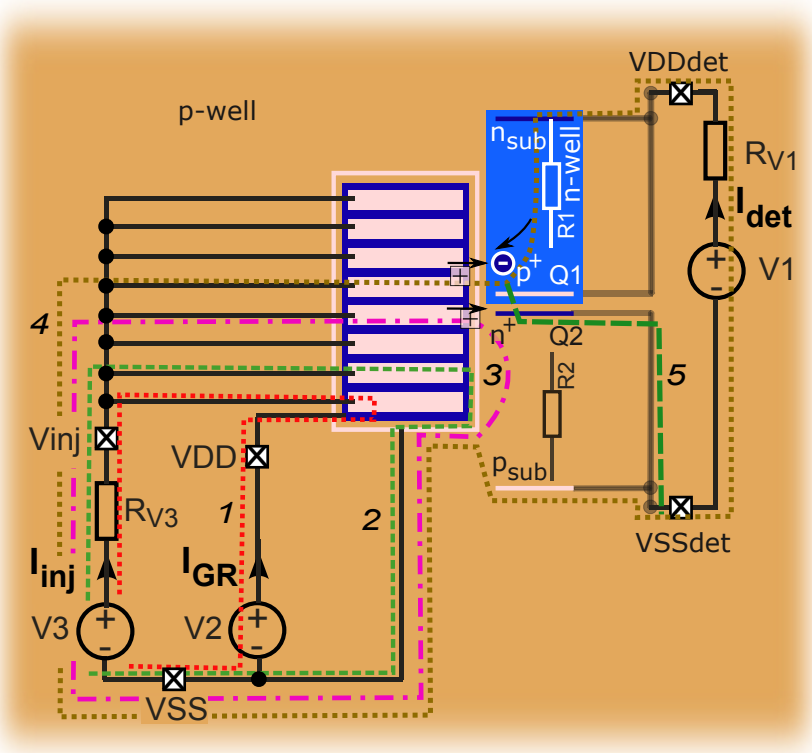


Figure 3.41: Simplified current flow in layout (top) view. Loop *1* shows current flowing from injector to first (n^+) guard-ring. Loop *2* shows current flowing from injector to second (p^+) guard-ring. Loop *3* is analogous, but with extended p well of detector structure. Loop *4* shows current flowing from injector to detector n well, detector supply V_1, p well, *VSS* and back to pulse generator. Line *5* shows the part of substrate current that flows across the activated transistor Q_2.

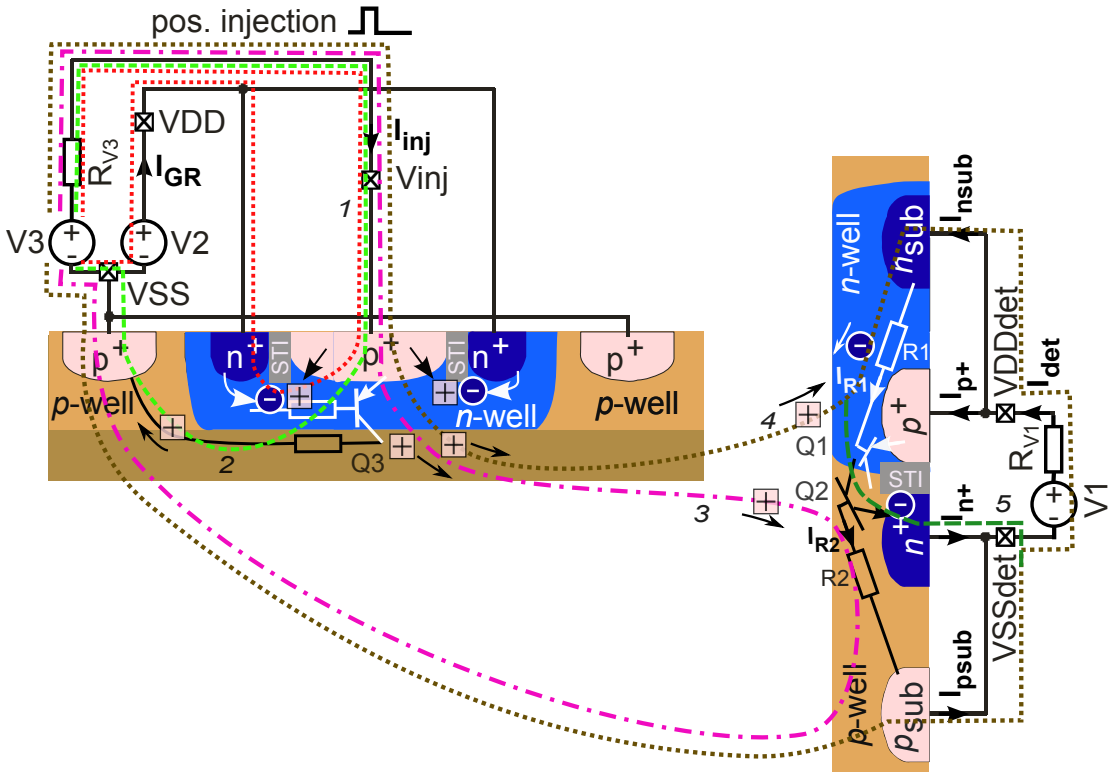


Figure 3.42: Simplified current flow with rotated schematic cross section (both SCR-wells are facing to injector – top view see Figure 3.41). Loop *1* shows positive charge flowing from pulse generator (V_3) to injector, first (n^+) guard-ring, *VDD*-pad, guard-ring supply (V_2), *VSS*-pad and back to pulse generator. Loop *2* shows charge flowing from injector across *n* well to *p* substrate, second (p^+) guard-ring, *VSS*-pad and back to pulse generator. Loop *3* is analogous, but with *p* well of detector. Loop *4* shows current flowing from injector to detector *n* well, detector supply V_1, *p* well, *VSS*-pad and back to pulse generator. Line *5* shows the part of substrate current that flows across the activated transistor Q_2.

band diagram in Figure 3.43. One part of the n well current flows to detector supply (V_1) – resulting in a *negative* n well current I_{R1} [28] and therefore in a *negative* contribution to the total detector current I_{det}. The other part flows across the activated transistor Q_2 (see line "5"). This means the injector "*powers*" transistor Q_2 – and even the detector voltage supply V_1. This effect causes high heating at the middle of the detector structure (see Figure 3.40) in combination with small negative currents at the detector supply. Holes from the detector area flow in the extended p well back to the second (p^+) guard-ring.

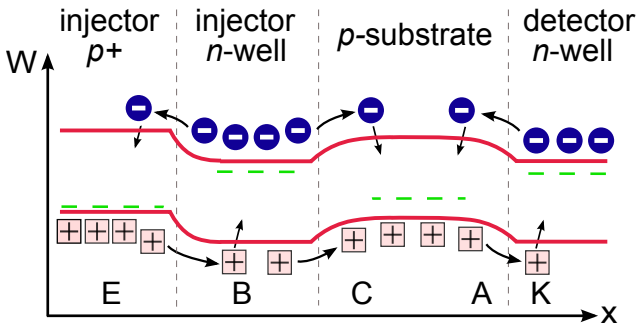


Figure 3.43: Simplified schematic energy band diagram showing saturation of the injector structure (*pnp* transistor Q_3 – E, B, C) and forward biasing of p substrate / detector n well junction (A, K).

At the terminating edge of the injection pulse the forward current flow at the p substrate / n well junction stops. Remaining minority carriers in the substrate are collected by the n well and the n_{sub} contact of the detector structure. The majority carriers, which shielded these minority carriers, are released and collected by the p_{sub} contacts. The collected minority (and majority) carriers cause the well-known *reverse recovery* current of p/n junctions. If this current through the n well (R_1) causes a voltage drop around 0.6 V, the *pnp* transistor Q_1 will be activated as well. This current flow causes a positive spike in the detector current transient (see "4" in Figure 3.32). If this current is high and long enough, latch-up occurs (see "1" in Figure 3.33). Now both bipolar transistors are active and self-sustaining current flows through the detector structure – similar as for negative injection currents (see loop "6" in Figure 3.12).

SPICE modeling of *small* latch-up test structure under positive injection

The observed negative detector current in conjunction with significant heating at the detector structure during positive injection current is reproduced with a *SPICE* simulation of the lumped circuit shown in Figure 3.44.

[28] *Negative* current flow through R_1 diminishes activation of *pnp* transistor Q_1.

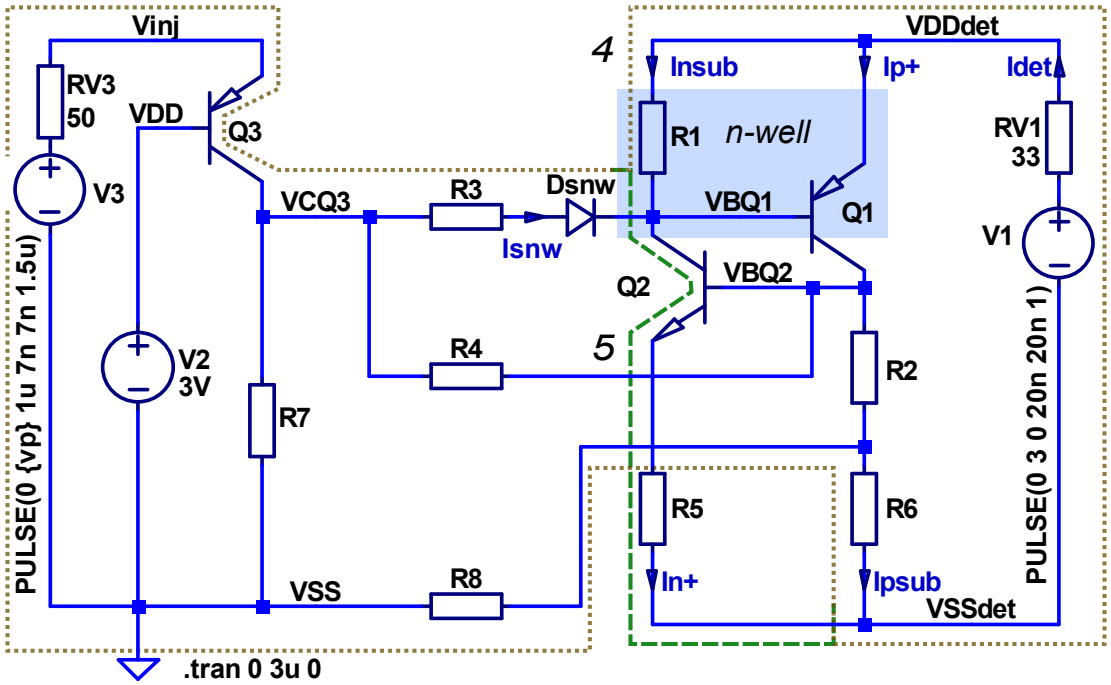


Figure 3.44: Lumped circuit of positive external latch-up structure. At left side is the injector with intrinsic transistor Q_3 and on the right side is the detector structure with parasitic transistors Q_1 and Q_2.

```
1  .model Q3 PNP (IS=1e-14 VAF=100 BF=4 ikf=0.4 xtb=1.5 BR=4
2  CJC=4e-12 cje=8e-12 rb=12 rc=37 re=2 TR=2.5e-9 tf=350e-12 itf=1
3  vtf=2 xtf=3 vceo=40 icrating=200m mfg=ifx)
```

Listing 3.2: *SPICE* transistor model for the positive injector structure.

The injection pulse is approximated with a pulse voltage source (V_3) and load line resistor R_{V3}. It is connected to the *pnp* transistor Q_3, which represents the injector structure. The adapted transistor model parameters of the injector structure (modified *2N3906* transistor) are shown in Listing 3.2. The voltage supply V_2 biases the guard-rings.

Diode D_{snw} (*1N4148* diode) and resistor R_3 (10 Ω) represent the *p* substrate / *n* well junction of the detector structure. The detector structure is the same as used for *SPICE* simulation of the negative injector structure. The substrate resistance to the base region (*p* well) of transistor Q_2 is shown as R_4 (295 Ω). The resistors R_5 and R_6 represent parasitic resistances (4 Ω). The resistors R_7 (350 Ω) and R_8 (20 Ω) represent distributed substrate resistances.

The pulse amplitude parameter ".param *vp* 15.6 V" corresponds to an injection current of $I_{inj} \simeq 191$ mA, which is slightly below latch-up condition. For the simulation of a latching

pulse the amplitude parameter ".param *vp* 16 V" is used ($I_{\mathrm{inj}} \simeq 197\,\mathrm{mA}$). The *SPICE* results of such a latching pulse are shown in Figure 3.45. It shows negative detector current ("1") during the injection pulse and positive detector current in the latched state ("2") after the injection pulse.

The activity of transistor Q_3 increases the collector potential V_{CQ3} until transistor Q_3 saturates. The reason for negative detector current during injection is collector potential (V_{CQ3}) increase above the potential of the detector *n* well (V_{BQ1}). This causes forward biasing of the diode D_{snw} (*p* substrate / *n* well junction of the detector structure) and the base / emitter junction of *npn* transistor Q_2. The simulations and measurements show detector potential shifts around 0.5 V during the injection pulse (see Figures 3.45 and 3.32). The substrate current to the detector *n* well (I_{snw}) splits into I_{nsub} (a negative contribution to the detector current I_{det}, see loop "4" in Figure 3.44) and into a positive contribution to the collector current of transistor Q_2 (see line "5"). The *negative* I_{nsub} current across R_1 prevents activation of *pnp* transistor Q_1 during injection (see $V_{\mathrm{BEQ1}} > 0$). That explains why latch-up may start just with the terminating edge of the positive injection pulse, when the negative contribution of I_{snw} to I_{nsub} stops. The negative detector current (I_{det}) causes slightly increased detector voltage (V_{det}) during the injection pulse ("3") due to the series resistor at the detector supply V_1. The simulation of the total transistor power (P_{Q1}, P_{Q2}) shows that transistor Q_2 heats the detector structure during injection (see "4").

At the terminating edge of the injection pulse the *reverse recovery* current of diode D_{snw} (*p* substrate / *n* well junction of the detector structure) causes a positive voltage drop at resistor R_1. This voltage drop might activate the *pnp* transistor Q_1. This current flow is visible as significant spike in the detector current flow at the end of the injection pulse (see "4" in Figure 3.32). If this current is high and long enough, latch-up occurs – see "2" at detector current transient in Figure 3.45. During latch-up both transistors heat the detector structure ("5").

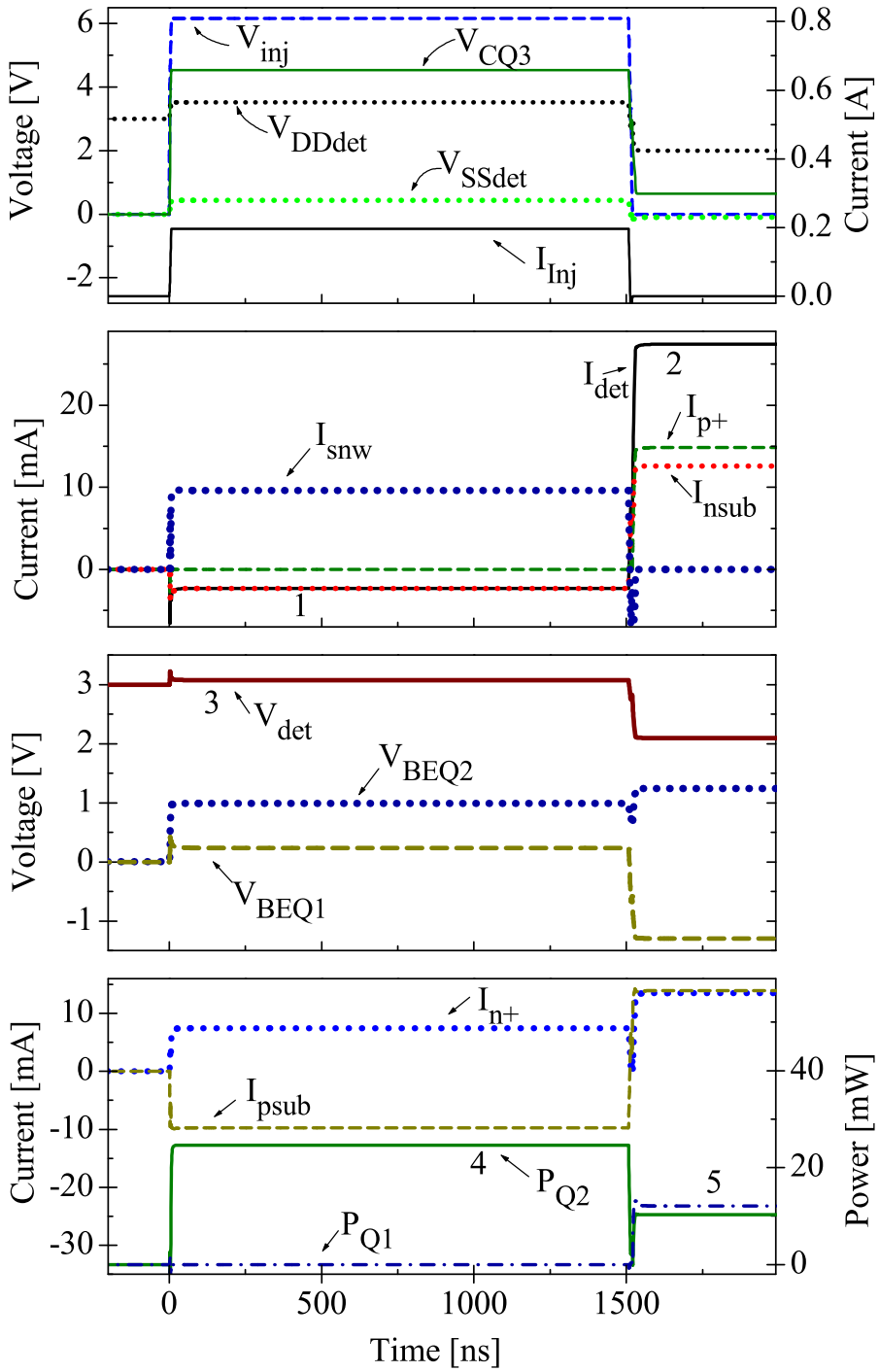


Figure 3.45: *SPICE* simulation of 197 mA injection pulse showing negative detector current (I_{det}) during the injection pulse ("1") and latch-up afterwards ("2").

Comparison to TCAD simulations

The experimental results are complemented with TCAD device simulations of a simplified two dimensional model performed at *Infineon Technologies AG*. The TCAD simulations are performed along the cross sections A–B B–D in Figure 3.5. Guard-ring biasing and injection current of the simulated structure is equivalent to the measurement conditions. The length of the injector and grounding (detector supply is not floating) are different.

Snapshots of the simulated hole concentration are shown in Figure 3.46. High excess hole density is present only in the injector region (see snapshot at $t = 1300\,\text{ns}$). The hole density in the snapshot 100 ns after the injection pulse (at $t = 1600\,\text{ns}$) is already similar to the unstressed level[29] – high hole density in p wells and very low hole density in n regions.

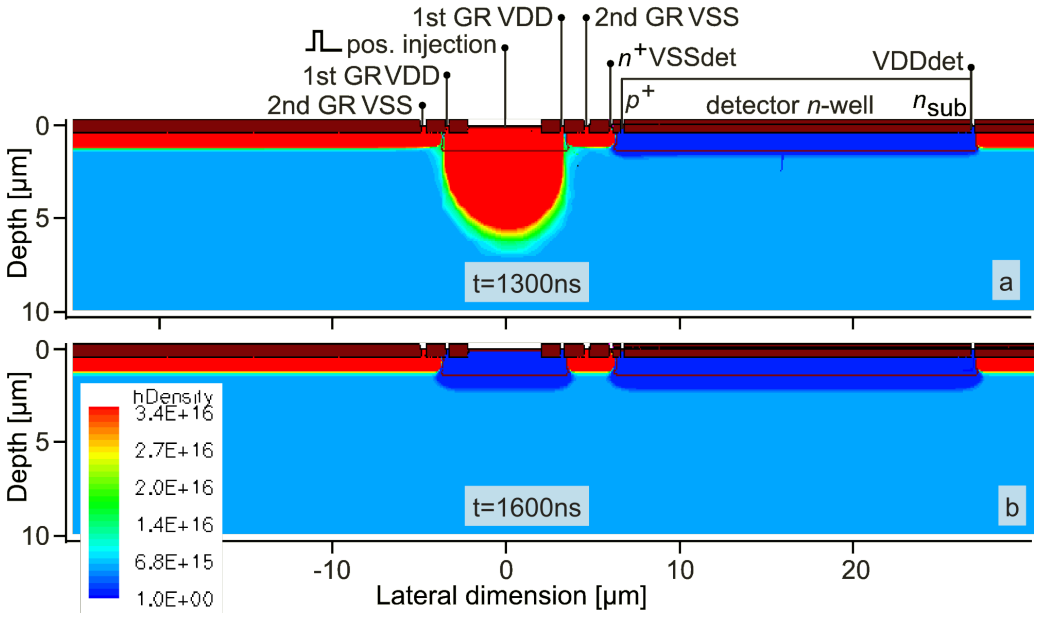


Figure 3.46: Two-dimensional TCAD simulation of hole density (cm^{-3}) during ($t = 1300\,\text{ns}$) and after ($t = 1600\,\text{ns}$) a positive injection pulse of 1500 ns duration [106].

The simulated electron concentration is shown in Figure 3.47. It shows at $t = 1300\,\text{ns}$ high electron density in p substrate below the injector diffusion. This high minority carrier concentration in the collector region (n_C) indicates saturation of the injecting *pnp* transistor Q_3 (base / collector diode is forward biased and injects minority carriers). The schematic minority carrier concentration of an unsaturated and a saturated *pnp* transistor is sketched in Figure 3.48.

[29] The static concentration of excess holes and electrons is not visible in the TIM experiments, because the carrier density is constant and so the refractive index change $\Delta n(t) = 0$.

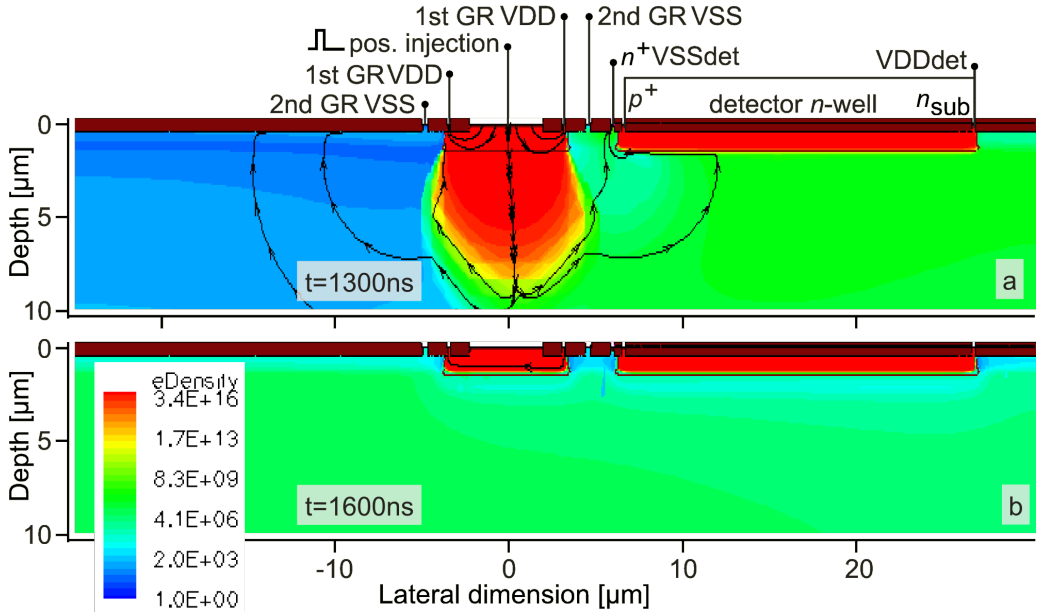


Figure 3.47: Two-dimensional TCAD simulation of electron density (cm^{-3}) during ($t = 1300$ ns) and after ($t = 1600$ ns) a positive injection pulse of 1500 ns duration [105].

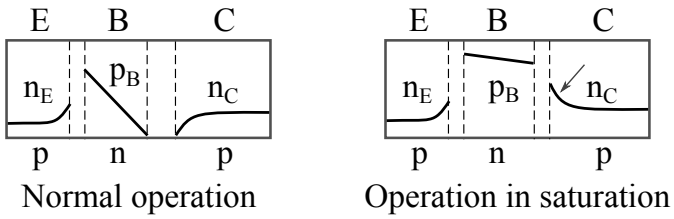


Figure 3.48: Sketch of the minority carrier concentration of an unsaturated and saturated *pnp* transistor (after [1]). n_E denotes the electron concentration in the emitter (E), p_B denotes the hole concentration in the base (B) and n_C denotes the electron concentration in the collector (C). Saturation of the bipolar transistor causes high minority carrier (electron) concentration n_C in the collector (see arrow) due to forward biasing of the base / collector diode.

The simulation of the substrate potential at $t = 1300\,\text{ns}$ in Figure 3.49 shows increased potential below the injector (saturation of the injecting *pnp* transistor Q_3) and an elevated potential at the detector structure. This detector potential shift is compatible with the detector voltage measurements in Figure 3.32. The potential in the snapshot 100 ns after the injection pulse (at $t = 1600\,\text{ns}$) is already similar to the unstressed level.

The comparison of excess carrier concentrations for negative and positive injection currents shows that excess holes do not penetrate remarkable distances in *p* substrate like it is observed for excess electrons (compare Figures 3.29 and 3.46).

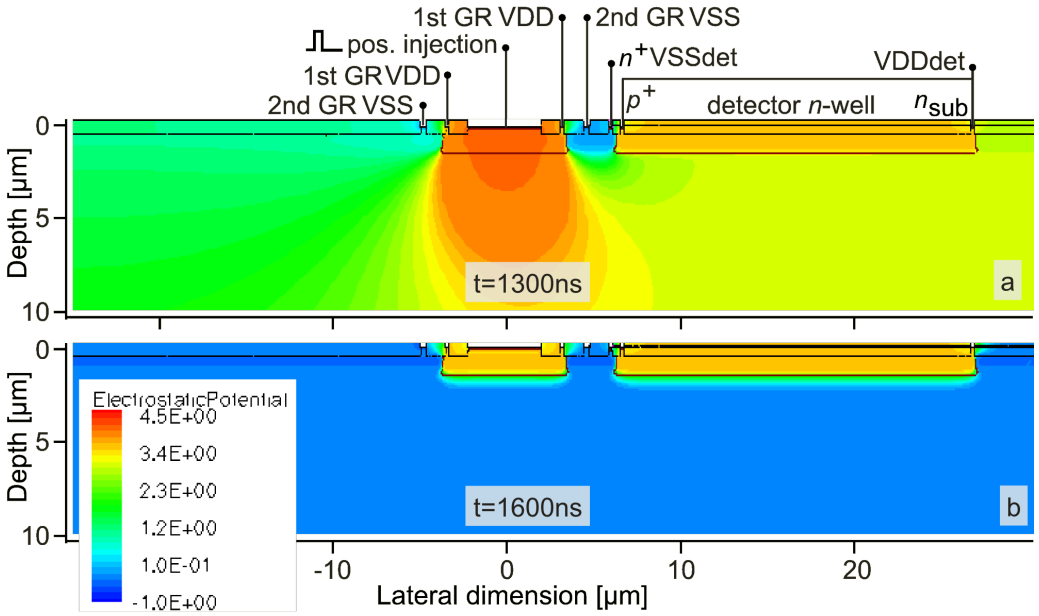


Figure 3.49: Two-dimensional TCAD simulation of electrostatic potential (V) during ($t = 1300\,\text{ns}$) and after ($t = 1600\,\text{ns}$) a positive injection pulse of 1500 ns duration [105].

Transition to the latched state

If the injection current is high enough, the detector structure latches at the terminating edge of the injection pulse. The voltage and current transients for a latching 197 mA injection pulse are shown in Figure 3.33, where the latch-up current in the detector structure settles around 20 mA. The corresponding phase shift transient at the center of the detector structure is shown in Figure 3.50.

The heating during injection ("1") is similar to the measured phase shift transient for a non-latching pulse (see curve p_2 in Figure 3.36) and also caused by the activated transistor Q_2. At the terminating edge of the injection pulse a significant drop ("2") in the measured phase shift transient is observed. The sudden drop must be caused by additional carriers

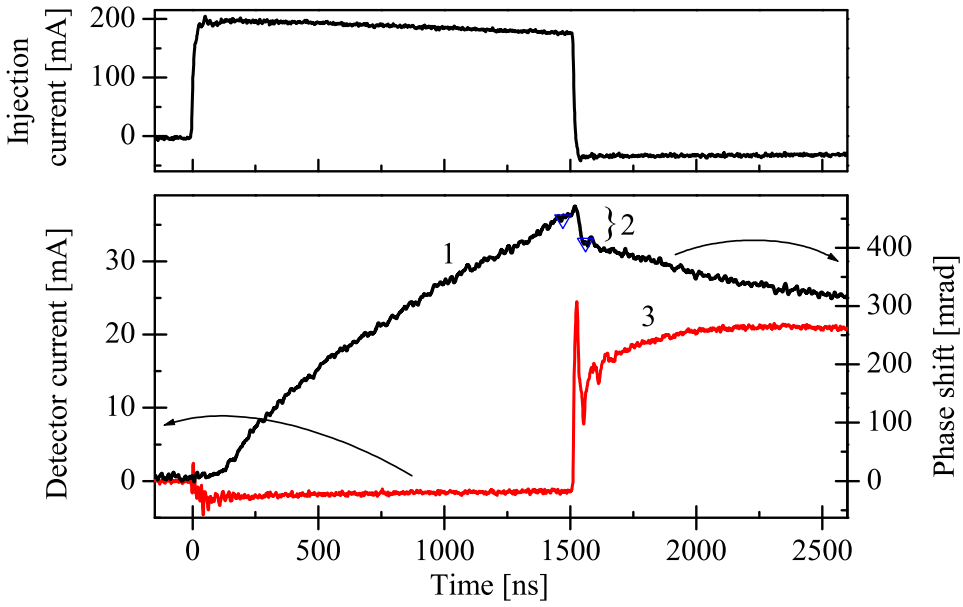


Figure 3.50: Phase shift transient at center of the detector structure showing a significant drop at the terminating edge of the injection pulse (beginning of latch-up). The instants $t = 1470\,\text{ns}$ and $t = 1560\,\text{ns}$ are marked with triangles at the phase shift transient.

originating from the activated SCR (see high detector current "3" after the injection pulse). The falling slope of the phase shift transient after the injection pulse indicates cooling of the total structure (total heating during injection is higher than self-heating of the triggered SCR).

The phase shift measurement across the structure (along the dashed line in Figure 3.5) is shown in Figure 3.51 at $t = 100\,\text{ns}$, short before latch-up (at $t = 1470\,\text{ns}$) and in latch-up (at $t = 1560\,\text{ns}$). The excess carrier contribution of the injection pulse is outlined with the 100 ns line.

After the termination of the injection pulse a sudden increase of phase shift ("1") is visible at the injector area due to cease of injected carriers (similar as observed at negative injector structures). During latch-up a sudden *decrease* of phase shift ("2") is observed at the detector area due to additional carriers from the activated SCR.

Figure 3.52 shows the two-dimensional phase shift snapshots before (a) and after (b) triggering latch-up. A significant drop of phase shift after triggering the SCR is visible at the center of the latch-up detector.

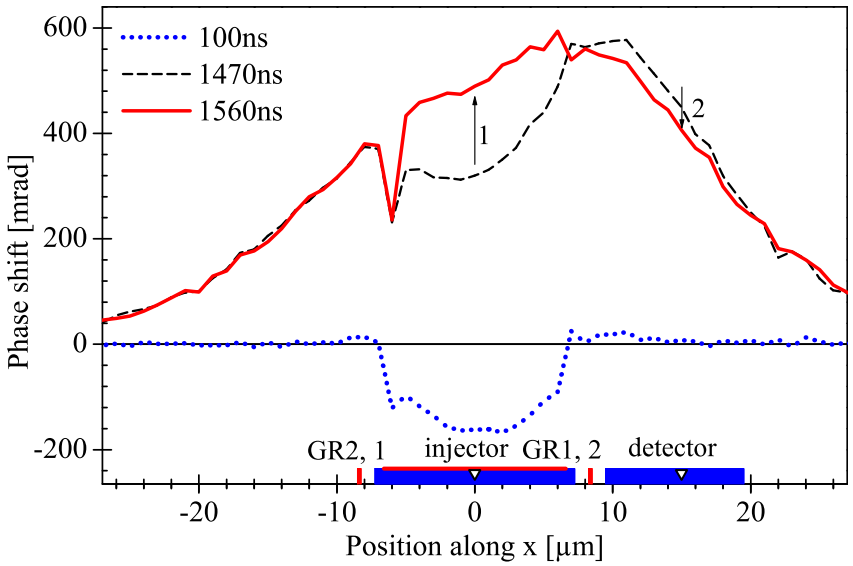
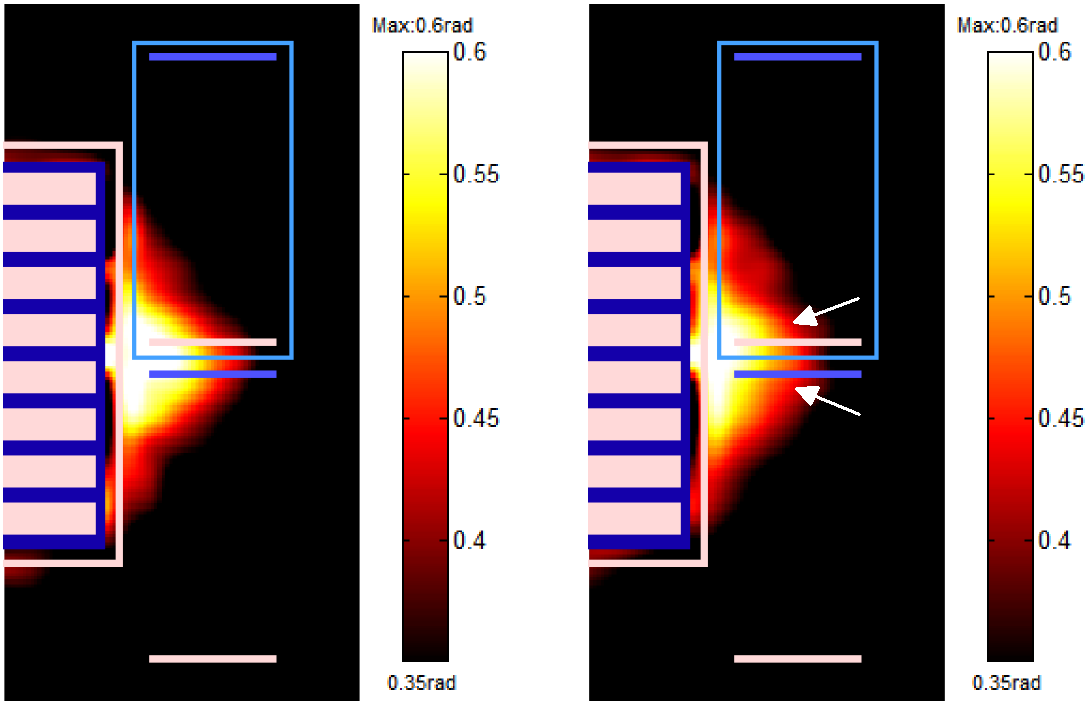


Figure 3.51: TIM phase shift scan across the structure showing phase drop ("2") at the detector structure during latch-up.



(a) (b)

Figure 3.52: Two-dimensional TIM phase shift scan with layout overlay (a) short before latch-up ($t = 1470\,\text{ns}$) and (b) during latch-up ($t = 1560\,\text{ns}$) showing a significant phase shift drop at the center of the detector structure after triggering the SCR.

3.1.5 Investigation of proximity effects

For the design of latch-up protection concepts proximity of the injector structure and the parasitic SCR structure (detector) have an impact on its latch-up trigger current. Therefore, several cases of layouts containing asymmetrically placed guard-rings were investigated by TIM under negative injection[30]. A test structure and a commercial I/O cell are discussed as representative examples. Other investigated I/O cells are investigated as well – their results are presented in [106].

Previous section showed that roughly $-20\,\mathrm{mrad}$ phase shift is already latch-up critical in this 90 nm CMOS technology for the worst-case parasitic SCR structure (see phase shift measured slightly below latch-up condition in Figure 3.22). Thus, it is possible to estimate from phase shift measurements at which areas of the chip layout latch-up sensitive structures should be avoided. Such information allows the optimization of floor plans and latch-up protection structures.

Test structure case

The extensive TIM scan of a ggNMOS injector (similar to the *large* latch-up test structure) under $-200\,\mathrm{mA}$ injection is shown in Figure 3.53 at $t = 1000\,\mathrm{ns}$. This instant represents nearly steady state excess carrier condition (see also exemplary excess carrier component $\Delta\varphi_{\mathrm{fc}}$ in Figure 3.17). In regions with phase shift around $-20\,\mathrm{mrad}$ significant excess carriers are present and worst-case parasitic SCRs might be activated[31]. The biased third (n^+) guard-ring remarkably reduces excess carriers reaching the detector structure (see position "1").

The gaps between the n^+ guard-ring structures (see dashed ellipses) do not cause significant current crowding in substrate. Based on the phase shift data a video animation is made to monitor the spreading process of injected carriers in top view [109].

Investigation of a commercial I/O cell

The effect of biased guard-ring constructs on the penetration of substrate currents into neighboring regions is analyzed with $-200\,\mathrm{mA}$ pulses. The investigated I/O cell is in power-down state (all gates are turned off), thus whole current is injected to the substrate through n^+ diffusions of NMOS drivers and ESD protection elements. A schematic cross

[30] Previous sections showed that for p substrate negative external injection is worse than positive.
[31] E.g. due to temperature increase or slightly stronger injection.

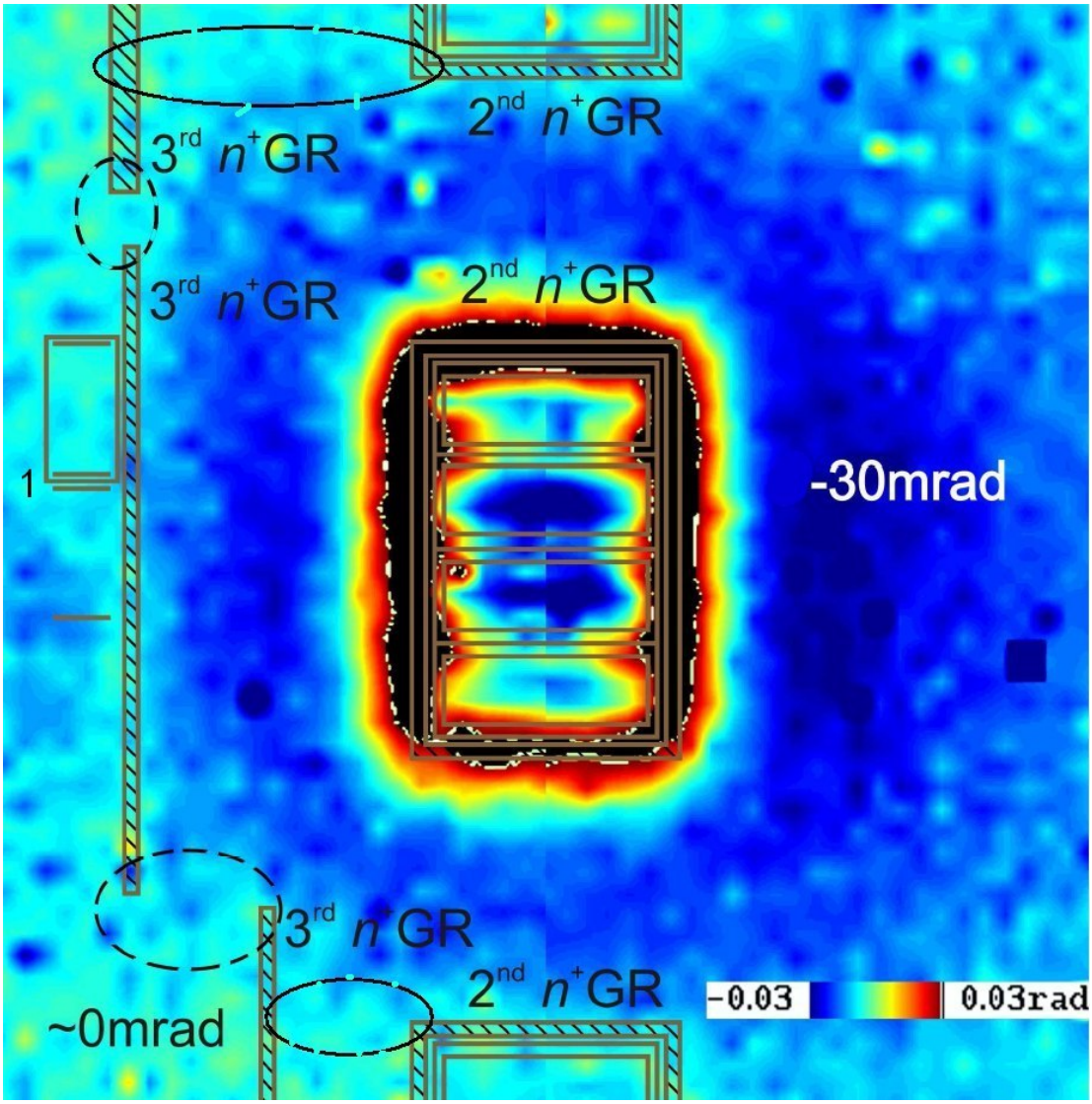


Figure 3.53: Two-dimensional TIM phase shift scan (interpolated, top view – labels see Figure 3.4) of an injecting ggNMOS showing asymmetrical spreading excess carriers. The snapshot is composed of two scans at $t = 1000\,\mathrm{ns}$ under $-200\,\mathrm{mA}$ injection and $3\,\mathrm{V}$ n^+ guard-ring biasing. Dashed ellipses mark gaps in the n^+ guard-ring structures. Black color indicates phase shift exceeding $+30\,\mathrm{mrad}$.

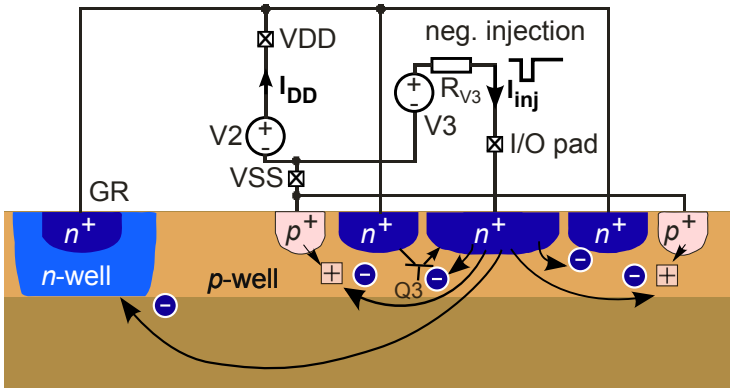


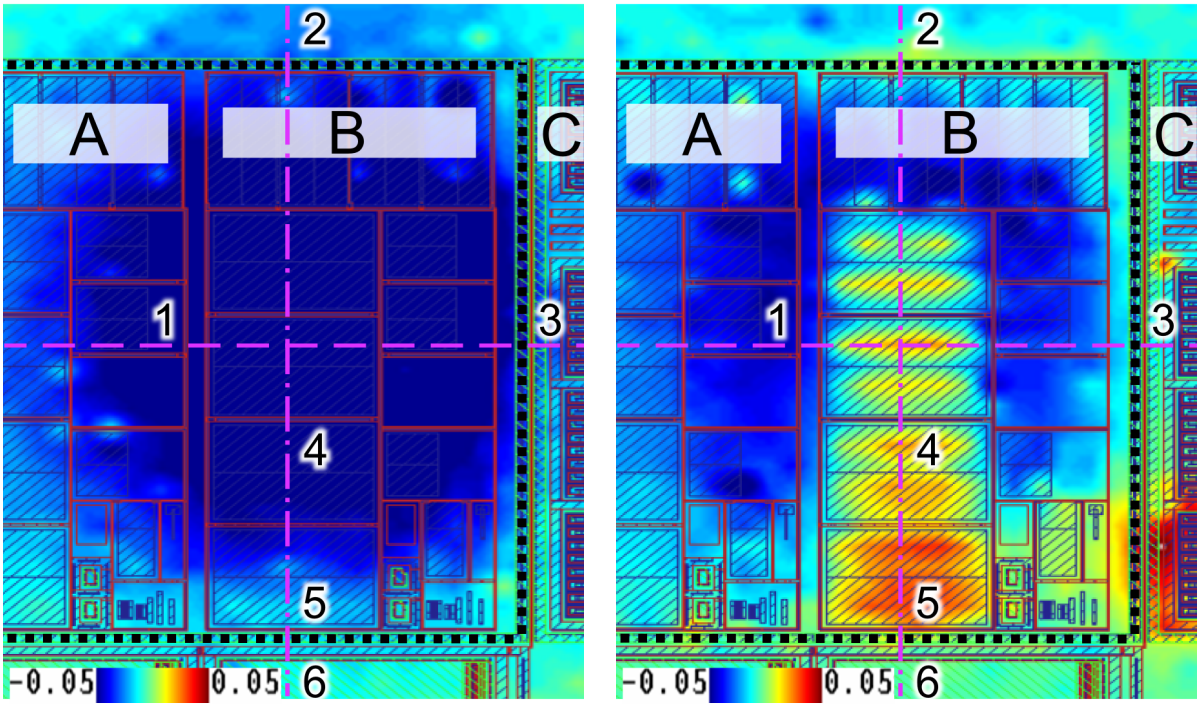
Figure 3.54: Schematic cross section of the injecting structure with grounded p^+ and biased n^+ diffusions. The injecting n^+ diffusion forms with the p well and n^+ diffusion connected to *VDD* the intrinsic *npn* transistor Q_3.

section of the injecting structure with an n^+ guard-ring is shown in Figure 3.54.

The two-dimensional phase shift scan at $t = 1000$ ns is shown in Figure 3.55 for (a) floating and (b) 3 V biased *VDD* pad. In the floating case excess carriers spread from the stressed I/O cell ("B") to the left (see position "1"), where the next I/O cell ("A") is placed, to the top (see position "2") and right side (cell "C", see position "3").

Biasing the *VDD* pad (n^+ guard-rings and several n^+ diffusions) with 3 V (Figure 3.55b) significantly decreases the excess carrier concentration in the area of the stressed I/O cell and behind the guard-rings on top (see "2") and right hand side (see "3") with respect to the floating case. Inside the I/O cell area heating is clearly visible (see position "4"). This heating occurs at n^+ diffusions (collector of parasitic transistor Q_3), which are connected to the *VDD* pad. These biased n^+ diffusions collect injected electrons – they act like additional guard-rings. This leads to less substrate current (less free carrier contribution to the measured phase shift) and to higher heating. The biased n^+ guard-rings (see "2" and "3") reduce further substrate currents spreading outside the stressed I/O cell. Logic circuit could be placed without any additional guard-rings in areas where the phase shift is above -20 mrad.

The TIM scans along the dashed lines of Figure 3.55 are shown in Figure 3.56 at $t = 300$ ns and $t = 1000$ ns. They show that at cell ("A") the free carrier contribution is significantly reduced by biasing the *VDD* pad (see position "1"), but it is anyway latch-up critical – see dotted line at -20 mrad. A worst-case SCR structure would latch here. The phase shift transients for the floating case show negligible heating and the minimum is at the pulse end – similar as shown with curve n_3 in Figure 3.18. In the biased case, the phase shift transients show also heating and the phase shift minimum is around $t = 300$ ns –



(a) (b)

Figure 3.55: Two-dimensional TIM phase shift scan (interpolated, top view – for legend see Figure 3.7b) of a commercial I/O cell showing phase shift under −200 mA injection at $t = 1000$ ns. Blue color indicates negative phase shift corresponding to excess carrier concentration in substrate. The locations of n^+ guard-rings at *VDD* are marked with dotted lines. *VDD* pad is (a) floating, (b) biased with 3 V.

similar as shown in Figure 3.17.

The TIM scans along the dash-dot lines of Figure 3.55 are shown in Figure 3.57 at $t = 300$ ns and $t = 1000$ ns. They show that on the bottom side of the I/O cell the free carrier contribution is not latch-up critical regardless of guard-ring biasing (see phase shift at position "5").

The reason for this low excess carrier concentration at the bottom side is the nearby n well for PMOS transistors, which is located directly behind the guard-ring. This n well collects electrons as well (see phase shift at position "6"). Thus, the guard-ring ("5") placed on the bottom side of the I/O cells could be removed from the design and the I/O cell topology could be simplified.

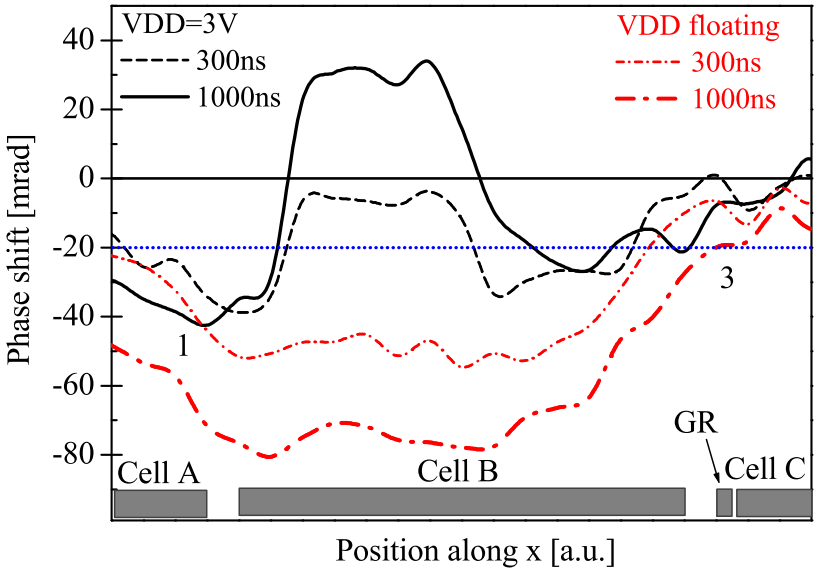


Figure 3.56: TIM scans along the dashed lines of Figure 3.55 at $t = 300$ ns and $t = 1000$ ns. The labels correspond to Figure 3.55.

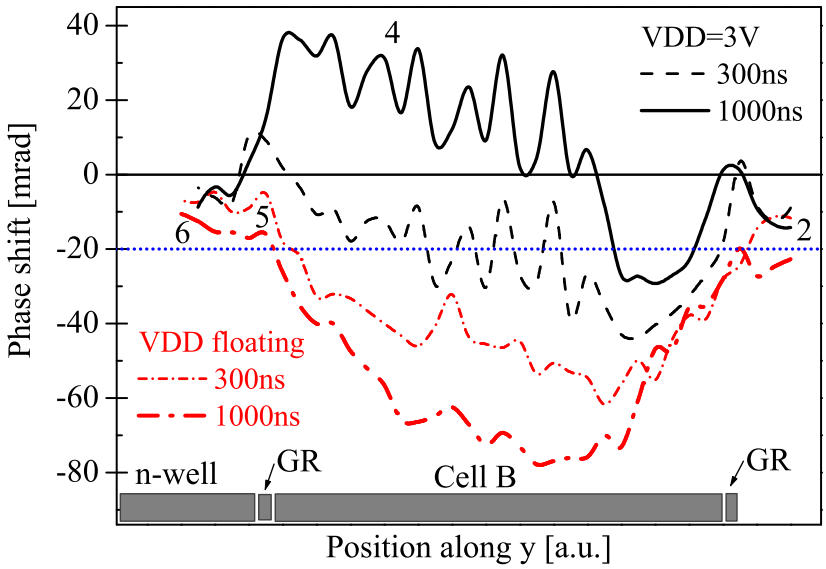


Figure 3.57: TIM scans along the dash-dot lines of Figure 3.55 at $t = 300$ ns and $t = 1000$ ns. The labels correspond to Figure 3.55.

3.2 Latch-up root cause in a commercial power control device

A case study of a transient induced latch-up problem in a commercial product is presented [111]. The commercial power control device failed due to latch-up during harsh reliability tests with spikes on the positive supply pin. During the reliability tests the current through the device is not externally limited, thus latch-up destroys several metal tracks on the chip and the original latch-up site is not obvious. Therefore, a controlled transient latch-up test is developed and the onset of the transient latch-up problem is analyzed in detail.

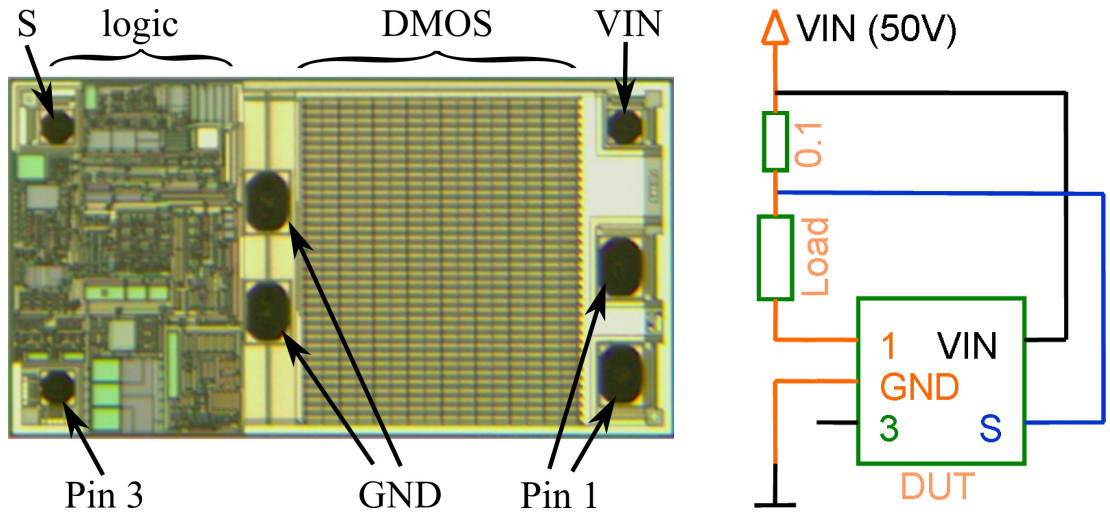
3.2.1 Description of investigated devices

The investigated power control integrated circuit is shown in Figure 3.58a. It is fabricated by *Diodes Incorporated* [112] in a 60 V, 0.8 µm BiCMOS (bipolar and CMOS) process in bulk silicon and packaged in a TSOT23-5 case. The size of the die is 2100 µm × 1200 µm, where half of the die is a power DMOS device and the rest is CMOS control logic and drive circuitry. The chip is designed to control the current through a user defined load. It is based on a power DMOS switch and a high side output current sensing circuit, which is shown in Figure 3.58b.

To access the silicon backside of the investigated surface mounted devices, the leads of the package are flattened. The package is opened from backside and the silicon substrate – as well as the package – is grinded and polished to a die thickness of 220 µm to get a sufficiently bright infrared image for optical investigations from the device backside. The opened chip is soldered upside-down on a test board to make access to the back of the chip during its operation possible (see Figure 3.59a). Figure 3.59b shows the mounted test board with the soldered chip in the scanning TIM setup.

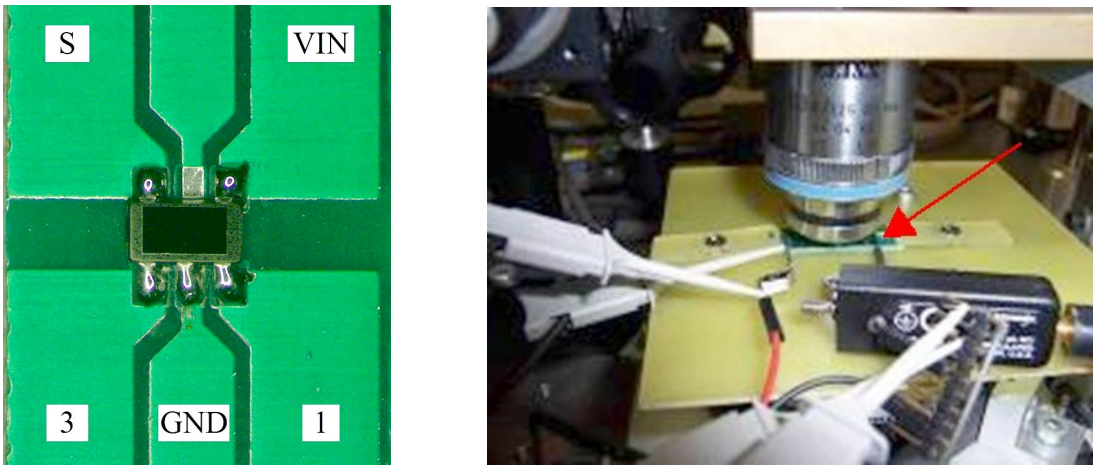
3.2.2 Experimental details

The observed latch-up event during the reliability tests is destructive, therefore a non-destructive transient latch-up test system for negative pulses on the supply line is designed and incorporated in the scanning TIM setup.



(a) (b)

Figure 3.58: (a) Mirrored top view of die. (b) Typical schematic of the power control device, which is based on a power DMOS switch at pin 1 and a high side output current sensing circuit ($R_{\text{sense}} = 0.1\,\Omega$).



(a) (b)

Figure 3.59: (a) Backside opened power control device soldered upside-down at the test board. (b) Mounted test board (see arrow) in the scanning TIM setup.

Stressing scheme

The schematic diagram of the created latch-up test system is shown in Figure 3.60. To emulate transient latch-up events due to short negative pulses applied to a 50 V supply voltage, a programmable solid-state pulse generator with a baseline option (*Agilent 8114A*) is used. The pulse generator provides the 50 V baseline (V_{high}) with a superimposed downward pulse resulting in a second (lower) voltage level (V_{low}). The voltage levels and their durations are programmable. The V_{low} setting is varied from -1.5 V to $+6.5$ V, providing thus negative and positive voltage levels to the input voltage pin (VIN) and current sense pin (S) of the device under test. The total current is measured at the ground pin (GND) using a *Tektronix CT1* current transducer. The current limiting series resistor (250 Ω) is introduced to avoid damage to the chip during latch-up. After a few milliseconds the baseline voltage of the pulse generator is set to zero in order to stop the latch-up event and to discharge the sample before the next latch-up test.

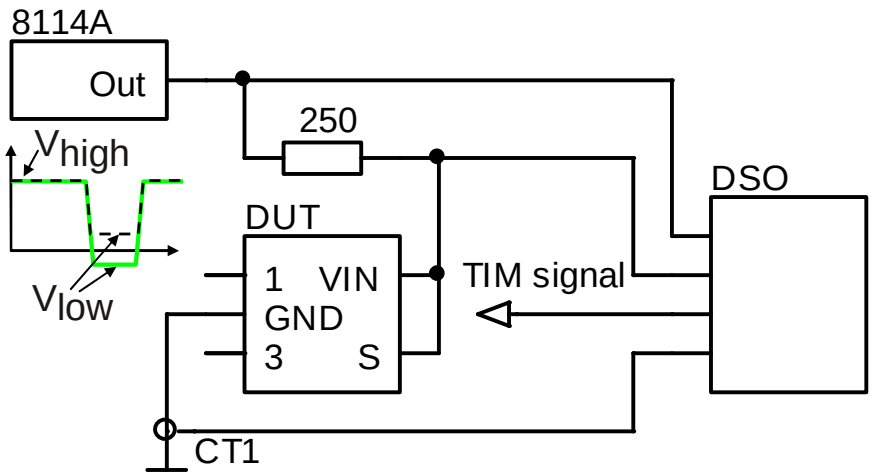


Figure 3.60: Schematic diagram of the transient latch-up setup with *Agilent 8114A* solid-state pulse generator and four channel digital sampling oscilloscope (DSO).

Refocusing system

The TIM scanning of the large chip area requires a very precise alignment of torsion and inclination angles of the sample in the setup to avoid defocusing of the laser beam during scanning long distances. Therefore, an automated beam refocusing[32] system is developed. The refocusing system requires *teach-in programming* at three good reflecting points. After this calibration it calculates for the current position a vertical correction

[32] Auto-focus might have problems at edges (scattered laser beam) and at non-reflecting areas of the chip. The global maximum of the reflected beam is at the silicon surface and not in the active layer.

value and applies the corresponding voltage to a piezoelectric actuator. The compensation of torsion angles is realized by *teach-in programming* of a second coordinate system with three orthogonal points in the IR image and corresponding matrix operations [7]. The modified microscope objective holder and a screenshot of the enhanced scanning software *heterodyne.vi* [108] are shown in the appendices in Figures B.1 and B.2.

3.2.3 Latch-up identification

The voltage and current transients for a non-latching stress pulse of 200 ns duration are shown in Figure 3.61. The current flow and power dissipation stops after $t = 400$ ns (see "1"). If the pulse on the supply is slightly more negative, the device latches after the 200 ns pulse. Figure 3.62 shows the voltage and current transients for a latching stress pulse, where the current settles at 150 mA due to the current limiting series resistor (see "1"). During latch-up the voltage at VIN drops to 2.5 V.

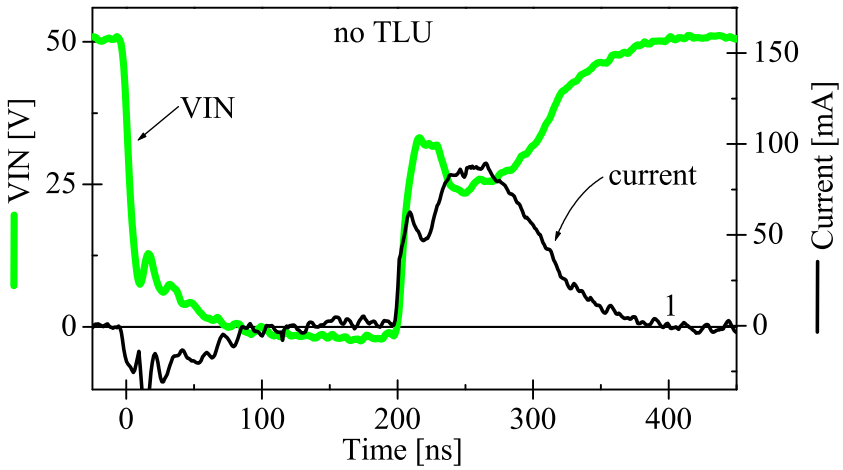


Figure 3.61: Current and voltage waveform during a non-latching 200 ns stress pulse showing no current flow after $t = 400$ ns. $V_{\text{high}} = 50$ V and $V_{\text{low}} = -2$ V.

3.2.4 Effect of pulse duration on transient latch-up

The effect of pulse duration on latch-up trigger voltage is investigated in Figure 3.63. For long pulses the circuit latches for negative V_{low} voltage values at the VIN pin. For pulses shorter than ~135 ns even positive V_{low} voltage on the VIN pin can trigger latch-up, thus the triggering mechanism seems to change – this will be analyzed in Section 3.2.6. The pulse duration for latch-up triggering with the highest V_{low} setting of the pulse generator (6.5 V) is 75 ns (see "A" in Figure 3.63). At this pulse duration the circuit latches for

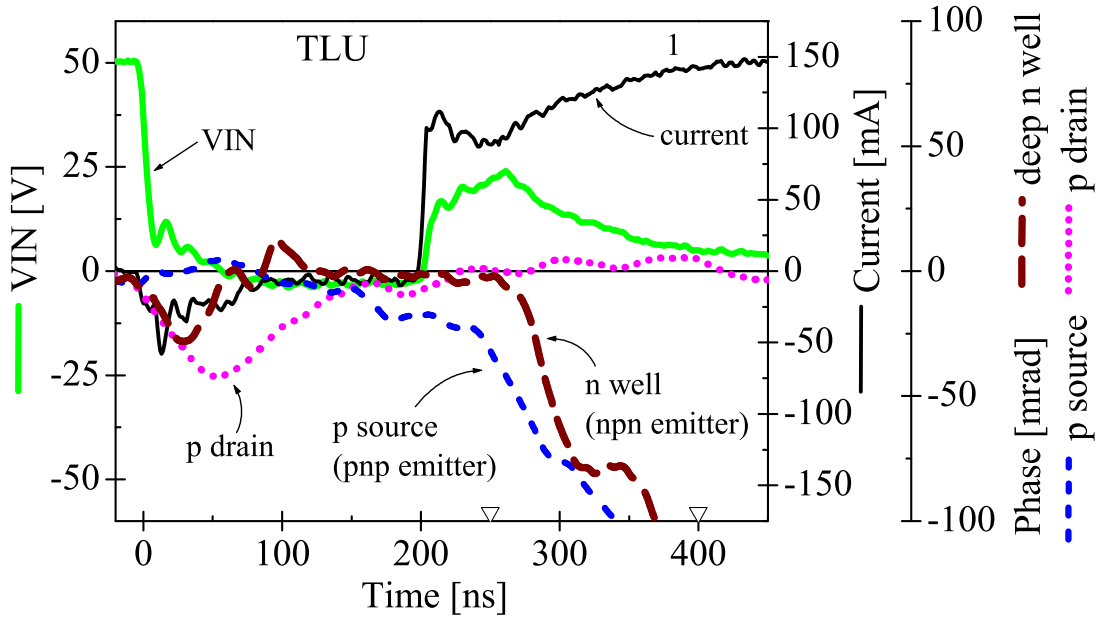


Figure 3.62: Current, voltage and phase shift waveforms during latch-up stress with 200 ns pulses. The *pnp* transistor is earlier activated than the *npn* transistor. The instants of the 2D phase cross sections are marked with triangles. $V_{\text{high}} = 50\,\text{V}$ and $V_{\text{low}} = -2.4\,\text{V}$.

+4.2 V at the VIN pin. The corresponding voltage transient is shown in Figure 3.64. For pulses shorter than 75 ns the V_{low} setting of the pulse generator has to be again decreased to get sufficient amount of injected carriers for triggering latch-up.

As shown later, negative and positive stress voltages at the VIN pin lead to different latch-up triggering mechanism. Thus, the next results are split according to the polarity of V_{low}.

3.2.5 Latch-up onset under negative stress voltages at VIN

An overlay of the infrared emission microscopy image obtained from the front side during latch-up with 200 ns pulses and a repetition rate of 1 kHz is shown in Figure 3.65a [111]. The infrared emission image is acquired at *Diodes Incorporated* with a *Carl Zeiss LSM310* laser scanning microscope and a cooled *Photometrics AT200* CCD camera [112].

The infrared emission microscopy highlights several spots on the chip, but they are not part of the typical "*burn*" pattern of the latch-up damaged chips. This leads to speculations, that infrared emission from bond pad ESD diodes might be obscured by the metal layers. The top view of a latch-up failure signature is shown in Figure 3.65b. The infrared

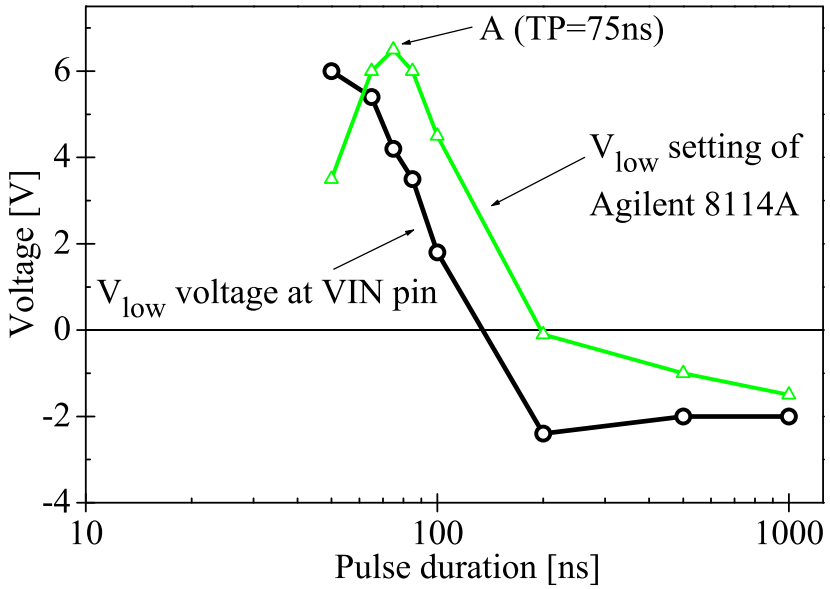


Figure 3.63: Effect of pulse duration on latch-up trigger voltage. For pulses shorter than ∼135 ns even positive voltage at the VIN pin can trigger latch-up.

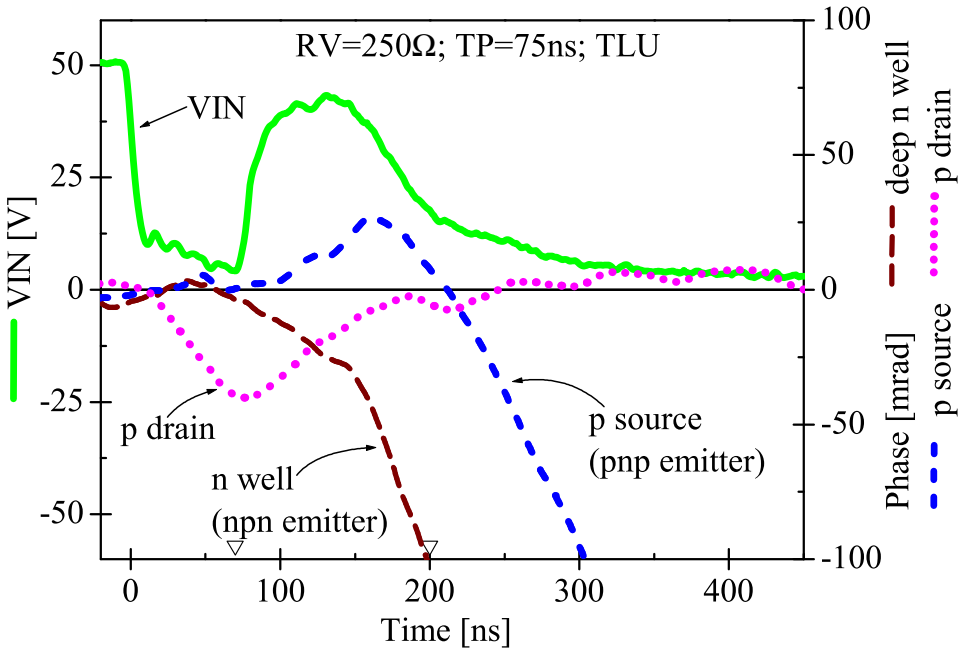
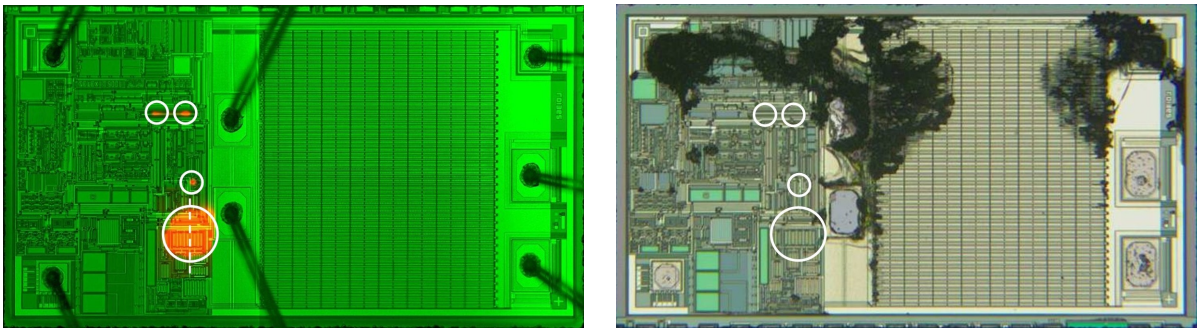


Figure 3.64: Current, voltage and phase shift waveforms during latch-up stress with 75 ns pulses. The *npn* transistor is activated earlier than the *pnp* transistor. The instants of the 2D phase cross sections are marked with triangles. $V_{\text{high}} = 50\,\text{V}$ and $V_{\text{low}} = +4.2\,\text{V}$.

emission microscopy does not show how the chip latches in detail and cannot tell us which structures exactly form the activated parasitic SCR structure. To gain full insight into the transient triggering mechanism of the activated SCR and the involved carrier injecting junctions, optical investigations from the back of the device are performed in-situ with the scanning TIM setup.



(a) (b)

Figure 3.65: (a) Mirrored IR emission image with top view overlay of the chip during latch-up with 200 ns pulses and a repetition rate of 1 kHz [111]. The dashed line marks the cross section of the found parasitic SCR structure. The circles mark IR emission spots. (b) Mirrored top view of the die with typical latch-up failure signature. The circles mark the position of the IR emission spots, which are obviously not part of the typical "*burn*" pattern.

The TIM scan across the largest IR emitting area (dashed line in Figure 3.65a) shows in Figure 3.66 strong carrier injection (negative phase shift) at position "A" (parasitic *pnp* transistor), high heating at "B" and carrier injection at "C" (parasitic *npn* transistor).

The corresponding schematic device cross section is shown in Figure 3.67a. It shows from left to right the PMOS transistor M_1, a surrounding p guard-ring and a nearby deep n well (deep n tub). The p guard-ring and the grounded deep n well are normally employed to prevent latch-up, however in this case they complete a parasitic SCR structure. The emitter of transistor Q_1 is the p source diffusion of the PMOS transistor M_1, the base is the shallow n well and the collector is the p substrate (p guard-ring). The emitter of transistor Q_2 is the deep n well (deep n tub), the base is the p substrate and the collector is the shallow n well. The layout in the vicinity of the identified SCR is shown in Figure 3.67b with the parasitic *pnp* (Q_1) and *npn* (Q_2) transistors.

A two-dimensional TIM scan of the investigated area is shown in Figure 3.68a. It shows the free carrier distribution during the beginning of latch-up at $t = 250$ ns. The TIM experiments reveal clearly the source diffusions of the PMOS transistor M_1 as carrier injector (negative phase shift, blue area). This indicates that the parasitic *pnp* transistor

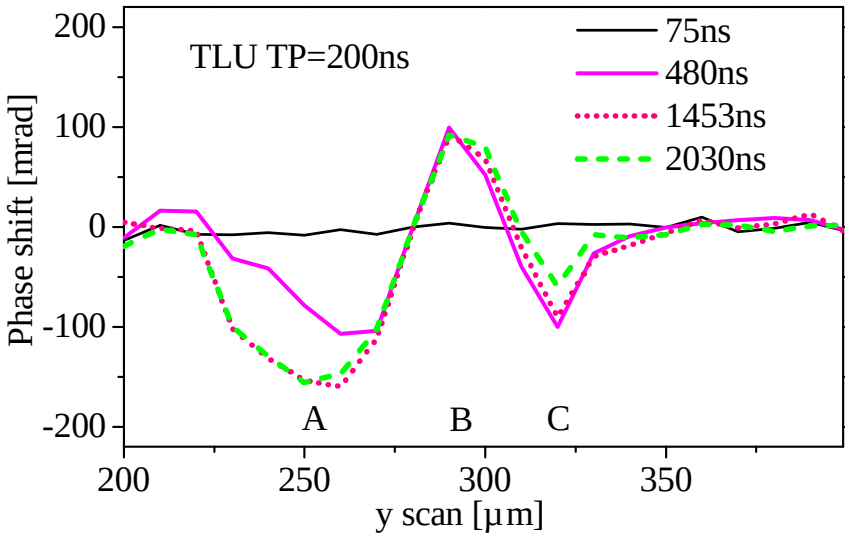
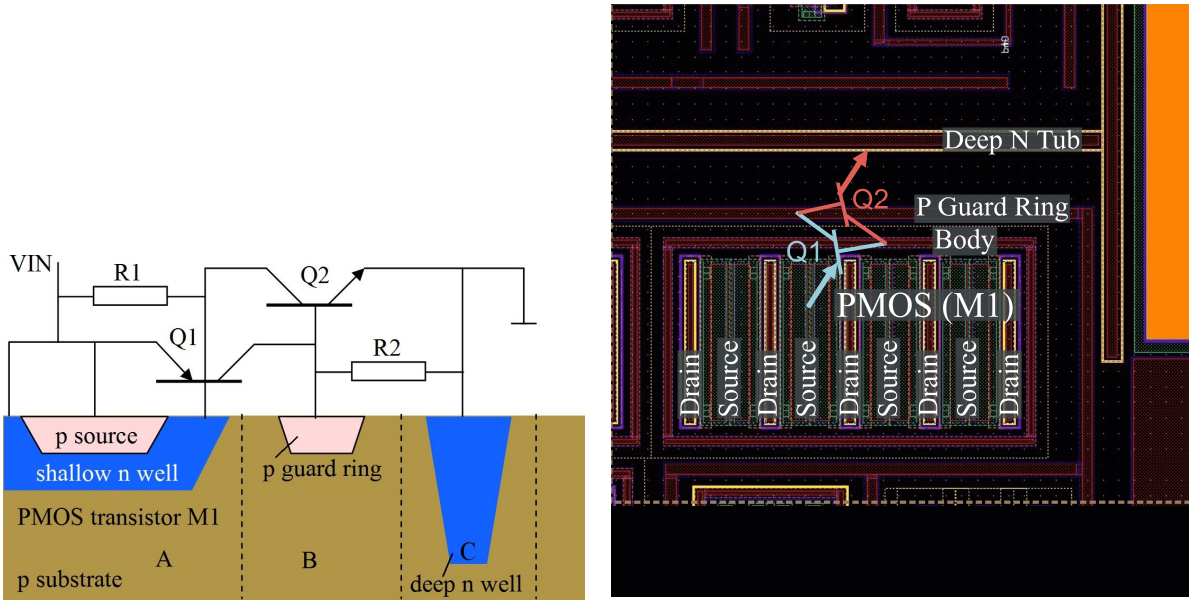


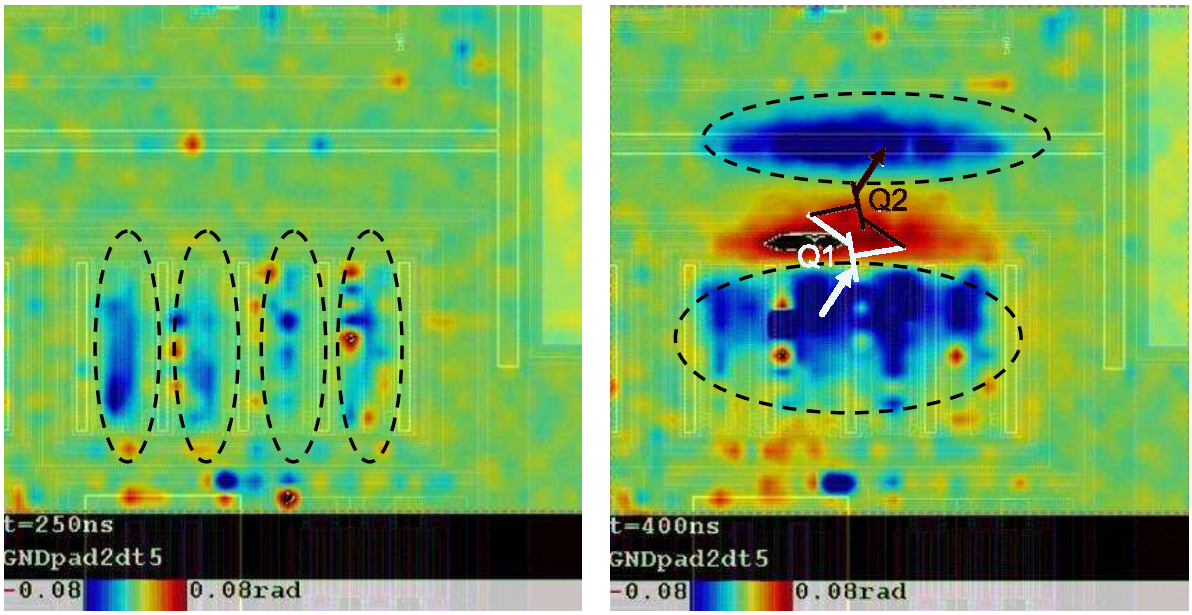
Figure 3.66: Phase shift across the SCR during latching 200 ns stress pulses showing strong carrier injection at the emitters (position "A" and "C") and heating at the collector area "B".



(a) (b)

Figure 3.67: (a) Cross section of the active area with parasitic *pnp* (Q_1) and *npn* (Q_2) transistors. (b) Layout of the investigated area with PMOS (M_1), parasitic *pnp* (Q_1) and *npn* (Q_2) transistors. The emitter of transistor Q_1 is the *p* source of M_1, the base is the shallow *n* well and the collector is the *p* substrate (*p* guard-ring). The emitter of transistor Q_2 is the deep *n* well (deep *n* tub), the base is the *p* substrate and the collector is the shallow *n* well. The black stripe at the bottom is added to get the same scale as in the other overlay images (Figures 3.68–3.70).

Q_1 is active. The voltage drop in the shallow n well is due to the reverse recovery current[33] during the rising edge of the stress pulse. Later the *npn* transistor Q_2 becomes active, causing the SCR to latch.



(a) (b)

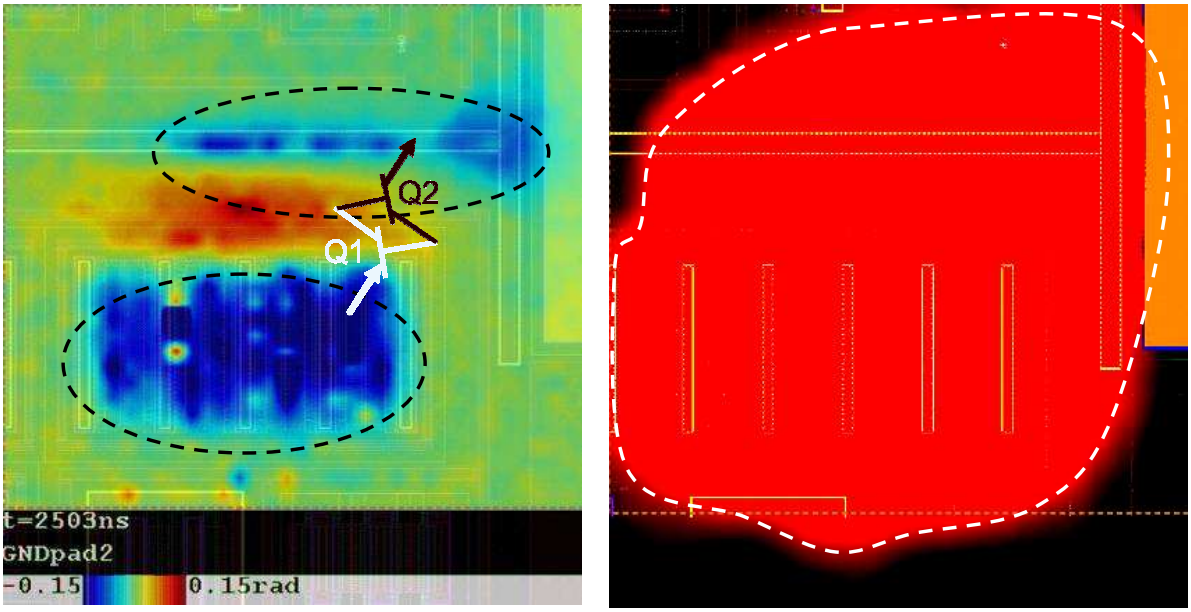
Figure 3.68: Two-dimensional TIM phase map with layout overlay of active area during −2.4 V 200 ns latch-up stress pulses. (a) At $t = 250$ ns showing four areas (dashed ellipses) of carrier injection (blue) at the source diffusions of PMOS transistor M_1. Parasitic *pnp* transistor is active, but not the parasitic *npn* transistor. (b) At $t = 400$ ns showing two active carrier emitters (dashed ellipses, blue area). Black color indicates phase shift exceeding 80 mrad.

Figure 3.68b shows the excess carrier and heat distribution during the latched state at $t = 400$ ns. It shows the PMOS transistor M_1 as carrier emitter (negative phase shift, blue area) of the *pnp* transistor and the p guard-ring as collector, where strong heating occurs (positive phase shift). The deep n well acts as second emitter (upper blue area, see upper dashed ellipse) and completes the parasitic SCR structure. The corresponding phase shift transients related to the latch-up pulse are shown in Figure 3.62, where the negative phase shift at p source shows, that the *pnp* transistor is activated first. Figure 3.69a shows an increase of the active area towards the corner of the deep n well (deep n tub) during latch-up due to heating. Considering this increase the active area matches to the obtained infrared emission microscopy image shown in Figure 3.69b.

Several other locations (i.e. the bond pad ESD diodes) on the chip are investigated as

[33] Collection of electrons remaining from forward current flow at the p substrate / shallow n well junction.

well, but no further significant carrier injection sources are found.



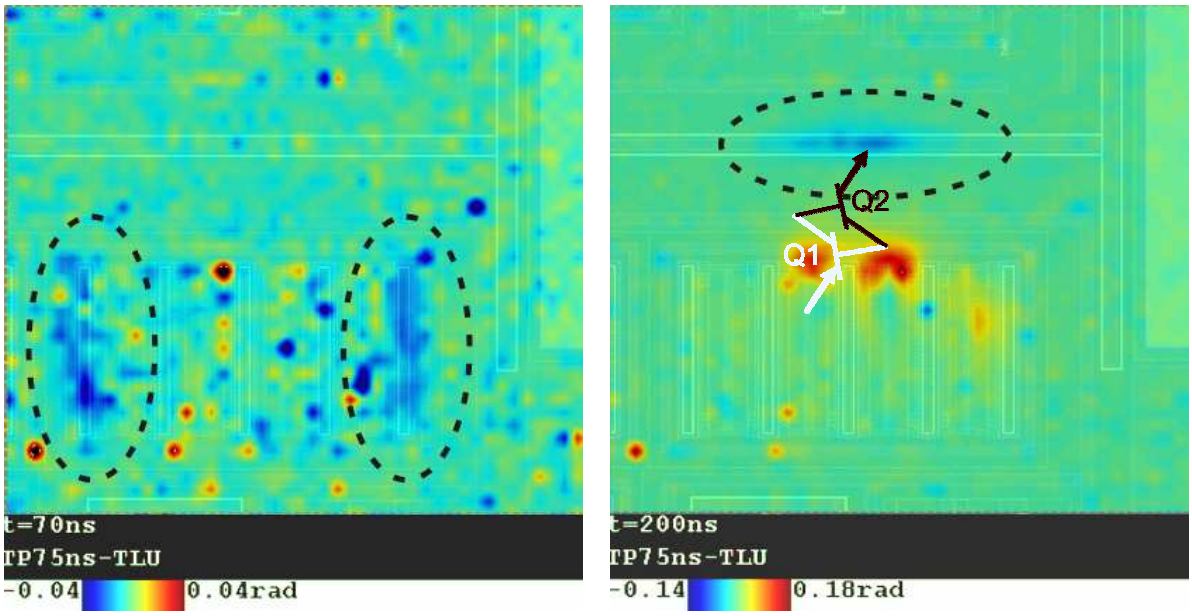
(a) (b)

Figure 3.69: Two-dimensional TIM phase map with layout overlay of active area during −2.4 V 200 ns latch-up stress pulses. (a) At $t = 2.5\,\mu s$ showing movement of active area (dashed ellipses, blue area) to the corner of the deep n well. (b) IR emission image with layout overlay of active area during latch-up. The dashed line marks the IR emission area.

3.2.6 Latch-up onset under positive stress voltages at VIN

The two-dimensional TIM scan at $t = 70\,ns$ during stress pulses with 75 ns duration (the device is not in latched state at this time) is shown in Figure 3.70a. It shows two areas with high excess carrier concentration (see dashed ellipses), which assist the latch-up process at short pulses. The reason might be forward biasing of the p drain / body diode (shallow n well) of the PMOS transistor for n well voltages below the drain potential (about 15 V). The schematic cross section of the PMOS transistor M_1 with parasitic *pnp* transistor Q_3 is shown in Figure 3.71. The activated parasitic *pnp* transistor Q_3 injects holes into substrate. The increased substrate potential could activate the *npn* transistor Q_2 of the SCR. After discharge of the load capacity on the drain, the injection of holes stops. This is also visible in the corresponding phase shift transient at the outer drain diffusions shown in Figure 3.64 (see phase shift at p drain).

The two-dimensional TIM phase map in Figure 3.70b shows the excess carrier distribution



(a) (b)

Figure 3.70: Two-dimensional TIM phase map with layout overlay of the active area during +4.2 V latch-up stress pulses with 75 ns duration. (a) At $t = 70$ ns showing two significant areas (dashed ellipses) of carrier injection (blue) at the outer drain diffusions of transistor M_1. (b) At $t = 200$ ns showing one area of carrier injection (dashed ellipse) at the deep n well. Parasitic npn transistor Q_2 is active, but not the parasitic pnp transistor Q_1. The red areas indicate heating at the shallow n well (collector of npn transistor Q_2).

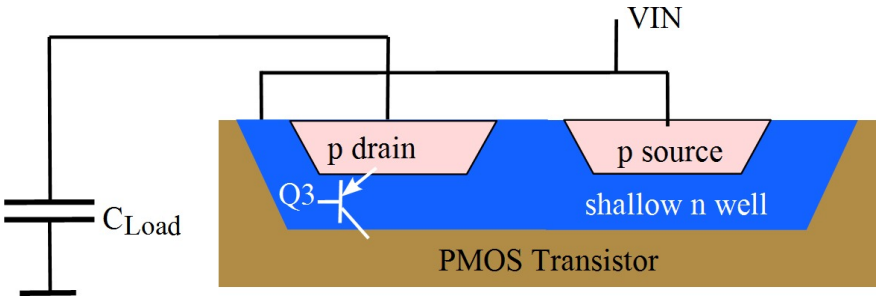


Figure 3.71: Schematic cross section of PMOS transistor M_1 with capacitive load (C_{Load}). The p drain / n well junction is forward biased for VIN voltages below the voltage of the capacitive load, enabling Q_3 to inject holes into substrate.

at $t = 200\,\text{ns}$ of 75 ns stress pulses. It shows the activated parasitic *npn* transistor Q_2 as carrier emitter (negative phase shift, blue area) and heating at its collector area. The corresponding phase shift transients related to the latch-up pulse are shown in Figure 3.64. The negative phase shift at the deep *n* well shows, that now the *npn* transistor Q_2 is activated first. Opposite behavior was observed for the 200 ns pulses, because the injected carriers of the discharge current are vanished before the terminating edge of the stress pulse and consequently they cannot activate the parasitic *npn* transistor (see *p* drain in Figure 3.62).

3.2.7 Improvement of the latch-up robustness

Exemplarily, focused ion beam surgery is employed to eliminate the parasitic SCR structure by disconnecting the grounded deep *n* well (emitter of parasitic *npn* transistor Q_2) and therefore to improve the latch-up robustness. Alternatively the use of silicon-on-insulator substrates eliminates substrate currents and consequently the latch-up problem.

3.3 Summary of latch-up investigations

The scanning TIM method was extended with a facility for transient latch-up testing with multiple supply domains to perform detailed analysis of the excess carrier diffusion under transient current injection in silicon devices. Further enhancements compensated for sample misalignments like torsion and inclination angles – thus the mechanical alignment of the device under test was greatly facilitated. The introduced automated laser beam refocusing system allowed the scanning of several millimeters without defocusing and enabled investigations of large circuits, such as the presented commercial case studies ($\sim$4 000 000 µm^2).

Negative as well as positive substrate currents were investigated as a trigger for possible *external* transient latch-up at special test structures with floating detector (SCR) supply domain. Further, case studies of commercial I/O cells and a power control device were performed. The transient excess carrier concentration was studied for various layout configurations and injection carrier types and the results were complemented with device simulations. The excess carrier density at the detector structure and therefore its sensitivity to latch-up was found to strongly depend on guard-ring configurations and on the distance of the SCR structure to the injecting junction. Layout configurations with both SCR-wells facing to the injector structure were most sensitive due to the short distance between the injector and the *pnpn* junction. Heat spreading associated with current flow through the injector junction was identified as an additional factor, which lowers latch-up trigger currents for long injection pulses. The measured and simulated phase shifts matched well. A strong impact of the polarity of injected currents on the latch-up trigger current was proven.

Negative injection at external latch-up test structures. Negative injection currents applied on an *n* well / *p* substrate junction caused a permanent increase of the minority carrier (electron) concentration in *p* substrate during the injection pulse. This led to an increasing current in the latch-up detector. Latch-up onset occurred usually at the terminating edge of the injection pulse, for higher injection amplitudes latch-up triggered already during the injection pulse. Biasing the guard-ring constructs substantially reduced the excess carrier concentration and therefore the latch-up sensitivity of the test structures was lowered. It was found, that in this CMOS technology, a phase shift (excess carrier concentration) of -0.02 rad was already critical for activation of worst-case SCR structures. The effective minority carrier (electron) lifetime near the injector and guard-rings was $\tau_{n2} = 350$ ns (480 ns for floating guard-rings) and far from injector $\tau_{n3} = 950$ ns.

Guard-ring biasing reduced the fitting coefficient (amplitude factor) of the excess carrier contribution in near region about 33% and far region about 27%. The carrier diffusion process could be modeled with a short diffusion length $L_{n1} = 18\,\mu m$ (23 µm for floating guard-rings) in a layer near the surface – which was affected by guard-rings and higher doped wells – and a long diffusion length $L_{n2} = 55\,\mu m$ in the low doped substrate.

Positive injection at external latch-up test structures. Positive injection currents applied on a parasitic *pnp* transistor caused an increase of the local substrate potential. Excess carriers were observed only in direct vicinity of the injector. Saturation of the injector transistor led to forward-biasing of the *p* substrate / detector *n* well junction and therefore to a *negative* contribution to the total detector current, which impeded latch-up during the injection pulse. Consequently, latch-up was observed only after the terminating edge of positive injection pulses. The latch-up onset (activation of the SCR) manifested itself as an abrupt phase shift decrease (increase of carrier density) in the TIM scans. The latch-up trigger current characteristics for positive injection showed 2–3 times higher current amplitudes compared to the corresponding negative injection structure. This was related to the limited injection efficiency of the saturated positive injector structure and the short diffusion length of excess holes (majority carriers, Debye length $L_{Dp} \simeq 120\,nm$) in *p* substrate and their short dielectric relaxation time ($\tau_{dp} \simeq 14\,ps$). Therefore, in this CMOS technology positive external injection current was less critical than negative. The lifetime of minority carriers (excess holes) in the *n* well was $\tau_p \simeq 25\,ns$, which could be attributed to a diffusion length of $L_p \simeq 1.5\,\mu m$.

Proximity effects. The TIM investigations of proximity effects showed a strong influence of surrounding guard-rings to the excess minority carrier concentration in substrate. In commercial I/O cells the effect of biased guard-ring constructs on the diffusion of minority carriers into neighboring regions was analyzed. The collection of electrons by biased n^+ guard-rings significantly reduced the amount of carriers spreading outside the stressed I/O cell. Regions with latch-up critical excess carrier concentration (phase shift below $-0.02\,rad$) were identified. At these areas of the chip layout any latch-up sensitive structures should be avoided. Such information allowed the optimization of floor plans and latch-up protection structures.

Case study. In the case study of the commercial power control device the latch-up triggering mechanism was analyzed by controlled transient latch-up testing. It was the first time use of the transient interferometric mapping method for transient latch-up

investigations in a real product. The injecting junction and the parasitic SCR structure were identified by TIM scans. The experiments revealed the dynamic latch-up triggering mechanism and the higher latch-up sensitivity for shorter pulses. The power control device latched during negative spikes on the supply voltage between a transistor and guard-rings. These guard-rings were normally employed to prevent latch-up. However, in this particular case they were counterproductive. Disconnecting the guard-ring by focused ion beam or – as short term solution – the use of silicon-on-insulator (SOI) substrates increased the latch-up robustness. The experimental results gave very useful hints for redesigning the chip and as consequence the design guidelines were amended to prevent similar problems in future.

Chapter 4

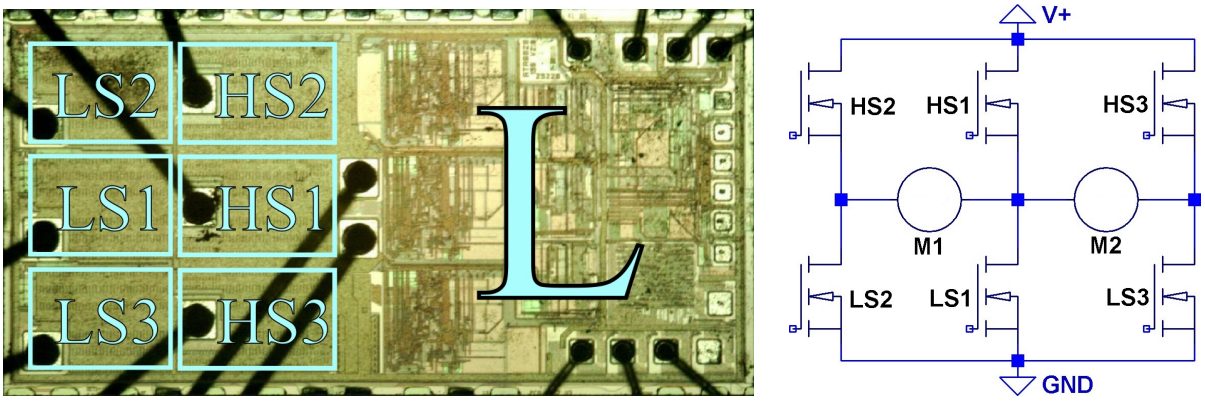
Investigation of hot spots in a full operating half bridge driver IC

Suspected hot spot problems during reliability tests of a commercial H-bridge driver IC will be investigated in-situ during full operation in an application board. In normal operation the built-in thermal shutdown circuit of the triple half-bridge driver IC is sufficiently fast to protect the chip in overload conditions, but during accelerated reliability tests some chips failed with suspicion to hot spots in the output transistors. Therefore, hot spots in the output transistors will be searched during full operation just before activation of the thermal protection circuit.

4.1 Device description

The investigated integrated circuits contain three half-bridge DMOS output drivers (LS1–HS1, LS2–HS2, LS3–HS3) with control logic ("L") and a standard serial data interface (serial peripheral interface, SPI). The top view of an opened chip is shown in Figure 4.1a [117]. The currents through the DMOS output transistors are limited by internal logic to approximately 1.4 A. A typical application would be a dual full-bridge circuit with common mid-rail. That allows control of two motors in both directions, as shown in Figure 4.1b.

The chip is designed by *Atmel* [86] in 0.8 µm SOI-BCD technology for automotive and industrial applications for supply voltages up to 40 V. The cross section of one finger of the lateral DMOS transistor is shown in Figure 1.4 [113]. The active silicon layer (∼2 µm thickness) is electrically (and thermally) isolated from the silicon handle wafer



(a) (b)

Figure 4.1: (a) Mirrored top view of triple half-bridge driver chip. Each half-bridge consists of a low-side (LS) and a high-side (HS) DMOS output driver. Total die size is $\sim 2900\,\mu m \times 1400\,\mu m$ [117]. (b) Typical application circuit for controlling two motors (M1, M2) with three half bridges.

with a silicon dioxide layer ($\sim 1\,\mu m$ thickness). Details of the DMOS transistor itself are presented in [113–116].

The hot spot investigations are focused on the high-side output driver ("HS1") in the center of the chip, because it has least lateral cooling and showed most damage during the reliability tests. The layout (90° turned H-shape) of the investigated output driver is shown in Figure 4.2. It consists of ten DMOS transistor blocks ("D") and one separate temperature control monitoring device (shutdown circuit "S", $\sim 40\,\mu m \times 60\,\mu m$) with built-in thermal shutdown circuit in its center. The temperature control disables the DMOS output transistor when the temperature at the sensor exceeds 175 °C (448 K).

4.2 Experimental details

For investigations during full operation, the chip is operated in an application board. The application board shown in Figure 4.3 includes power supply, status LEDs, load resistors and a communication port.

A special software interface *SPIgen.exe* [118], which is running at a personal computer, controls the application board with SPI commands over a link cable. Therefore, the scanning TIM setup cannot initiate – as usually – the stress pulses itself and it must be synchronized with the application board by a voltage probe at the output pin of the DMOS output driver.

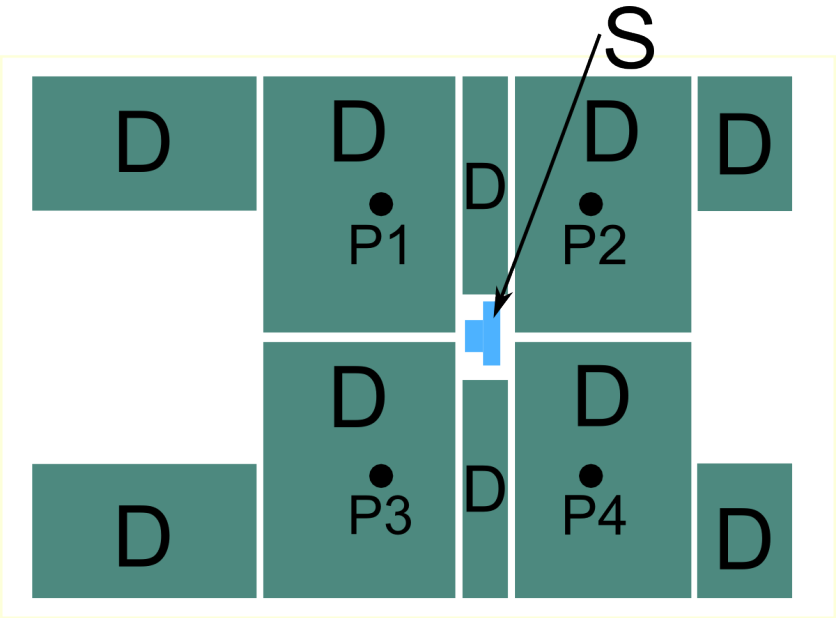


Figure 4.2: Simplified layout of HS1 output driver. The DMOS transistor blocks are marked with "D" and the thermal shutdown circuit with "S".

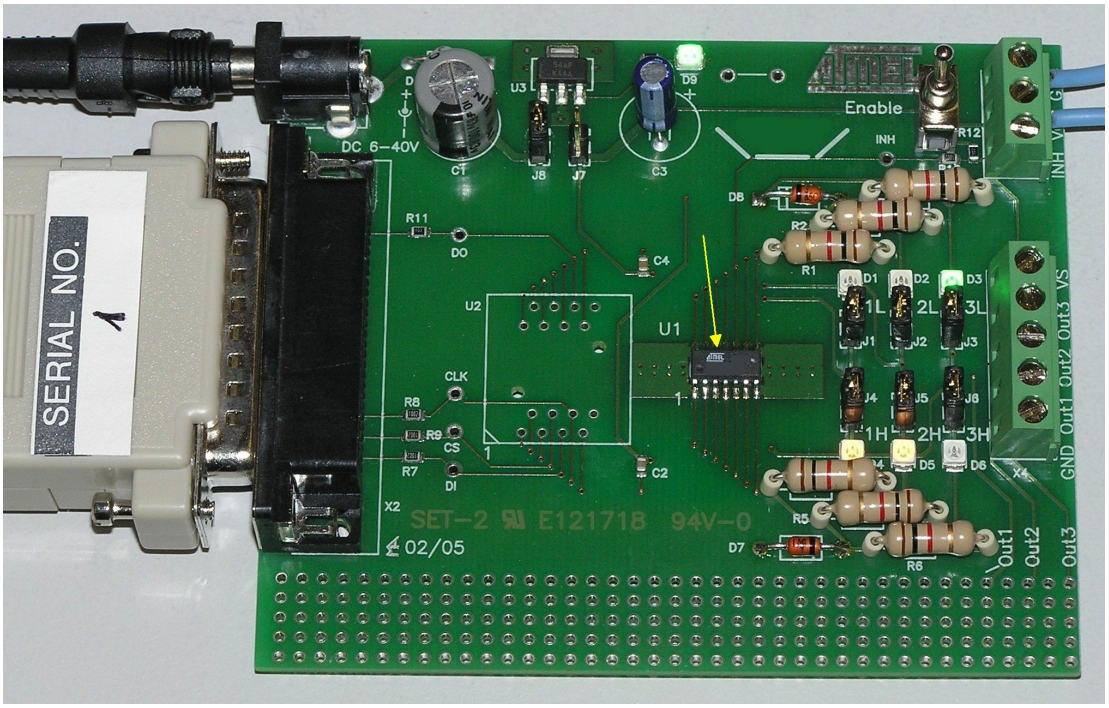
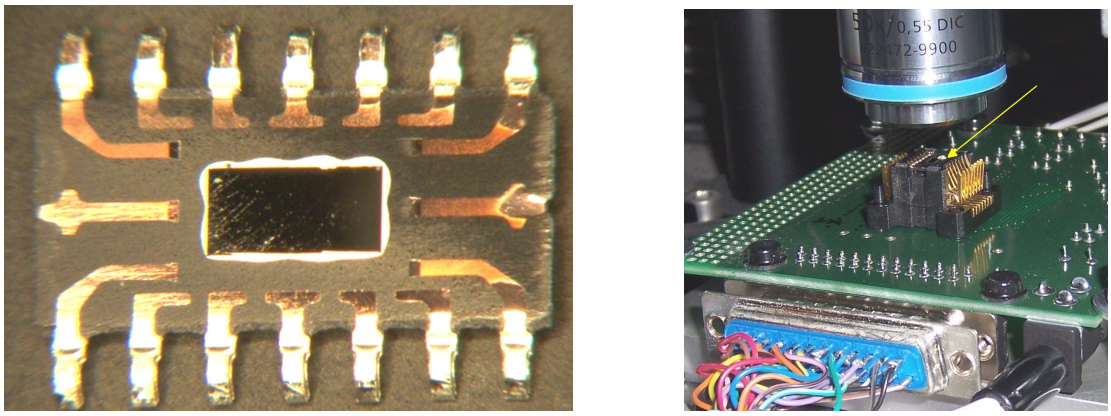


Figure 4.3: Application board (105 mm × 90 mm) for triple half-bridge driver chip with power supply, status LEDs, load resistors and a communication port.

4.2.1 Device preparation

To access the silicon backside of the investigated surface mounted device, the leads of the package are flattened. The whole package is opened from backside and the silicon substrate (with package) is grinded and polished to get a sufficiently bright infrared image from the back of the device for TIM investigations. The backside polished chip is shown in Figure 4.4a.

The opened SO14 package is mounted upside-down in an adapted socket of the application board to provide access to the back of the chip during its operation. To correct the mirrored pin assignment, the leaded socket is soldered to the application board on its opposite side (solder side). The chip backside is scanned with the laser beam by moving the whole application board with an x-y stage. The upside-down mounted application board with the chip in the socket is shown in Figure 4.4b. Due to backside polishing the ground connection to the substrate via the lead frame is removed. It is restored with conductive glue, to prevent effects of charge accumulation and breakdown voltage shifts.



(a) (b)

Figure 4.4: (a) Backside polished chip. (b) Mounted chip in an adapted socket at the application board installed in the scanning TIM setup.

4.2.2 Electrical methods

The schematic diagram of the measurement setup is shown in Figure 4.5. The application board is powered by two DC-supplies (*VBias* and *VCC*). For pulsed excitation during the TIM experiments the DMOS output transistors are turned on and off with serial commands (SPI) by a personal computer. The pulse duration is 650 µs and the repetition rate is set to 1.5 Hz to ensure cooling down of the chip after each stress pulse. The biasing

voltage *VBias* is chosen up to 50 V and a load resistance of 1 Ω is used.

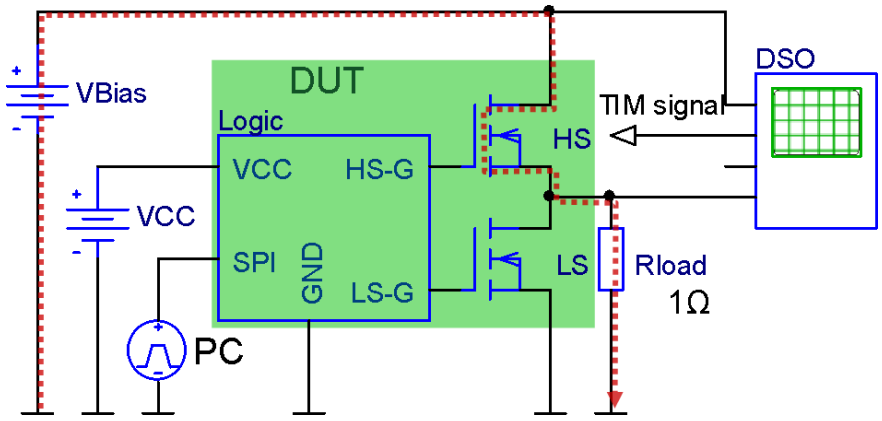


Figure 4.5: Schematic diagram of the high-side (HS) output driver test setup. The SPI commands are generated by a personal computer (PC). A digital sampling oscilloscope (DSO) is used to record current, voltage and phase shift transients. The dotted line marks the load current flow.

4.2.3 Optical methods

The scanning TIM method is adapted for investigation of internal temperature distribution of the opened half-bridge driver IC during its operation. In the present case the dominant contribution to the optical phase shift comes from heat giving positive phase shift values. In SOI the TIM signal is also nonlinearly influenced by active silicon and buried oxide layer thickness [87, 119].

4.3 Electrical characterization of thermal shutdown

To uncover any critical hot spots during the thermal shutdown process, the device is tested inside (22 V) and above its specification[1] (50 V). The measured voltage and current waveforms for 22 V and 50 V supply voltage are shown in Figures 4.6 and 4.7 [120]. As the temperature at the sensor reaches 175 °C the built-in logic circuit shuts down the hot output transistor. This occurs after 420 µs and 31 µs respectively.

The effect of supply voltage on the time to shutdown is shown in Figure 4.8. As the power increases, the time to shut down (the effective pulse duration) decreases – the critical temperature of 175 °C at the sensor is reached earlier. For 12 V biasing the temperature

[1] The chip is designed for supply voltages up to 40 V.

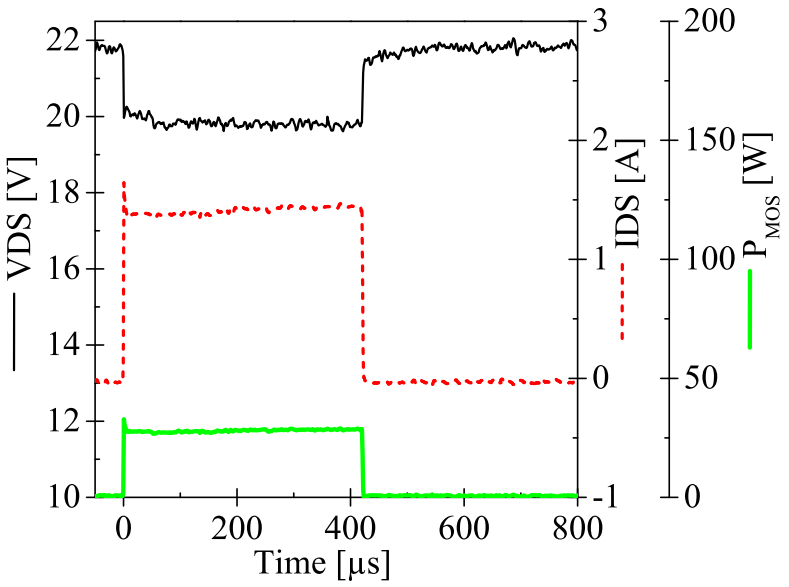


Figure 4.6: Current, voltage and power waveform during 22 V stress pulses. After 420 µs the temperature sensor reaches 175 °C and the internal logic circuit shuts down the output transistor.

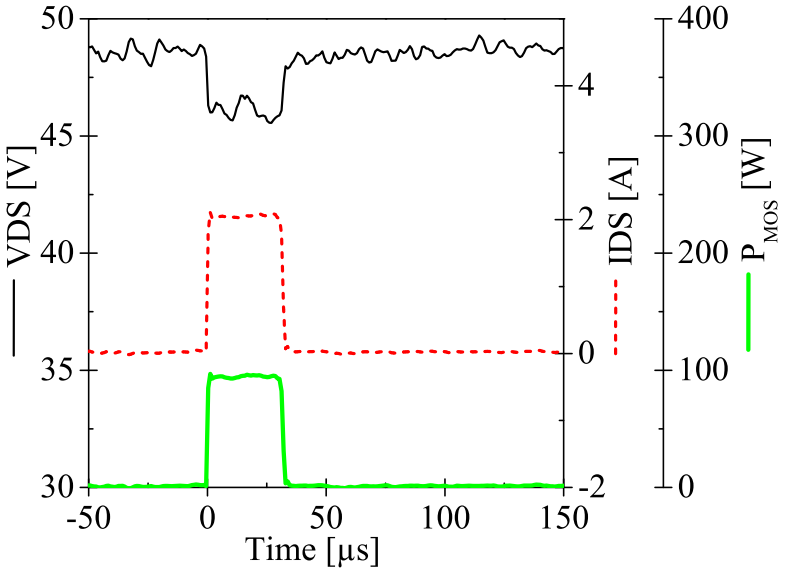


Figure 4.7: Current, voltage and power waveform during 50 V stress pulses. After 31 µs the temperature sensor reaches 175 °C and the internal logic circuit shuts down the output transistor.

stays below 175 °C and no thermal shutdown occurs. Therefore, after 650 µs the current is turned off with an SPI command from the personal computer.

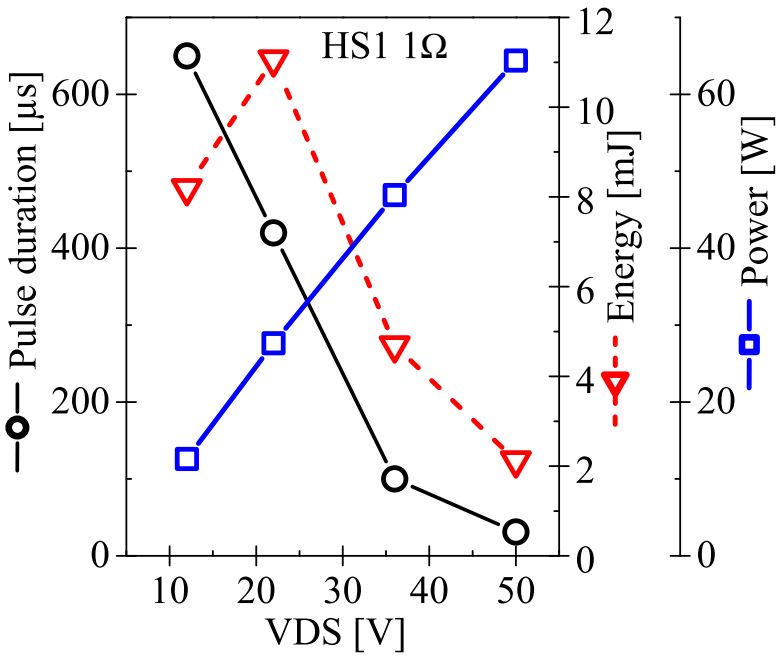


Figure 4.8: Effect of supply voltage on time to thermal shutdown (pulse duration). Shutdown occurs at a sensor temperature of 175 °C. At 12 V shutdown is initiated by SPI-software.

4.4 Internal behavior of the output transistor during thermal shutdown

The phase shift transient at the position of temperature sensor ("S") for 22 V pulses is given in Figure 4.9. Thermal shutdown occurs at 34 rad. The slight undulation in the phase is caused by the Fabry-Pérot interferences, which are typical for SOI systems [10, 62]. They were predicted in [119] for large phase shift range such as in this study, but not observed in previous investigations where phase shifts one order of magnitude lower were measured during short ESD pulses.

The phase shift transients for 50 V pulses are given in Figure 4.10. At thermal shutdown the phase shift at the temperature sensor ("S") reaches 6 rad.

To uncover local hot spots, 2D TIM scans of the whole output driver are performed. The measurement at 22 V/420 µs pulses shows the highest phase shift (heating) in the center of

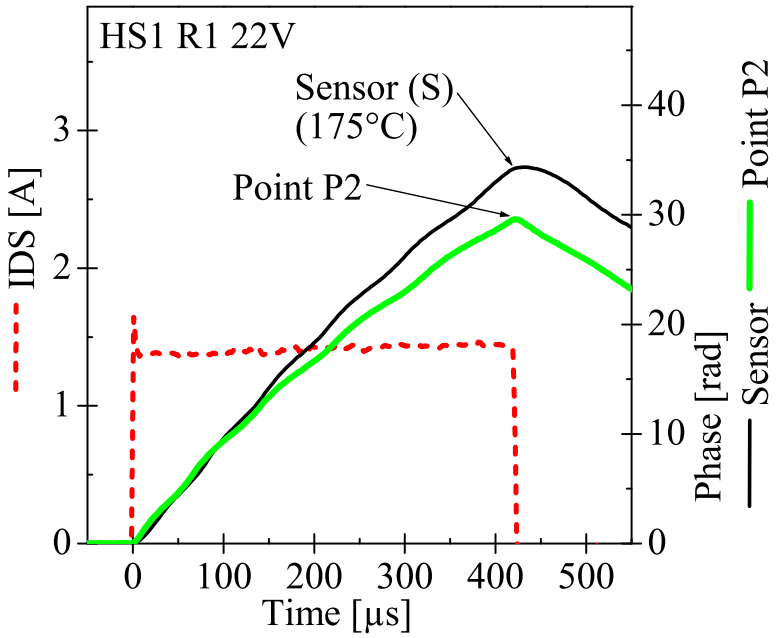


Figure 4.9: Current and phase shift waveform at temperature sensor ("S") and point P_2 for 22 V pulses. The locations are marked in Figure 4.11. After 420 µs the temperature sensor reaches 175 °C and the internal logic circuit shuts down the output transistor.

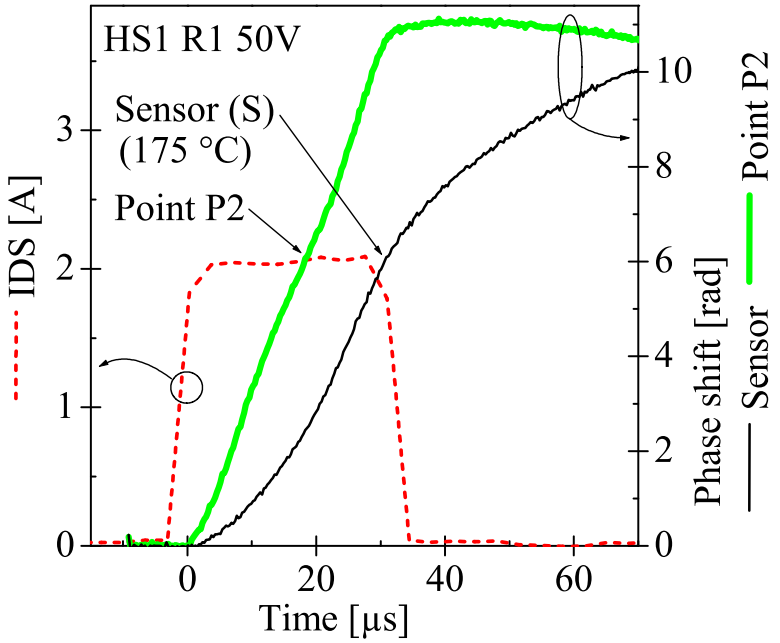


Figure 4.10: Current and phase shift waveform at temperature sensor ("S") and point P_2 for 50 V pulses. The locations are marked in Figure 4.15. After 31 µs the temperature sensor reaches 175 °C and the internal logic circuit shuts down the output transistor.

the output driver (see Figure 4.11), where the temperature sensor ("S") is located. Due to the long thermal diffusion length for long pulses (Equation (1.6) gives for 420 µs in silicon ∼194 µm and Equation (1.7) for silicon dioxide ∼16 µm) the heat distribution of the four biggest contiguous DMOS areas (the areas around P_1, P_2, P_3 and P_4) overlaps. Thus the temperature sensor in the center of the output driver does not influence significantly the heat distribution and the output driver behaves as a single big heat source.

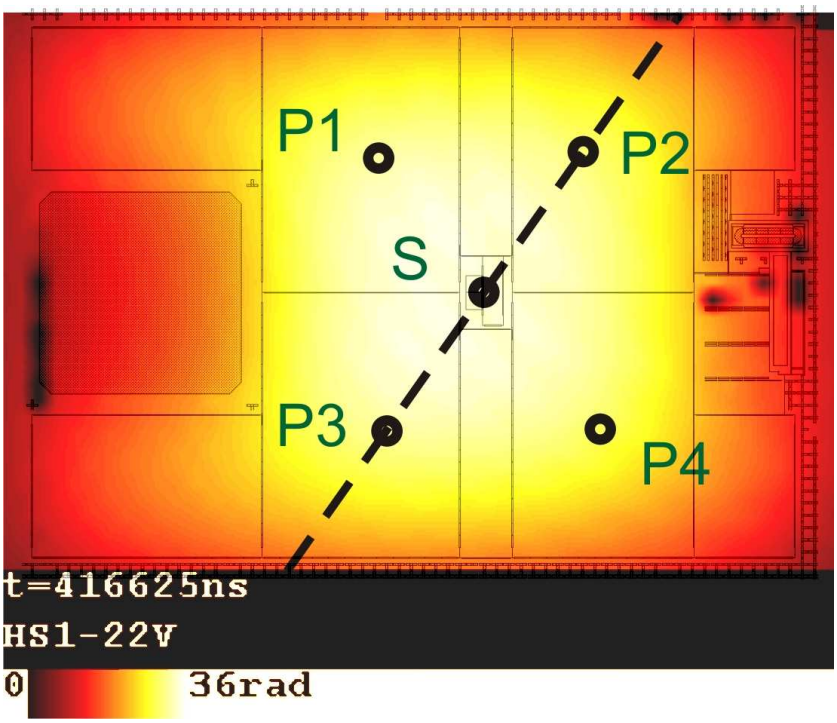


Figure 4.11: Two-dimensional TIM phase shift scan with layout overlay of HS1 output driver showing an extended hot area at the temperature sensor ("S") just before thermal shutdown of 22 V (420 µs) pulses.

The temperature distribution in the output driver is much different for 50 V/31 µs pulses. The 2D TIM scan at $t = 15$ µs (roughly in the middle of the stress pulse) shows in Figure 4.12 heating at the ten DMOS transistor blocks and just a slight overlapping heat distribution at the sensor area (see "S"). The H-shape (90° turned) of the hot DMOS transistor blocks and the colder temperature sensor in its center is clearly visible. The visible undulations in the phase shift are related to slight heating and thermal expansion of the setup and DUT during the several hours lasting TIM scan and optical artifacts due to inherent thickness variations of the SOI layer structure. Due to shorter thermal diffusion length for shorter pulses (for 15 µs the diffusion length in silicon is ∼38 µm and in silicon dioxide ∼3.1 µm) and the heat removal along the border and to the vertical sides, the heat distribution of the DMOS areas does not overlap very much.

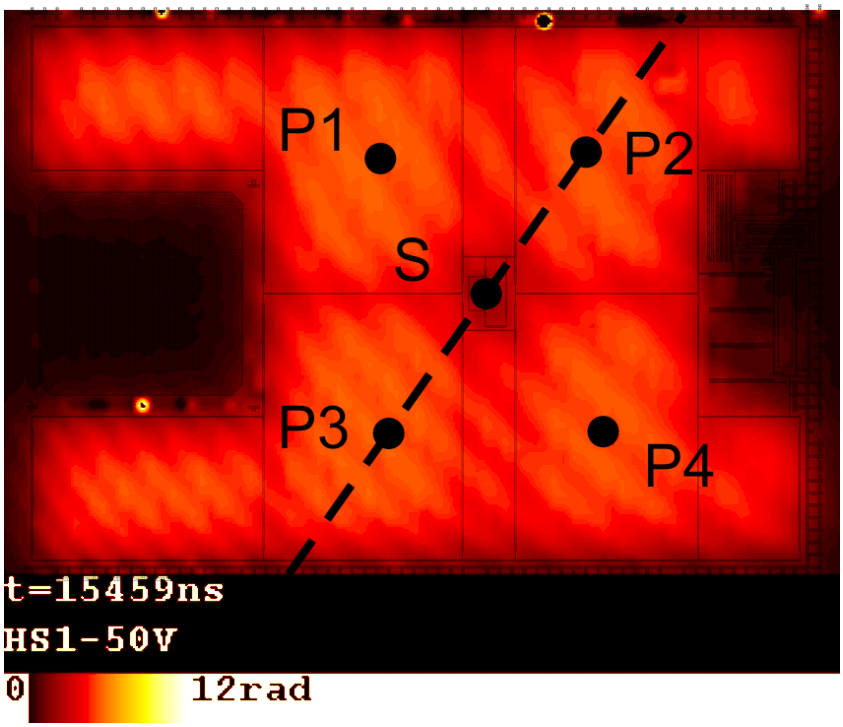


Figure 4.12: Two-dimensional TIM phase shift scan with layout overlay of HS1 output driver showing heated DMOS at $t = 15\,\mu s$ of 50 V pulses. The shape of the hot output driver and the colder temperature sensor in its center is clearly visible.

For a first simple estimation of the phase shift contributions from the active silicon layer and the handle-wafer, the heat diffusion is calculated with Equation (1.4). Figure 4.13 shows the heat diffusion at $t = 15\,\mu s$. With Equations (1.31) and (1.37) the phase shift for a temperature increase of 1 °C can be calculated. This gives for the active silicon layer a phase shift of 3.6 mrad [2] and for the handle-wafer the (dominating) phase shift of 49 mrad [3].

At the temperature sensor layout block ("S") no power DMOS transistor is located and therefore no direct heating occurs. Heating of the temperature sensor occurs only due to heat transfer from surrounding areas. Figure 4.14 illustrates the heat transfer via the metal layers of the chip, trenches and buried oxide in conjunction with the handle wafer.

At $t = 31\,\mu s$ the sensor reaches 175 °C and thermal shutdown occurs. In the corresponding 2D TIM scan in Figure 4.15 four local hot spots (P_1, P_2, P_3 and P_4) can be clearly distinguished. These hot spots are located in the four biggest contiguous DMOS areas. Due to the delayed heat transfer to the sensor area, the phase shift (and temperature) at the sensor area is much lower than at the hot spots. Consequently the temperature

[2] The contribution of the silicon dioxide layer is more than one order of magnitude lower.
[3] At $t = 1\,\mu s$ the phase contribution of the active silicon is 3.4 mrad and of the handle-wafer is 4.3 mrad.

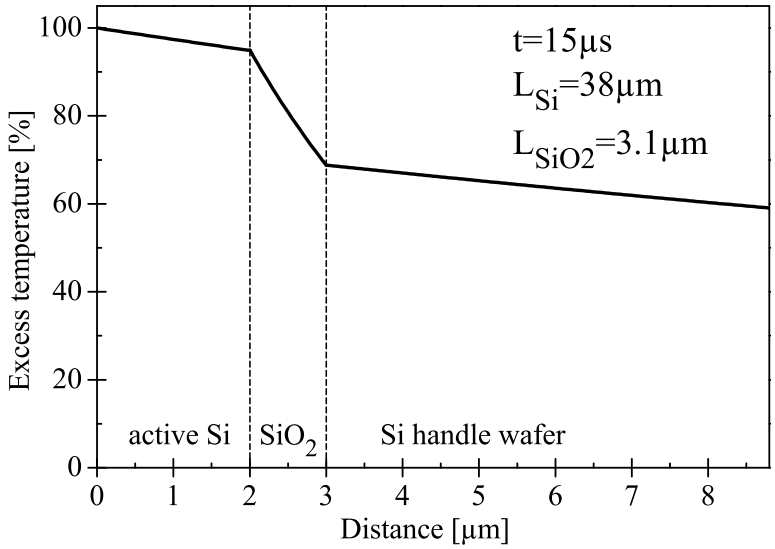


Figure 4.13: Schematic temperature profile in an SOI structure at $t = 15\,\mu s$. The temperature decays with the spatial decay constant (thermal diffusion length) L.

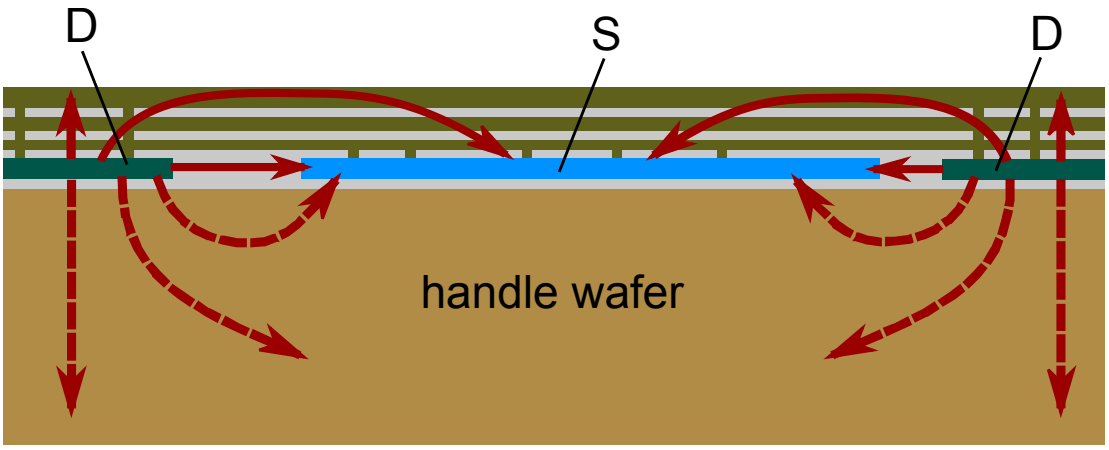


Figure 4.14: Schematic cross section with symbolic heat transfer (see arrows) from DMOS transistors blocks ("D") to sensor block ("S"). The active silicon layer is electrically and thermally isolated from the handle wafer with silicon dioxide (gray color).

sensor underestimates the real peak temperatures in the DMOS transistors at short stress pulses. Based on the phase shift data a video animation is made to monitor the heating process [120].

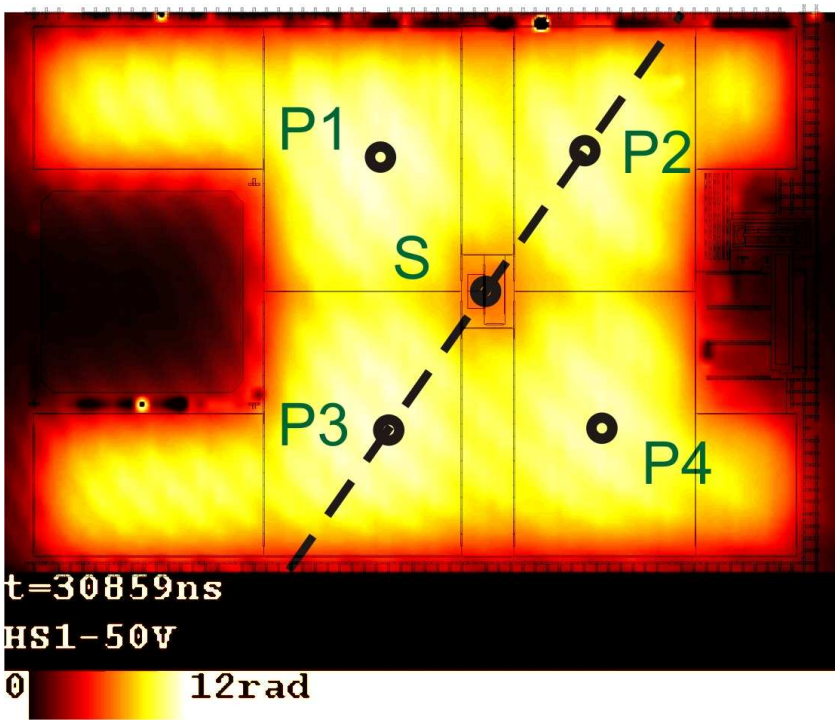


Figure 4.15: Two-dimensional TIM phase shift scan with layout overlay of HS1 output driver showing four hot areas (P_1, P_2, P_3, P_4) just before thermal shutdown of 50 V (31 µs) pulses.

The cross section along the dashed line of Figure 4.15 shows for 50 V pulses a large phase shift difference (approximately 38 %) and therefore temperature difference between the hot spots and the temperature sensor area (see Figure 4.16). The observed hot spots correlate with the failure positions obtained during reliability tests.

The comparison of the phase shift evolution at the temperature sensor area and at the hot spot for 50 V pulses shows a significantly delayed heating of the temperature sensor area (see Figure 4.10). The phase shift value for thermal shutdown (6 rad at the sensor area) is reached at point P_2 approximately 13 µs earlier. The delayed heating of the temperature sensor cause a too late shutdown of the output driver and therefore the DMOS transistor temperature exceeds the desired limit.

The phase shift increase at the sensor area after the stress pulse is related to heat transfer from surrounding hotter areas to the sensor area. Phase increase still occurs, if just the

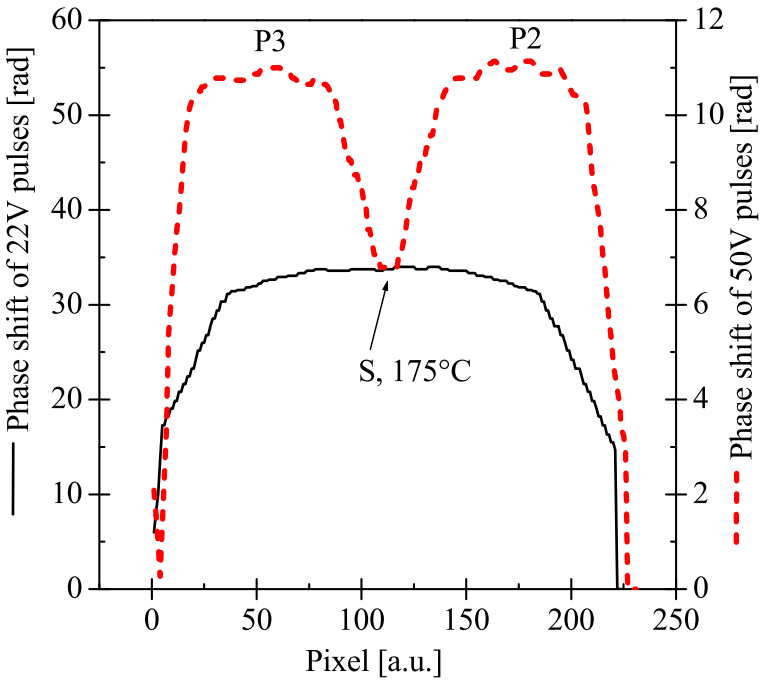


Figure 4.16: Phase shift cross section along dashed line of Figures 4.11 and 4.15 for 22 V and 50 V pulses.

handle wafer below the sensor is heated by lateral heat diffusion[4]. On the other hand for long pulses (22 V/420 µs) the temperature at the sensor is the maximum temperature in the output driver – see phase shift at sensor and point P_2 in Figure 4.9.

A rough relation of optical phase shift to temperature is shown in Figure 4.17 by correlating the phase shift at the sensor at thermal shutdown to 175 °C. It shows that the temperature sensor underestimates the average temperature of the output driver for short (31 µs) stress pulses with 50 V.

Actually the phase shift represents the integrated temperature along the depth (z) of the DUT, but nevertheless often inhomogeneities in lateral temperature distributions can be uncovered. The following dominant tolerances and nonlinearities are taken into account: (a) ±20 K of the temperature sensor itself and (b) the nonlinearity (the undulations in Figure 4.10) of the optical phase shift in SOI.

[4] Electrical measurements on other SOI structures with a diode as temperature sensor showed increasing diode temperature up to 10 µs after the termination of the stress pulse [117].

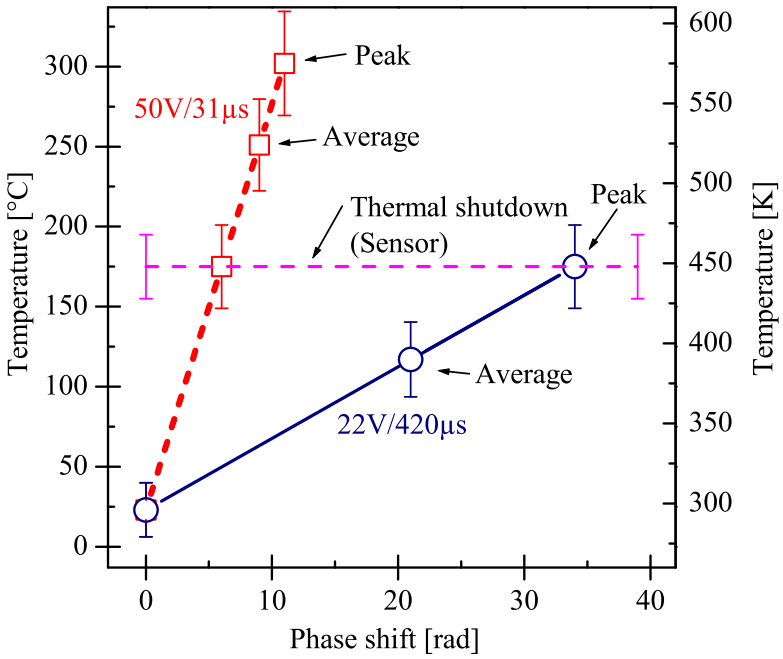


Figure 4.17: Rough temperature estimation for 50 V (31 µs) and 22 V (420 µs) pulses. The temperature sensor has a tolerance of ± 20 K.

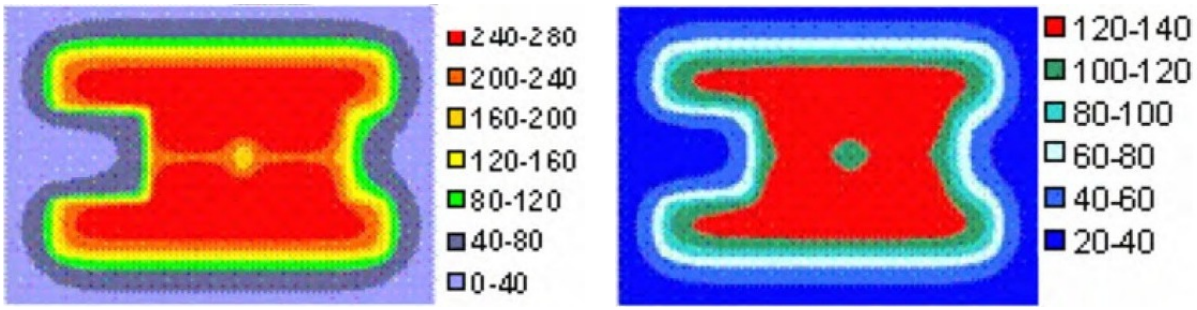
4.5 Comparison to electrothermal simulations

Based on these TIM results *J. Teichmann* performed electro-thermal simulations of the output driver structure with the temperature sensor circuit [117]. The simulations reproduce well the experimental results at 50 V and give insight to the temperature distribution in the third dimension (depth) of the SOI chip.

The simulated temperature distribution in the active silicon layer of the output driver shows a peak temperature in range of 240 °C to 280 °C, while the sensor reaches its shutdown temperature of 175 °C (see Figure 4.18a [117]). The temperature of the handle wafer just below buried oxide reaches up to ∼130 °C (see Figure 4.18b [117]). The rough approach of temperature estimation by correlating the phase shift at the sensor to its temperature in Figure 4.17 was an acceptable first assumption.

A simple calculation of the phase shift contributions in the power DMOS transistor according to Equation (1.31) gives at $t = 31\,\mu s$ for the active silicon layer with an averaged excess temperature of $\Delta\overline{T_a} = 233\,°C$ a phase shift of $\Delta\varphi \simeq 0.87\,rad$ and for the handle-wafer with Equations (1.4) and (1.37) and the boundary temperature of $\Delta T_{h0} = 103\,°C$ a phase shift of $\Delta\varphi \simeq 10.18\,rad$. The total phase shift[5] of 11.1 rad matches quite well to

[5] The phase shift in silicon dioxide is ∼0.016 rad.



(a) (b)

Figure 4.18: Simulated temperature (°C) with 12.5 µm grid at thermal shutdown of the output driver [117]. (a) At the active silicon layer. (b) Just below the buried oxide.

the TIM measurement (see line P2 in Figure 4.10).

The simulated temperature of six fingers of an SOI power DMOS transistor is shown in Figure 4.19 [117] at instants 30 ns, 1 µs and 10 µs. It shows much higher temperature at the metal layers than at the handle wafer below the buried oxide, because silicon dioxide has roughly 112 times lower thermal conductivity compared to silicon. The electro-thermal simulations depict that during short pulses the main heat flow to the temperature sensor occurs through the metal layer system of the chip.

A better thermal interaction of the temperature sensor and the output transistor is necessary. This could be done by incorporation of the temperature sensor directly (without trench) into the output transistor or layout the temperature sensor as thin stripe close to the middle of the power transistor fingers[6].

4.6 Summary of hot spot investigations

The first in-situ TIM investigation of an opened chip during full operation in an application board was performed. The origin of failure locations during accelerated reliability tests was found to be related to delayed response of the built-in thermal shutdown circuit. In the DMOS output transistors four hot spots were revealed, where the temperature exceeded the limit of the built-in temperature sensor. The hot spots correlate with the failure locations obtained during the accelerated reliability tests. In contrast to bulk silicon devices the TIM results of SOI devices showed undulations in the phase shift due to optical artifacts, but inhomogeneities were clearly identified. The built in thermal

[6] The end of the fingers is in the middle of the output driver – see horizontal gap in Figures 4.2 and 4.18a.

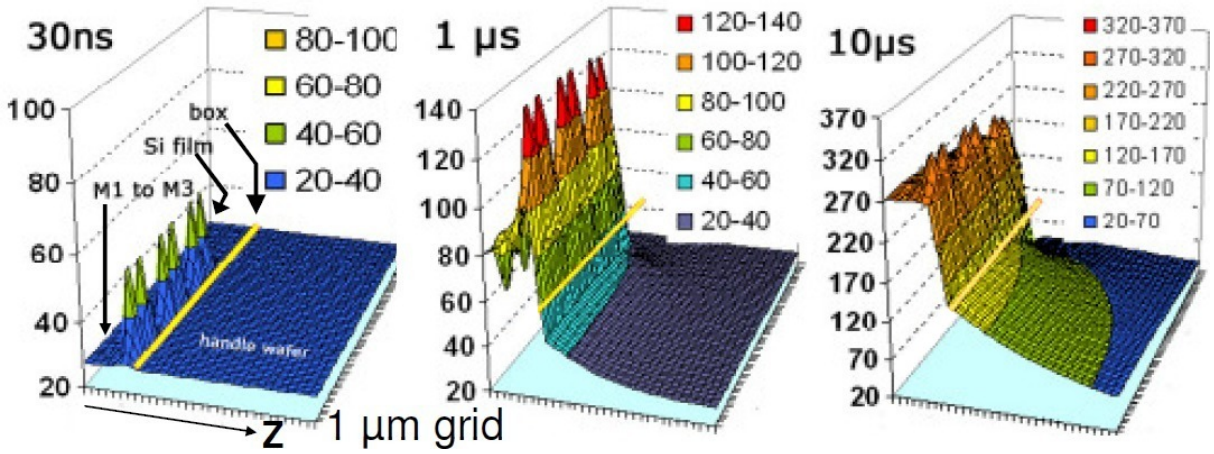


Figure 4.19: Simulated temperature (°C) with 1 µm grid of six stripes in an SOI power transistor during a 6 W/mm pulse showing much higher heating at the metal layers than at the handle wafer below the buried oxide [117]. The simulation nodes of the metal layers and their vias are from $z = 0$ to 5 ("M1 to M3"). The active silicon (drift region, "Si film") is at $z = 6$. The buried oxide ("box", yellow line) node is at $z = 7$ and followed by the nodes of the handle wafer.

shutdown circuit could not identify fast enough distant hot spots due to slow heat diffusion and consequently delayed heating of the temperature sensor.

The electrothermal simulations agreed with the TIM experiments and complemented the measurements in the depth of the chip. They revealed the main heat transfer through the metal layer system of the SOI chip during short pulses.

A better thermal interaction of the temperature sensor and the output transistor was found to be necessary. This could be done by incorporation of the temperature sensor directly (without trench) into the output transistor or layout the temperature sensor as thin stripe close to the middle of the power transistor fingers.

Chapter 5

Conclusion and prospects

Inhomogeneities in temperature and current flow (excess charge carrier) distributions were revealed by optical phase shift measurements with the non-destructive transient interferometric mapping (TIM) technique at various test structures for libraries and at two case studies of commercial integrated circuits. Especially during the case studies with their large and complex circuits TIM helped to locate problems, which were further analyzed with simulations of the involved area to provide also insight into the third dimension (depth) of the structures.

Measurement setup progress. The scanning TIM method was extended with a facility for transient latch-up testing with multiple supply domains to perform detailed analysis of the excess carrier diffusion under transient current injection in silicon devices. Further enhancements compensated for sample misalignments like torsion and inclination angles – thus the mechanical alignment of the device under test was greatly facilitated. The introduced automated laser beam refocusing system allowed the scanning of several millimeters without defocusing and enabled investigations of large circuits, such as the presented commercial case studies ($\sim$4 000 000 µm^2).

ESD protection structures. Pulse-to-pulse instabilities in the pulsed current-voltage (I-V) characteristics of gate-coupled multi-finger NMOS ESD protection structures were explained by directly observed triggering patterns using the holographic TIM method. The different voltage branches in the pulsed I-V characteristics were caused by different numbers of triggered intrinsic *npn* bipolar transistors. The measured phase shift in single- and two-finger devices was compatible with the TCAD simulations. It was found that

the central fingers of multi-finger devices were always activated, while the cathode side fingers behaved most unstably.

Latch-up investigations. Negative as well as positive substrate currents were investigated as a trigger for possible external transient latch-up at special test structures with floating detector (SCR) supply domain. Further, case studies of commercial I/O cells and a power control device were performed. The transient excess carrier concentration was studied for various layout configurations and injection carrier types and the results were complemented with device simulations. The excess carrier density at the detector structure and therefore its sensitivity to latch-up was found to strongly depend on guard-ring configurations and on the distance of the SCR structure to the injecting junction. Layout configurations with both SCR-wells facing to the injector were most sensitive due to the short distance between the injector and the *pnpn* junction. Heat spreading associated with current flow through the injector junction was identified as an additional factor, which lowers latch-up trigger currents for long injection pulses. The measured and simulated phase shifts matched well. A strong impact of the polarity of injected currents on the latch-up trigger current was proven.

Negative injection currents applied on an n well / p substrate junction caused a permanent increase of the minority carrier (electron) concentration in p substrate during the injection pulse. This led to an increasing current in the latch-up detector structure. Latch-up onset occurred usually at the terminating edge of the injection pulse, for higher injection amplitudes latch-up triggered already during the injection pulse. Biasing the guard-ring constructs substantially reduced the latch-up sensitivity of the test structures. It was found, that in this CMOS technology, a phase shift (excess carrier concentration) of $-0.02\,\mathrm{rad}$ was already critical for activation of worst-case SCR structures. The carrier diffusion process could be modeled with a short diffusion length in a layer near the surface – which was affected by guard-rings and higher doped wells – and a long diffusion length in the low doped substrate.

Positive injection currents applied on a parasitic *pnp* transistor caused an increase of the local substrate potential. Excess carriers were observed only in direct vicinity of the injector. Saturation of the injector transistor led to forward-biasing of the p substrate / detector n well junction and therefore to a *negative* contribution to the total detector current, which impeded latch-up during the injection pulse. Consequently, latch-up was observed only after the terminating edge of positive injection pulses. The latch-up onset manifested itself as an abrupt phase shift decrease (increase of carrier density) in the TIM scans. The latch-up trigger current characteristics for positive injection showed

2–3 times higher current amplitudes compared to the corresponding negative injection structure. This was related to the limited injection efficiency of the saturated positive injector structure and the short dielectric relaxation time of excess majority carriers (holes, $\tau_{\mathrm{d}} \simeq 14\,\mathrm{ps}$) and their short diffusion length (Debye length $\simeq 120\,\mathrm{nm}$) in p substrate. Therefore, in this CMOS technology positive external injection current was less critical than negative.

The TIM investigations of proximity effects showed a strong influence of surrounding guard-rings to the excess minority carrier concentration in substrate. In commercial I/O cells the effect of biased guard-ring constructs on the diffusion of minority carriers into neighboring regions was analyzed. The collection of electrons by biased n^+ guard-rings significantly reduced carriers spreading outside the stressed I/O cell. Regions with latch-up critical excess carrier concentration (phase shift below $-0.02\,\mathrm{rad}$) were identified. At these areas of the chip layout any latch-up sensitive structures should be avoided. Such information allowed the optimization of I/O cell topology and floor plans.

In the case study of the commercial power control device the latch-up triggering mechanism was analyzed by controlled transient latch-up testing. The injecting junction and the parasitic SCR structure were identified by TIM scans. The experiments revealed the dynamic latch-up triggering mechanism and the higher latch-up sensitivity for shorter pulses. The power control device latched during negative spikes on the supply voltage between a transistor and guard-rings. These guard-rings were normally employed to prevent latch-up. However, in this particular case they were counterproductive. The experimental results gave very useful hints for redesigning the chip and as consequence the design guidelines were amended to prevent similar problems in future.

Hot spot investigations. Hot spots in an opened commercial H-bridge driver IC – fabricated in silicon-on-insulator (SOI) technology – were uncovered in-situ during full operation in an application board. The origin of failure locations during accelerated reliability tests was found to be related to delayed response of the built-in thermal shutdown circuit. In the DMOS output transistors four hot spots were revealed, where the temperature exceeded the limit of the built-in temperature sensor. In contrast to bulk silicon devices the TIM results of SOI devices showed undulations in the phase shift due to optical artifacts, but inhomogeneities were clearly identified. The built in thermal shutdown circuit could not identify fast enough distant hot spots. Electrothermal simulations complemented the measurements and revealed the main heat transfer through the metal layer system of the SOI chip during short pulses. A better thermal interaction of the temperature sensor and the output transistor was found to be necessary (e.g. incorporate

the temperature sensor directly – without trench – into the output transistor or layout the temperature sensor as thin stripe).

Prospects

Smaller feature size and increasing device density in the integrated circuits lead to shorter distances between junctions and to higher power densities. This makes CMOS bulk technology more sensitive to latch-up. However, guard-ring structures reduce excess carriers in substrate, but they might also complete parasitic SCR structures – as found in the presented case studies. Therefore, an increasing number of semiconductor device manufacturers switch to the more expensive SOI technology. Power devices in SOI technology demand an improved thermal management compared to bulk silicon integrated circuits and for phase shift analysis a detailed modeling of the exact optical properties of the SOI layer structure is necessary to correct undulations in the measured phase shift data.

A feasibility study of system level ESD tests in the TIM setup with a commercial IEC ESD pulse emulator ("ESD-gun") was performed. Such combination would make in-situ TIM measurements at opened ICs in application boards possible, which would allow direct verification of current sharing between on-chip ESD protection and on-board ESD protection during system level ESD stress without the need for current probes at the pins of the ICs. This would facilitate adjustments to human metal model (HMM) networks for system level ESD tests at wafer level.

Appendix A

Transient interferometric mapping setups

A.1 Scanning transient interferometric mapping setup

The scanning transient interferometric mapping setup is based on a heterodyne interferometer. Heterodyne techniques are based on slightly shifted probe beam frequency ($f_\mathrm{p} = \frac{\omega_\mathrm{p}}{2\pi}$) and reference beam frequency ($f_\mathrm{r} = \frac{\omega_\mathrm{r}}{2\pi}$). The beams interfere and any optical phase shift of the beams changes the phase φ_b of the generated beating signal.

The electric field of the reference beam at the photodetector can be written according Equation (1.26) as

$$\underline{E}_\mathrm{r}(t) = E_\mathrm{r0}\,\mathrm{e}^{\mathrm{j}(\omega_\mathrm{r}t-\varphi_\mathrm{r})}. \tag{A.1}$$

In this setup the reference beam is reflected at a fixed mirror, thus its phase φ_r is constant. The superposition of the electric field of the probe and reference beam results in the interference beam

$$\underline{E}(t) = \underline{E}_\mathrm{p}(t) + \underline{E}_\mathrm{r}(t). \tag{A.2}$$

The intensity I of a laser beam is the time-averaged value[1] of the energy flux $\vec{S}$ [68, 72] $I = |\langle\vec{S}\rangle| = |\frac{1}{2}\vec{\underline{E}} \times \vec{\underline{H}}^*|$, where $\vec{\underline{E}}$ is the vector of the complex electric field and $\vec{\underline{H}}$ is the vector of the complex magnetic field. The characteristic impedance $Z = \sqrt{\mu/\epsilon}$ yields in

[1] Amplitude variations in the THz regime cannot be measured directly.

isotropic media with $\underline{H} = \underline{E}/Z$ to the intensity of the interference beam

$$I = \frac{\underline{E} \cdot \underline{E}^*}{2Z} \tag{A.3}$$

and with Equation (A.2) to

$$I = \frac{1}{2Z}\Big(E_{\mathrm{p0}}^2 + E_{\mathrm{r0}}^2 + E_{\mathrm{r0}}E_{\mathrm{p0}}\,\mathrm{e}^{\mathrm{j}\left(\omega_\mathrm{r}t - \varphi_\mathrm{r} - \omega_\mathrm{p}t + \varphi_\mathrm{p}(t)\right)} + E_{\mathrm{p0}}E_{\mathrm{r0}}\,\mathrm{e}^{\mathrm{j}\left(\omega_\mathrm{p}t - \varphi_\mathrm{p}(t) - \omega_\mathrm{r}t + \varphi_\mathrm{r}\right)}\Big). \tag{A.4}$$

For simplicity some literatures omit $1/(2Z)$ and denote just EE^* [121]. The signal in Equation (A.4) can be written in the form[2]

$$I = \frac{1}{2Z}\Big(E_{\mathrm{p0}}^2 + E_{\mathrm{r0}}^2 + 2E_{\mathrm{p0}}E_{\mathrm{r0}}\cos\left(\omega_\mathrm{r}t - \varphi_\mathrm{r} - \omega_\mathrm{p}t + \varphi_\mathrm{p}(t)\right)\Big). \tag{A.5}$$

The first and second terms in Equation (A.5) are unmodulated intensities and result in a DC offset at the photodetector. The third term is the modulated intensity – the wanted interference pattern. The maximum interference modulation occurs, if both beams have same amplitude at the photodetector ($E_{\mathrm{p0}} = E_{\mathrm{r0}}$). Usually the intensity of the reflected reference beam is much higher than the intensity of the reflected probe beam, because the reference beam is reflected at a well reflecting mirror. In this setup the intensities can be adjusted by slight rotation of the acousto-optic modulator, which is used to generate the probe and reference beams from an incident beam.

The use of the AC-output of the photodetector eliminates the offset of the intensity. The typical voltage of the interference signal at the AC-output of the photodetector is in the form

$$V_{\mathrm{det}}(t) = V_{\mathrm{b0}}\cos\left(\omega_\mathrm{b}t + \varphi_\mathrm{b}(t)\right). \tag{A.6}$$

V_{b0} is the amplitude of the beating signal – in some particular cases it is modulated by stress-related intensity changes[3]. Noise and distortions are filtered in postprocessing.

Comparing the instantaneous phase of the optical intensity in Equation (A.5) and the electrical photodetector voltage in Equation (A.6) gives for the beating frequency

$$\omega_\mathrm{b} = \omega_\mathrm{r} - \omega_\mathrm{p} \tag{A.7}$$

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[2] Using $\frac{\mathrm{e}^{\mathrm{j}a} + \mathrm{e}^{-\mathrm{j}a}}{2} = \cos a$

[3] IR absorption or multiple interference in conjunction with layer thickness variations.

and for the phase of the beating signal

$$\varphi_{\mathrm{b}}(t) = \varphi_{\mathrm{p}}(t) - \varphi_{\mathrm{r}}. \tag{A.8}$$

According to Equation (A.8) the *optical* phase of the probe beam (φ_{p}) appears positive at the *electrical* photodetector signal[4].

If the frequency of the reference beam is smaller than the frequency of the probe beam ($\omega_{\mathrm{r}} < \omega_{\mathrm{p}}$), the instantaneous phase ($\Phi = \omega_{\mathrm{b}} t + \varphi_{\mathrm{b}}$) in Equation (A.6) can be inverted[5]. This results then in the (positive) beating frequency

$$\omega'_{\mathrm{b}} = \omega_{\mathrm{p}} - \omega_{\mathrm{r}}. \tag{A.9}$$

In this case, the *optical* phase of the probe beam $\varphi_{\mathrm{p}}(t)$ appears negative (inverted) at the *electrical* beating signal and the final phase shift needs to be inverted in postprocessing[6]

$$\varphi'_{\mathrm{b}}(t) = \varphi_{\mathrm{r}} - \varphi_{\mathrm{p}}(t). \tag{A.10}$$

A.1.1 Setup description

The scanning TIM setup is based on a heterodyne interferometer, where the device under test is scanned with a probing laser beam. Therefore, at every scanned point a stimulus is needed. The basic function of the scanning TIM setup with most important mirrors[7] is shown in the schematic diagram in Figure A.1. A continuous wave laser diode (cw laser) allows recording of time resolved phase shift transients. The device under test is laterally moved by an automated xy-stage and phase shift transients are evaluated at dedicated positions [60].

The beam of the laser diode with a wavelength of $\lambda_0 = 1.31\,\mu\mathrm{m}$ ($f_0 \simeq 229\,\mathrm{THz}$) is guided to an acousto-optic modulator (AOM), which generates from the incident beam the probe (B_1) and reference beam (B_2). The photodetectors are denoted with DET_1 and DET_2 and the beam splitters with BS (polarized beam splitters with PBS). M_1 is the mirror for the reference beam; MO is the microscope objective and DUT is the device under test.

The sample is aligned with the help of an infrared illumination (IR lamp) and an infrared

[4] This case occurs in the later shown "*slow*" heterodyne measurement mode, where the probe beam modulation frequency (68.5 MHz) is smaller than the reference beam modulation frequency (71.5 MHz).

[5] Cosine is an even function: $\cos(-a) = \cos(a)$.

[6] This case occurs in the later shown "*fast*" heterodyne measurement mode, where the probe beam modulation frequency (68.5 MHz) is higher than the reference beam modulation frequency (0 Hz).

[7] For simplification the lenses are omitted.

camera. During phase shift scans with high intensity of the laser beam, the camera is closed with beam blocker BB_2.

The cosine output of one signal generator ($f_{gp} = 68.5\,\text{MHz}$) [8] is used for the modulation of the probe beam (B_1) and a second signal generator ($f_{gr} = 71.5\,\text{MHz}$) is used for the modulation of the reference beam (B_2). The power amplifier (PA) drives the acousto-optic modulator with the two frequencies.

The unmodulated zero order beam (B_0) of the acousto-optic modulator is blocked with beam blocker BB_1. The two generated first order beams are used as probe beam B_1 and reference beam B_2. They are very little shifted in their frequencies ($f'_p = f_0 + f_{gp}$, $f'_r = f_0 + f_{gr}$) and wavelength ($\lambda'_1 = c/(f_0 + f_{gp}) \simeq 1309.99961\,\text{nm}$, $\lambda'_2 = c/(f_0 + f_{gr}) \simeq 1309.99959\,\text{nm}$).

The reflected beams pass a second time the acousto-optic modulator, which increases again their frequencies

$$f_p = f_0 + 2f_{gp},\ f_r = f_0 + 2f_{gr}. \tag{A.11}$$

The reflected beams interfere and the beating frequency f_b of the interference beam B_I can be calculated with Equations (A.7) and (A.11). It is twice the frequency difference of the two signal generators $f_b = f_r - f_p = 2f_{gr} - 2f_{gp} = 6\,\text{MHz}$. This measurement mode is called "*slow*" heterodyne mode.

Introducing temporal heating of the DUT acts like a change of the optical path. For materials with positive temperature dependence of refractive index (such as silicon) heating results according to Equation (1.28) in a positive *optical* phase shift of the probe beam $\Delta\varphi_p(t)$ and according to Equation (A.8) in a positive[9] *electrical* phase shift of the beating signal $\varphi_b(t)$.

For measuring very fast temperature changes (e.g. in the ESD regime, where pulses around 100 ns are used) the setup can be configured in a "*fast*" heterodyne mode with a higher beating frequency and the faster photodetector DET_2. Mirror M_5 is inserted to guide the interference beam to the second photodetector. Beam B_0 (beam frequency f_0) is used as reference beam. The beam blocker BB_1 is shifted from reference beam B_0 to reference beam B_2. The second signal generator f_{gr} is turned off. Now, the frequency of the probe beam is higher than the reference beam and the beating frequency is calculated with Equation (A.9). This results in a beating frequency of $f_b = f_0 + 2f_{gp} - f_0 = 2f_{gp} =$

[8] The generator frequencies are chosen for optimal performance of the optical setup.

[9] In electrical engineering a delayed signal is usually denoted with a negative *electrical* phase shift – but due to the used interferometric setup the phase of the delayed probe beam appears positive at the output signal of the photodetector.

137 MHz. According to Equation (A.10) the *optical* phase shift of the probe beam in the fast heterodyne mode appears negative (inverted) at the *electrical* beating signal of the photodetector. Consequently, the phase shift needs to be inverted in postprocessing.

A.1.2 Phase shift extraction

The recorded intensity signals from the photodetector are processed with the *Matlab* evaluation software *phaswin.m* [122]. The deviation of the instantaneous phase from an ideal cosine with frequency f_b is calculated as described by *T. Kreis* [123]. This method is widely insensitive to amplitude variations. The photodetector voltage transients in Equation (A.6) can be written in complex form as

$$\underline{V}_\mathrm{det}(t) = \underline{C}(t) + \underline{C}^*(t) \tag{A.12}$$

with

$$\underline{C}(t) = B(t)\mathrm{e}^{\mathrm{j}\Phi}. \tag{A.13}$$

where B represents the half amplitude of the beating voltage and Φ the instantaneous phase. The photodetector voltage transients are Fourier transformed

$$\underline{v}_\mathrm{det}(f) = \underline{c}(f) + \underline{c}^*(f) \tag{A.14}$$

and band-pass filtered. Filtering the negative frequencies of the spectrum and inverse Fourier transformation yields to the complex signal $\underline{C}'(t)$ in time domain. From the complex values $\underline{C}'(t)$ the instantaneous phase is calculated at each instant of the recorded transient [60]. The arguments are between $-\pi$ and $+\pi$, thus they are corrected (unwrapped) by adding multiples (m) of 2π. From the unwrapped result the argument of the used beating frequency and an arbitrary offset are subtracted

$$\Delta\varphi(t) = \arctan\left(\frac{\Im\big(\underline{C}'(t)\big)}{\Re\big(\underline{C}'(t)\big)}\right) + m2\pi - 2\pi f_\mathrm{b} t - \varphi_0. \tag{A.15}$$

The phase shift just before the stress pulse is usually used as offset φ_0. This leads to zero phase shift at the beginning of the stress pulse. Depending on the used frequencies of the signal generators, the final phase shift needs to be inverted (see Equation (A.8) and (A.10)). An example of a fast heterodyne measurement is shown in Figure A.2. If the DUT shows no pulse-to-pulse instabilities several (a) phase shift transients might be

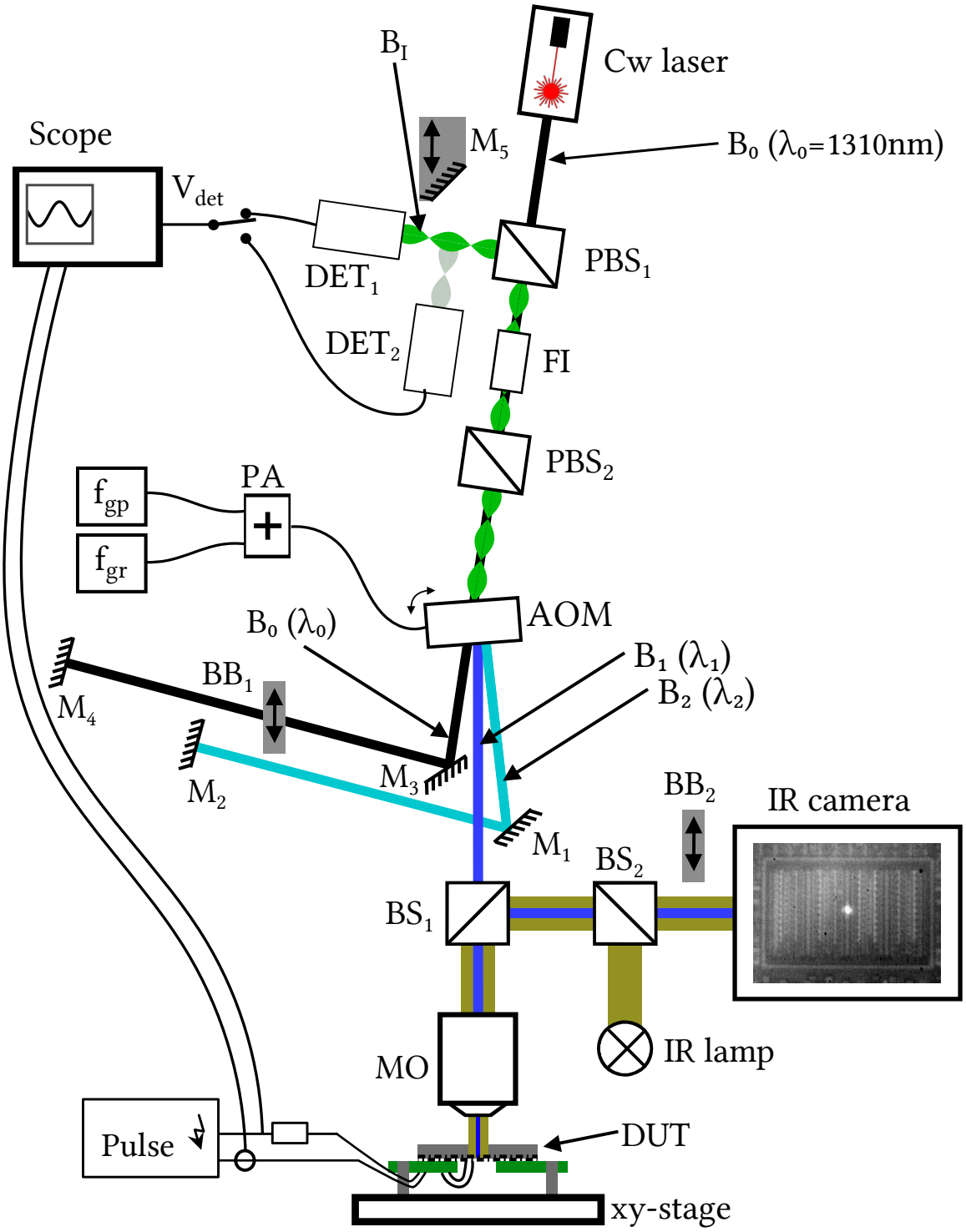


Figure A.1: Scanning heterodyne interferometer. The active area of the device under test (DUT) is scanned through the silicon substrate (backside) with a probing infrared laser beam for mapping the excess carrier and temperature distribution.

averaged to improve signal to noise ratio by $\frac{a}{\sqrt{a}}$. Averaging up to 30 measurements results in a phase resolution better than 5 mrad. The effect of excess carrier density, thickness and heat diffusion on phase shift are shown in Figures 1.22 and 1.23.

Linear or two-dimensional phase maps of the scanned area can be constructed at particular instants with the *Matlab* evaluation software *phaswin.m* [122].

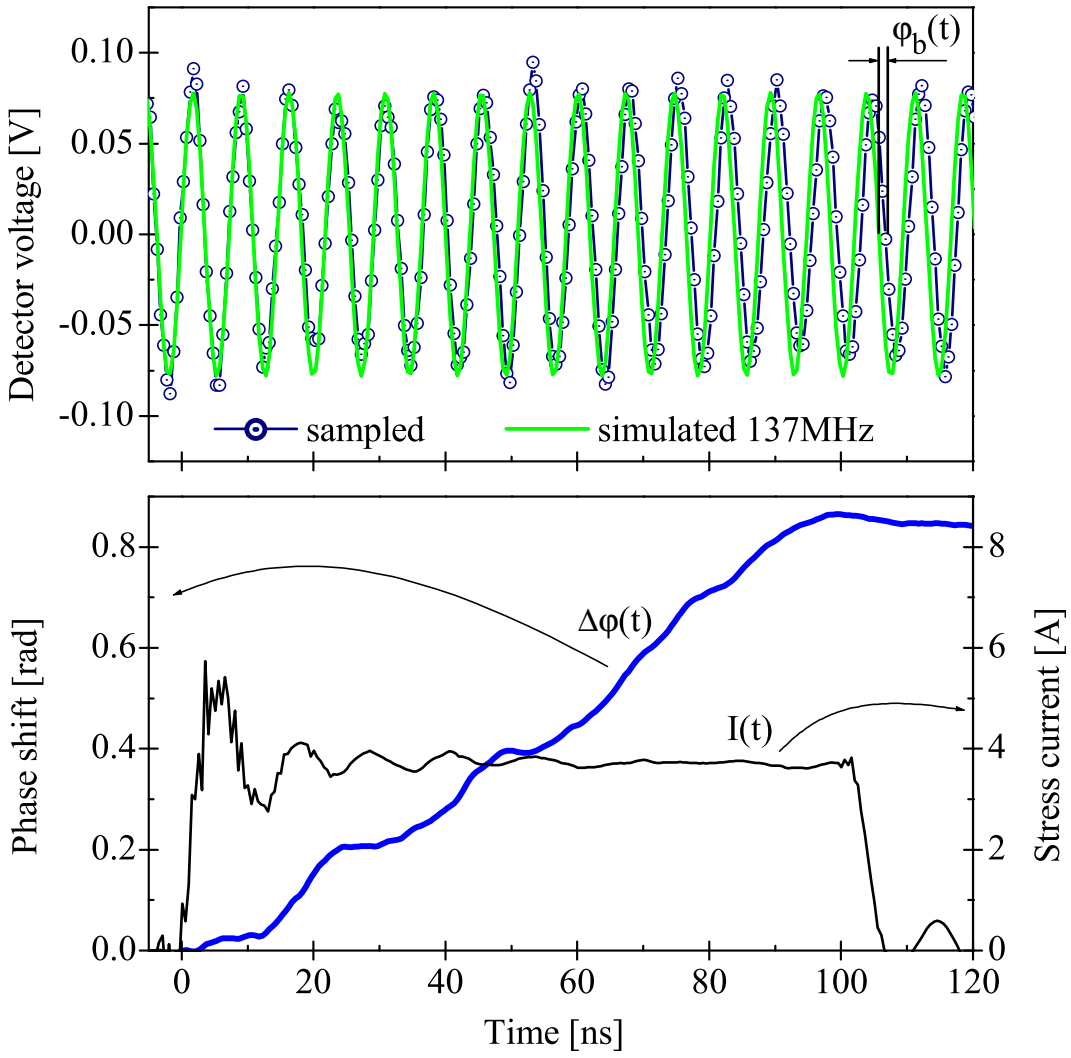


Figure A.2: Sampled photodetector voltage of a fast heterodyne measurement and simulated 137 MHz signal showing phase shift $\varphi_\mathrm{b}(t)$ during a 100 ns stress pulse. The extracted phase shift $\Delta\varphi(t)$ is inverted in postprocessing.

A.2 Holographic transient interferometric mapping setup

The holographic transient interferometric mapping setup (2D TIM setup) uses two orthogonal polarized laser pulses to exposure the whole device under test at two instants during a single stress pulse. The two interferogram images of the Michelson interferometer are recorded with two infrared cameras. Afterwards the phase shift $\Delta\Phi(x, y)$ is extracted from the *unstressed* and the *stressed* interferogram images in postprocessing with the *Matlab* program *profi.m* [124].

The basic function of the dual-beam holographic TIM setup with most important mirrors[10] is shown in the schematic diagram in Figure A.3 [69]. This setup measures the phase shift of the whole device under test with a pulsed laser exposure of the DUT. It records two snapshots of the interferogram pattern. Thus, unrepeatable behavior can be investigated with this holographic method. That speeds up experiments one order of magnitude compared to a scanning setup, which needs to repeat the stress pulse and acquisition for every scanned point.

The beam splitter BS_1 separates a part of the broad laser beams of the two high-energy pulsed laser sources to the photodetector (DET), which indicates the laser pulse on the oscilloscope ("scope"). The main beam is split up using the next beam splitter BS_2 into a reference branch B_r and a probe branch B_p. The reference branch is reflected at the slightly inclined mirror M_1. The inclination of the mirror causes parallel fringes in the interferogram image – this method is called spatial heterodyning [69]. The width and the direction of the interference fringes are set with adjusting screws at the mirror.

The probe beam is focused with a microscope objective (MO) through the silicon substrate at the active area of the DUT. The reflected beam from the metalization of the DUT interferes with the reference beam. The interference beam B_i is split using the polarized beam splitter PBS_2 for the two infrared cameras. The recorded holographic interferogram images contain in their fringes information of the device topology as well as the thermal and the excess carrier distributions. The topology information can be removed by subtraction of the phase distribution (phase map) of an unstressed situation.

A laser pulse usually overexposes the first frame of the infrared cameras. The memory effect of the cameras results in up to five subsequent dimmed frames. Mostly one of them is well exposed.

[10] For simplification the lenses are omitted.

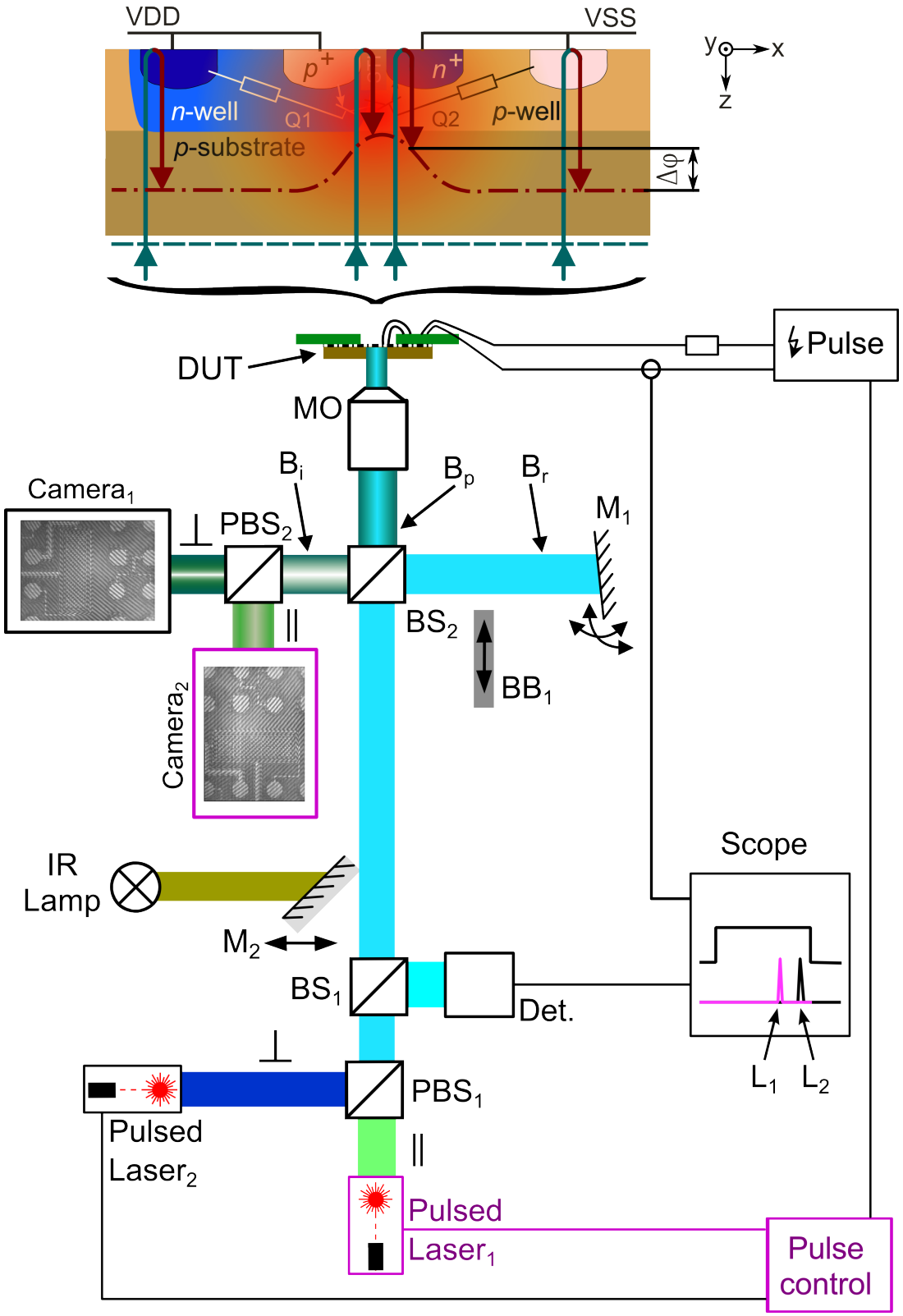


Figure A.3: Setup for holographic TIM experiments with two laser beams. The dashed line in the device cross section sketches the wave front of an incident laser pulse and the dash-dot line the reflected wave front, which is delayed by heated silicon (red shaded).

The time resolution of the phase shift measurements is determined by the laser pulse (∼5 ns). The space resolution of ∼3 µm is limited by the wavelength of the laser and the optics. The phase resolution is approximately 0.5 rad due to undulation and noise. Distortions in the interference images may cause artifacts in the phase maps [96].

A.2.1 Two-dimensional interferometry

The electric field of the reflected probe beam $\underline{\vec{E}}_\mathrm{p}$ can be described as two-dimensional transversal planar wave spreading in z direction [68, 69]

$$\underline{\vec{E}}_\mathrm{p}(\vec{r},t) = E_\mathrm{p0}(\vec{r})\,\mathrm{e}^{-\mathrm{j}\left(\vec{k}_\mathrm{p}\cdot\vec{r}+\varphi_\mathrm{p}(\vec{r},t)-\omega t\right)}\vec{e_\mathrm{p}}. \tag{A.16}$$

$\vec{e_\mathrm{p}}$ is the polarization direction and $E_\mathrm{p0}(\vec{r})$ is the amplitude of the reflected probe beam, which might be modulated due to temporal change of light absorption.

The reflected reference beam is

$$\underline{\vec{E}}_\mathrm{r}(\vec{r},t) = E_\mathrm{r0}(\vec{r})\,\mathrm{e}^{-\mathrm{j}\left(\vec{k}_\mathrm{r}\cdot\vec{r}+\varphi_\mathrm{r}(\vec{r})-\omega t\right)}\vec{e_\mathrm{p}}. \tag{A.17}$$

The phase of the reflected probe beam φ_p contains the vertical topology information of the DUT $\varphi_\mathrm{tp}(\vec{r},t_0)$, the initial phase $\varphi_\mathrm{p0}(\vec{r},t_0)$ and according to Equation (1.28) the phase shift due to refractive index changes $\Delta\varphi_\mathrm{p}(\vec{r},t)$

$$\varphi_\mathrm{p}(\vec{r},t) = \varphi_\mathrm{tp}(\vec{r},t_0) + \varphi_\mathrm{p0}(\vec{r},t_0) + \Delta\varphi_\mathrm{p}(\vec{r},t). \tag{A.18}$$

The phase of the reference beam $\varphi_\mathrm{r}(\vec{r})$ contains only[11] the initial phase of reference branch – e.g. the inclination of the mirror for spatial heterodyning [69]

$$\varphi_\mathrm{r}(\vec{r}) = \varphi_\mathrm{r0}(\vec{r},t_0). \tag{A.19}$$

The intensity of the interference pattern is calculated using Equation (A.2) and (A.3)

$$I(\vec{r},t) = \frac{1}{2Z}\Big(E_\mathrm{p0}^2(\vec{r}) + E_\mathrm{r0}^2(\vec{r}) + E_\mathrm{r0}(\vec{r})E_\mathrm{p0}(\vec{r})\,\mathrm{e}^{\mathrm{j}\left((\vec{k}_\mathrm{p}-\vec{k}_\mathrm{r})\cdot\vec{r}-\varphi_\mathrm{r}(\vec{r})+\varphi_\mathrm{p}(\vec{r},t)\right)} + E_\mathrm{p0}(\vec{r})E_\mathrm{r0}(\vec{r})\,\mathrm{e}^{-\mathrm{j}\left((\vec{k}_\mathrm{p}-\vec{k}_\mathrm{r})\cdot\vec{r}+\varphi_\mathrm{p}(\vec{r},t)-\varphi_\mathrm{r}(\vec{r})\right)}\Big). \tag{A.20}$$

The two-dimensional intensity pattern from the infrared camera can be written in the

[11] The topology information of reference mirror is usually zero.

form

$$I(x,y) = A(x,y) + \underline{C}(x,y) + \underline{C}^*(x,y) \tag{A.21}$$

with

$$\underline{C}(x,y) = B(x,y)\mathrm{e}^{\mathrm{j}\Phi} \tag{A.22}$$

and the instantaneous phase

$$\Phi = (\vec{k}_\mathrm{p} - \vec{k}_\mathrm{r}) \cdot \vec{r} - \varphi_\mathrm{r}(\vec{r}) + \varphi_\mathrm{p}(\vec{r},t). \tag{A.23}$$

$A(x,y)$ represents the background intensity and $B(x,y)$ the half amplitude of the interference fringes. Equation (A.20) represents a real signal, which can be written in the form[12]

$$I(\vec{r}) = \frac{1}{2Z}\Big(E_{\mathrm{p}0}^2(\vec{r}) + E_{\mathrm{r}0}^2(\vec{r}) + 2E_{\mathrm{p}0}(\vec{r})E_{\mathrm{r}0}(\vec{r})\cos\Phi\Big). \tag{A.24}$$

The first and second terms in Equation (A.24) are unmodulated intensities and result in a background intensity at the camera. The third term is the modulated intensity – the wanted interference pattern. The maximum interference modulation occurs, if both beams have same amplitude at the camera ($E_{\mathrm{p}0}(\vec{r}) = E_{\mathrm{r}0}(\vec{r})$). Usually the intensity of the reflected reference beam is much higher than the intensity of the reflected probe beam[13]. For this reason, the intensity of the reference beam needs to be adjusted with optical filters to get the best contrast in the interference pattern. The phase shift of the probe beam $\varphi_\mathrm{p}(\vec{r},t)$ appears positive in the instantaneous phase Φ in Equation (A.23).

For opposite inclination of the reference mirror the instantaneous phase Φ in Equation (A.23) can be inverted[14] and the phase shift of the probe beam $\varphi_\mathrm{p}(\vec{r},t)$ appears negative in the measurements

$$\Phi^\neg = (\vec{k}_\mathrm{r} - \vec{k}_\mathrm{p}) \cdot \vec{r} + \varphi_\mathrm{r}(\vec{r}) - \varphi_\mathrm{p}(\vec{r},t). \tag{A.25}$$

In this case, the final phase shift needs to be inverted in postprocessing.

A.2.2 Phase shift extraction

The phase shift extraction [125] is explained for one laser and one camera with a vertical MOS transistor, which infrared image from the back of the device is shown in Figure A.4a. The images from the delayed triggered second laser at the second camera are processed in the same way and then aligned with the *Matlab* program *imtransf.m* [126]. First, the

[12] Using $\frac{\mathrm{e}^{\mathrm{j}a}+\mathrm{e}^{-\mathrm{j}a}}{2} = \cos a$.
[13] The reference beam is reflected at a well reflecting mirror.
[14] Cosine is an even function: $\cos(-a) = \cos(a)$.

unstressed holographic interferogram image $I_{\mathrm{u}}(x,y)$ of the unstressed device[15] is acquired using the *Labview* [107] control software *auto_measurements.vi* [127–129] (Figure A.4b). At a certain instant during the electrical stress pulse the laser system is triggered and the *stressed* holographic interferogram image $I_{\mathrm{s}}(x,y)$ is acquired (Figure A.4c). The interferogram images are Fourier transformed (fast Fourier transform, FFT) to get the two-dimensional spectrum $\underline{i}$ of the intensity (Figure A.4d and e)

$$\underline{i}(u,v) = \underline{a}(u,v) + \underline{c}(u,v) + \underline{c}^*(u,v). \tag{A.26}$$

The center cross in the spectrum represents the edges of the interferogram image and the antisymmetric double cross represents the complex values $\underline{c}$ and $\underline{c}^*$. From these complex values only one part ($\underline{c}$) is used for the phase extraction. The unwanted parts and noise [96] are masked (Figures A.4f and g). The inverse Fourier transformation (inverse fast Fourier transform, IFFT) back to space region $\underline{C}'(x,y)$ results in the amplitude distributions (Figures A.5a and b) and the phase distributions of the unstressed DUT Φ'_{u} (Figure A.5c) and stressed DUT Φ'_{s} (Figure A.5d)

$$\Phi'(x,y) = \arctan\left(\frac{\Im\big(\underline{C}'(x,y)\big)}{\Re\big(\underline{C}'(x,y)\big)}\right). \tag{A.27}$$

In order to eliminate the device topology and inclination information, the unstressed phase map (Φ'_{u}) is subtracted from the stressed phase map (Φ'_{s}). Using the instantaneous phase in Equation (A.25), Equation (A.18) and (A.19) yields to the phase difference (Figure A.5e)

$$\Delta\Phi'(x,y) = \Phi'_{\mathrm{s}}(x,y) - \Phi'_{\mathrm{u}}(x,y) = -\varphi_{\mathrm{ps}}(\vec{r}) + \varphi_{\mathrm{pu}}(\vec{r}) = -\Delta\varphi_{\mathrm{ps}}(\vec{r}) + \Delta\varphi_{\mathrm{pu}}(\vec{r}). \tag{A.28}$$

The sign of the phase shift of the stressed probe beam $\Delta\varphi_{\mathrm{ps}}$ in Equation (A.28) is negative[16]. Consequently, the phase shift is inverted in postprocessing with the coefficient $s = -1$. The values of the phase difference are between -2π and $+2\pi$, thus the total phase shift $\Delta\varphi$ has to be unwrapped with multiples of 2π

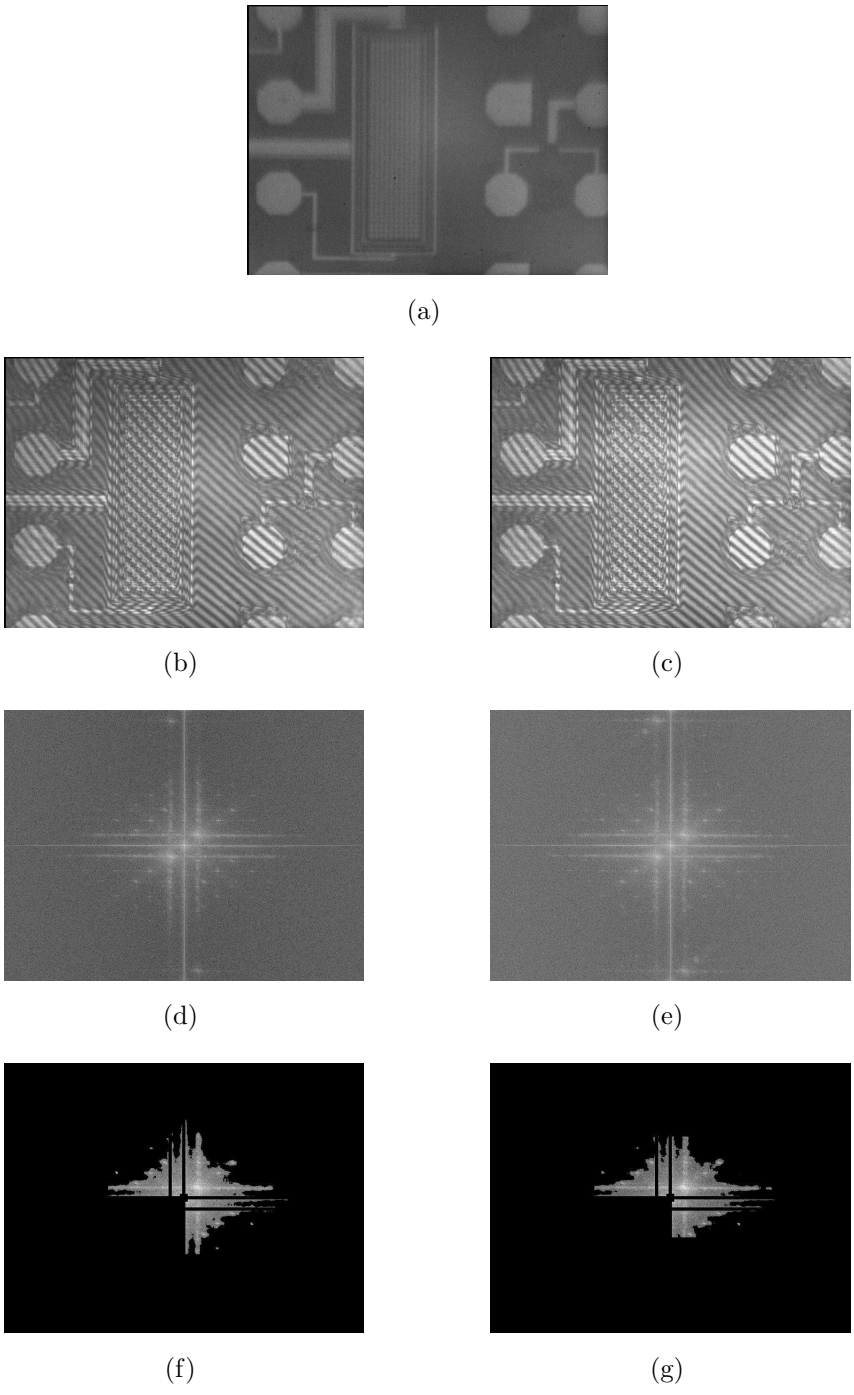
$$\Delta\varphi(x,y) = s\Delta\Phi'(x,y) \pm m(x,y)2\pi. \tag{A.29}$$

Several unwrapping approaches for two-dimensional phase maps (e.g. straightforward, pixel queue, minimum spanning tree) are reviewed by *V. Dubec* [69]. The final phase

[15] In order to clearly distinguish between phase of unstressed images and phase of the reference branch the usually called *reference* images are here called *unstressed* interferogram images.

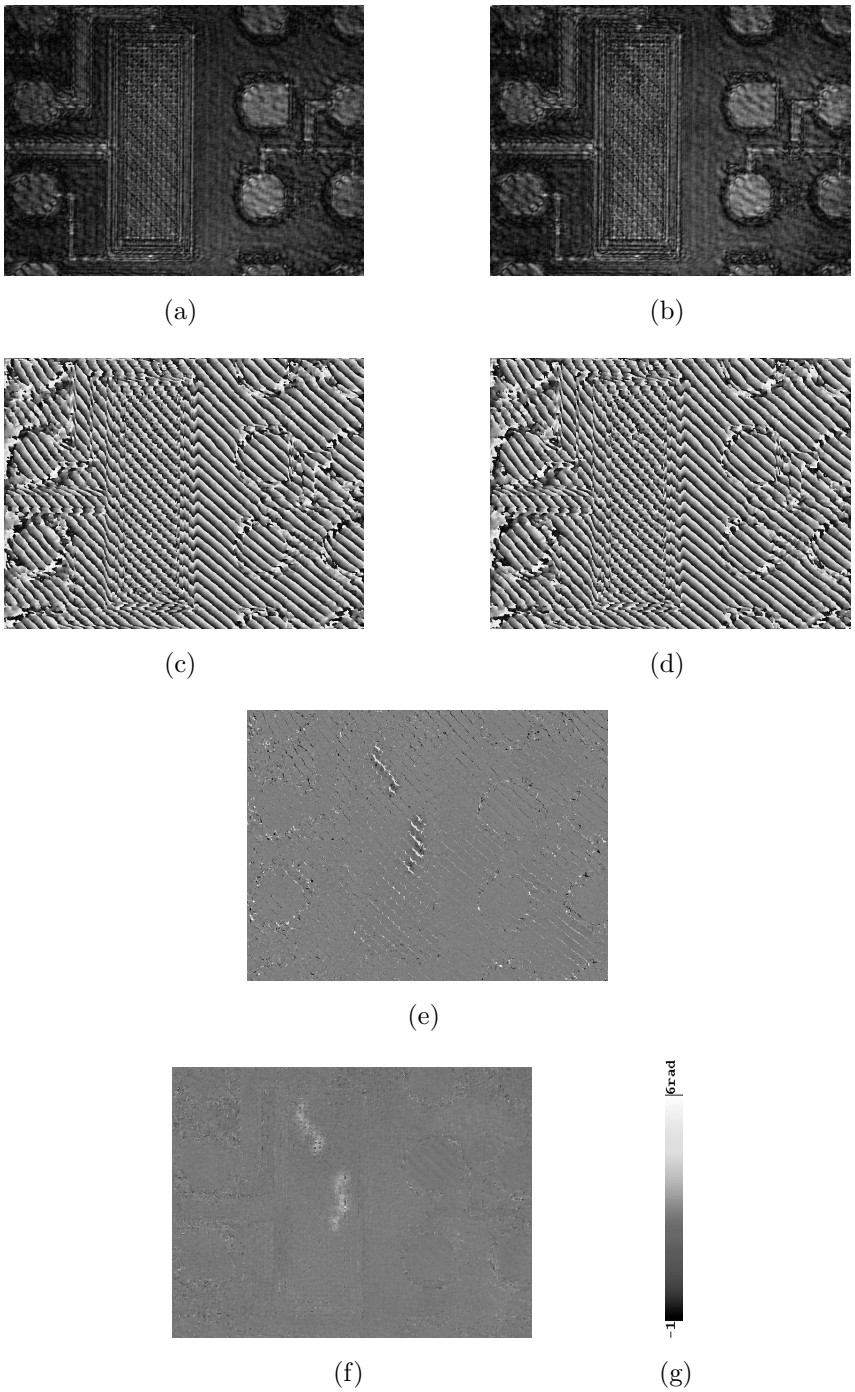
[16] For opposite inclination of the reference mirror no inversion is required ($s = 1$).

shift image is shown in Figure A.5f. Figure A.5g shows the corresponding phase scale. Further variants of TIM setups are described by *V. Dubec* in [69] and by *G. Haberfehlner* in [130, 131].



(a) (b) (c) (d) (e) (f) (g)

Figure A.4: Two-dimensional phase shift extraction. (a) Backside infrared image. (b) Unstressed interference image. (c) Stressed interference image. (d) Unstressed FFT image. (e) Stressed FFT image. (f) Unstressed masked FFT image. (g) Stressed masked FFT image.



(a) (b) (c) (d) (e) (f) (g)

Figure A.5: Two-dimensional phase shift extraction. (a) Unstressed IFFT amplitude image. (b) Stressed IFFT amplitude image. (c) Unstressed IFFT phase image. (d) Stressed IFFT phase image. (e) Subtracted phase images with negative phase shift. (f) Unwrapped and *inverted* phase image showing two heated regions (current filaments). (g) Phase scale.

Appendix B

Refocusing system

The TIM scanning of large chip areas requires a very precise alignment of torsion and inclination angles of the device under test in the setup to avoid defocusing of the laser beam during scanning long distances. Therefore, an automated laser beam refocusing[1] system is developed, which avoids defocusing during scanning. A piezoelectric actuator compensates inclination misalignments of the sample in the scanning setup up to 80 µm in vertical direction. The z-stage with manual actuator and piezoelectric actuator is shown in Figure B.1. The refocusing system requires *teach-in programming* at three good reflecting points. After this calibration it calculates for the current position a vertical correction value and applies the corresponding voltage to a piezoelectric actuator. A screenshot of the adapted scanning software *heterodyne.vi* [108] is shown in Figure B.2.

A further enhancement compensates for torsion misalignments – thus the mechanical alignment of the device under test is greatly facilitated. The compensation of torsion angles is realized by *teach-in programming* of a second coordinate system with three orthogonal points in the IR image and corresponding matrix operations [7].

[1] An auto-focus system will have problems at edges (scattered laser beam) and at non-reflecting areas of the chip. Further the global maximum of the reflected beam is at the silicon surface and not in the active layer.

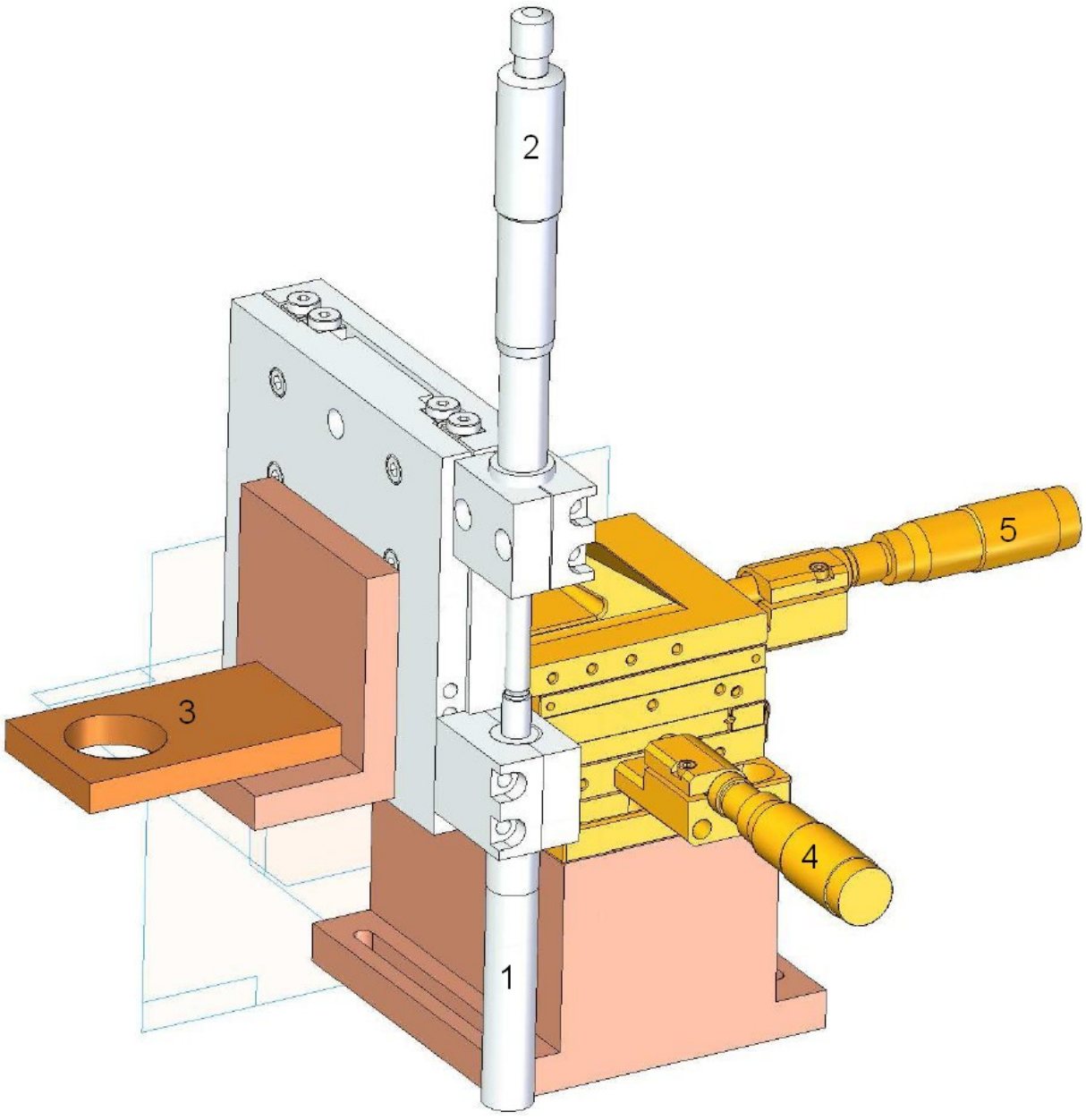


Figure B.1: Engineering drawing of the refocusing system. ("1") Piezoelectric actuator; ("2") Manual focusing screw; ("3") Microscope objective holder; ("4") and ("5") lateral alignment of microscope objective.

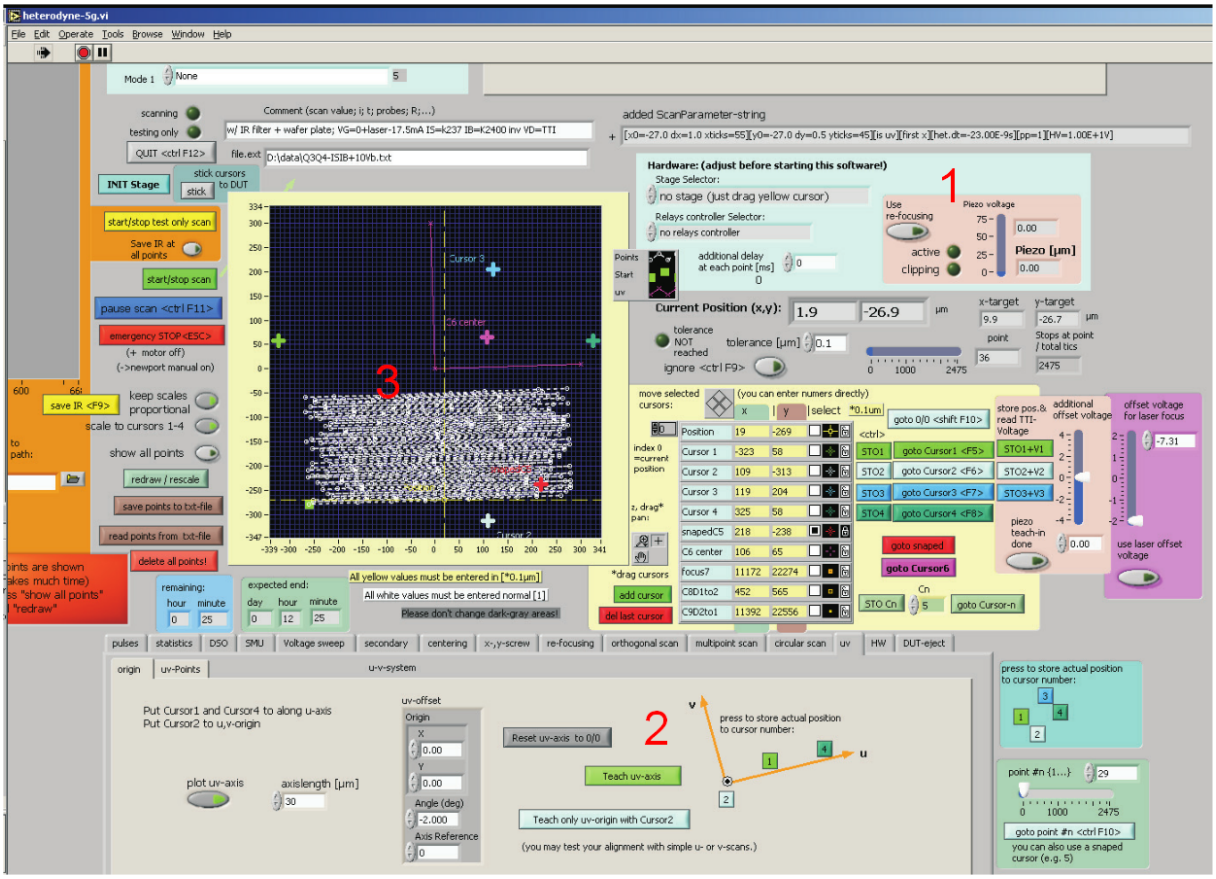


Figure B.2: Screen shot of the heterodyne scanning software *heterodyne.vi* with refocusing feature ("1") and second coordinate system ("2"). To speed up the user interface, several scanning points in the coordinate field ("3") can be skipped during redraw.

Acronyms

2D two dimensional

a.u. arbitrary unit

AC alternating current

AOM acousto-optic modulator

BB beam blocker

BCD technology combined bipolar, CMOS and DMOS technology

BOX buried oxide

BS beam splitter

CCD charge coupled device (camera)

CMOS complementary metal oxide semiconductors

cw continuous wave

DC direct current

DET detector

DMOS double diffused MOS

DSO digital sampling oscilloscope

DUT device under test

ESD electrostatic discharge

FFT fast Fourier transform

GND ground potential

HBM human body model

I-V characteristics current-voltage characteristics

I/O input/output

IC integrated circuit

IEC international electrotechnical commission

IFFT inverse fast Fourier transform

IR infrared

LU latch-up

M mirror

MOS metal oxide semiconductors

NMOS negative channel metal oxide semiconductors

$\mathbf{n_{sub}}$ n substrate (or n well) contact

PA power amplifier

PBS polarized beam splitter

PCB printed circuit board

PMOS positive channel metal oxide semiconductors

$\mathbf{p_{sub}}$ p substrate (or p well) contact

RH relative humidity

SCR silicon-controlled rectifier

Si silicon

$\mathbf{SiO_2}$ silicon dioxide

SOI silicon-on-insulator

SPI serial peripheral interface

SPICE simulation program with integrated circuit emphasis

TCAD technology CAD (computer-aided design for semiconductor manufacturing technology)

TIM transient interferometric mapping method

TL transmission line

TLP transmission line pulse

TLU transient latch-up

USB universal serial bus

VDD drain supply voltage (common drain voltage)

VIA vertical interconnect access

VSS source supply voltage (common source voltage, e.g. ground)

List of frequently used symbols

$\Delta\varphi$ phase shift

ΔN carrier concentration change

Φ instantaneous phase

ϵ_0 permittivity of free space ($8.854187817 \cdot 10^{-12}$ F/m)

λ wavelength

μ_0 permeability of free space ($1.256637061 \cdot 10^{-6}$ H/m)

τ time constant, lifetime

τ_d dielectric relaxation time

$\Im$ imaginary part of complex number

$\Re$ real part of complex number

c_0 speed of light in free space (299792458 m/s)

D diffusion coefficient

$\frac{\mathrm{d}n}{\mathrm{d}T}$ thermo-optic coefficient

E electric field

e Euler's number (2.718281828)

f frequency

I intensity of light

j imaginary unit

k_B Boltzmann constant ($1.380658 \cdot 10^{-23}$ J/K)

k_p wave number of probe beam

L spatial decay constant, diffusion length

L_D Debye length

n refractive index

n_e electron concentration

p_h hole concentration

q electronic charge ($1.60217733 \cdot 10^{-19}$ C)

T temperature

t time

W engergy

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Poster Presentations

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