DISSERTATION

Three-Phase AC-Simulator with Virtual Output Impedance Emulation

ausgeführt zum Zwecke der Erlangung des akademischen Grades
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Kurzfassung

Netzgebundene leistungselektronische Komponenten, wie z.B. Photovolatikwechselrichter, Batteriespeichersysteme oder doppeltgespeiste Asynchronmaschinen gewinnen immer mehr an Bedeutung für die Erzeugung elektrischer Energie. Dabei sinkt der Anteil konventioneller Energieerzeuger, basierend auf rotierenden Synchrongeneratoren, im elektrischen Energienetz und führt so zu einer Reduktion der Schwungmasse. Diese Schwungmasse stellt eine Energie- und Regelreserve für das elektrische Energienetz dar und ist daher ein wichtiger Parameter bei der Planung und Betriebsführung. Um das elektrische Energienetz stabil zu betreiben, wird für moderne netzgebundene Wechselrichter ein zunehmend komplexeres und entsprechend der aktuellen Netzsituation adaptives Betriebsverhalten gefordert. Dies betrifft Eigenschaften wie z.B. Blindleistungsmanagement, Primärregelfunktionen oder Low-Voltage-Ride-Through (LVRT-) Funktionalität. Um das zu erwartende Verhalten des netzgekuppelten Umrichters für unterschiedliche Netzzustände zu prüfen, ist es nötig unterschiedliche Tests sowohl simulativ als auch in geschützter Laborumgebung vorab, mit einfacher Modifizierbarkeit der Testparameter, durchzuführen. Dabei kommen i.d.R Netzsimulatoren zur Emulation von Frequenz- und Spannungsprofilen zum Einsatz. Weiters wird gefordert, dass das Betriebsverhalten des Umrichters auch für diverse resisitve und induktive Anteile der Netzimpedanz nachgewiesen werden muss. Bei konventionellen Prüfanlagen erfolgt die Nachbildung solcher Netzimpedanzen üblicherweise durch Vorschaltung physischer Widerstände und Induktivitäten, was in der Folge hohe Investitionskosten und elektrische Verluste im Betrieb nach sich zieht sowie auch die Flexibilität der Prüfeinrichtung beeinträchtigt. Ein Ansatz um dieses Problem zu verbessern, ist die Integration einer virtuellen Impedanz in die Regelung des Netzsimulators, womit resistives bzw. induktives Netzverhalten emuliert werden kann, ohne diese in ihrer physischen Form zu benötigen. Dies ermöglicht sowohl eine Reduktion der Anschaffungskosten als auch der elektrischen Verluste und dadurch eine Verbesserung des Wirkungsgrads der Anlage. Die vorliegende Dissertation beschäftigt sich mit der Entwicklung eines Netzsimulators mit variabler virtueller Impedanz für den normgemäß meist relevanten Frequenzberecih bis zu 2 kHz. Grundsätzlich könnten solche Netzsimulatoren mit Linear-Leistungsverstärkern realisiert werden, allerdings besitzen Schaltverstärker einen deutlich höheren Wirkungsgrad und sind für hohe Leistungen jedenfalls zu bevorzugen. Aufgrund der Forderung einer Bandbreite des Systems von 2 kHz, ist allerdings eine Schaltfrequenz von bis zu 200 kHz notwendig um Effekte und Einflüsse des LC-Ausgangsfilters zu minimieren. Dazu werden mehrere Topologien diskutiert, wobei für die Prototypenentwicklung initial ein 2-Level Wechselrichter gewählt wurde. Eine einstufige Realisierung hat allerdings gezeigt, dass die Messgenauigkeit/Auflösung und Bandbreite topolo-

giebedingt limitiert ist. Daher wird im Weiteren ein kaskadierter Ansatz untersucht, wobei der ursprüngliche Schaltverstärker in zwei Subsysteme aufgeteilt, nämlich einen Kleinsignal- und Großsignalverstärker. Dabei erzeugt der Großsingalverstärker eine möglichst ideale, impedanzfreie grundfrequente Netzspannung, während der Kleinsignalverstärker ausschließlich zur Emulation des Spannungsabfalls der virtuellen Netzimpedanz herangezogen wird. Im Vergleich zur einstufigen Lösung erlaubt die kaskadierte Variante die Realisierung eines Gesamtsystems mit erhöhter Auflösung/Genauigkeit bei gleichzeitig höherer Bandbreite. Eine Auslegung der Topologie sowie die Implementierung des Regelungskonzepts werden hier ausführlich behandelt. Die Validierung dieses Konzepts wird im Zeitbereich sowie im Frequenzbereich durchgeführt und erfolgt weiters unter Verwendung von nichtlinearen Lasten, wie z.B. einem dreiphasigen Diodengleichrichter (B6 Gleichrichter).

Abstract

Nowadays, the development as well as the market of components for distributed generation, namely photovoltaic inverters, battery management systems or small wind turbines, has increased significantly. A majority of these distributed generation systems are based on grid-tied converters, which are replacing conventional generators e.g. synchronous generators in the power grid resulting in a reduction of grid inertia. The grid inertia, however, represents an essential part of the control characteristic and stability and is also an important parameter for the system planing and operation for the electrical power grid. In order to support the power grid, the requirements for grid-tied inverters are getting more complex and adaptive operating behaviour according to the actual grid conditions is needed. Therefore several grid support functions were developed and have to be implemented for such grid-tied converters, in order to assist with system frequency control, voltage control or low-voltage ride through (LVRT) capability. Consequently, for the development and integration of smart-grid converters advanced testing procedures are required, which are mainly based on tests in a safe laboratory environment. For this purpose controllable AC power sources (AC-simulators) with adjustable grid characteristics (e.g. frequency and voltage profiles) are mandatory. AC-simulators can also perform simulations of transient grid behaviour as well as grid faults. With more sophisticated grid connected units like photovoltaic inverters, electric vehicles etc., not only the output voltage or output current are required as test parameters, additionally the corresponding grid impedance emulation is needed which further affects the performance of the application. Conventional test setups usually are emulating the grid impedance by using real inductors and resistors, which leads to high investment costs and also electrical losses during operation. One approach to improve this situation is the integration of a virtual impedance into the controller algorithm of the AC-simulator in order to emulate the resistive-inductive grid behaviour without need of bulky hardware. This enables a reduction in both the investment costs and the electrical losses improving the efficiency of the system at increased flexibility. The main focus of this thesis remains on the development of an AC-simulator with variable virtual grid impedance emulation for frequencies up to 2 kHz being defined in EMI regulations and grid codes. For the implementation of such a system, linear power amplifier could be used theoretically, however resulting in very low efficiency. Consequently, switched-mode power amplifiers showing much higher efficiency rates today and are generally preferred for AC power sources. In order to achieve the small-signal frequency up to 2 kHz, basic analyses show switching and sampling frequencies in the region of up to 200 kHz are required to achieve the intended dynamic behaviour at low output voltage noise levels. For this purpose, several topologies are investigated,

whereby for the prototype development initially a 2-level inverter was chosen. However, the single-stage system showed some limitations in terms of accuracy of current and/or voltage measurements. Furthermore, also the bandwidth of the emulated impedance is limited if both fundamental and harmonic components (i.e. impedance voltage drop) will be generated by only one three-phase switched-mode amplifier. These restrictions can be avoided by splitting-up the three-phase AC-simulator system into two separate converter topologies connected in series concerning their respective output voltages feeding in total the equipment under test. In fact the virtual impedance now is emulated by the small signal amplifier whereas the main (large signal) power amplifier provides the fundamental grid voltage. Therefore, voltage sensors with higher resolution can be employed for the impedance emulation. Compared to the single stage topology, the cascaded concept enables improved measurement resolution/accuracy and at the same time increased bandwidth. Based on this concept a two-level topology was selected for the laboratory prototype verification. The dimensioning of the topology was analytically described an a proper control method was developed an implemented as a laboratory prototype. Finally, a validation and analysis, of such a system feeding also non-linear loads (e.g. three-phase B6 rectifier) is also presented.

Contents

Chapter 1

Introduction

1.1 Motivation

The utilisation of renewable energy has led to a raising penetration of distributed energy resources (DER), which are typically using renewable energy sources (e.g. wind power, solar power, biomass). Such DER are mainly based on power electronic converter systems e.g.: photovoltaic (PV) inverters, double fed induction generators (DFIG) for wind turbines or battery energy storage systems (BESS). The increasing share of power electronic inverters raises new challenges for the management and operation of power grids, in terms of voltage variations in distribution systems and frequency stability issues. Thus, there is a continuous improvement of grid standards and requirements for operation of DER systems and for this purpose the development of grid tied power electronic inverters have gained more and more importance during the last decades. As a consequence existing grid standards are incessantly and also new standards are introduced .

Testing and validation of grid support functions (such as low-voltage-ride-through (LVRT), virtual inertia (VI) or enhanced frequency response (EFR)) of such grid-tied inverters under various grid conditions is mandatory. Since this cannot be fully covered by field tests, laboratory tests with controllable AC power sources (AC-simulators) for the emulation of voltage dips, frequency profiles or other grid characteristics are required.

AC-simulators enable the control ability of any grid characteristics and adjustable grid conditions during development and validation phase [1]. Furthermore also transient grid behaviour (e.g. flicker) can be simulated and analysed. In addition to the generation of voltage or frequency profiles, the simulation of the grid impedance characteristic is also mandatory.

Conventional AC-simulator systems are using passive components for the emulation of the grid impedance. On the one hand, this a simple and robust method for the emulation of a grid impedance. On the other hand it is costly and bulky hardware, which also causes losses during operation. In Fig. 1.1 (a) the equivalent circuit of the concept of a conventional AC-simulator with passive impedance emulation is depicted. A more flexible and compact approach is the emulation of the grid impedance by means of virtual impedance concept. Since the AC-simulator itself is a controlled power amplifier, the emulation of the grid impedance can be implemented directly into the control scheme. Fig. 1.1 (b) shows the equivalent

circuit of the concept of a advanced AC-simulator with virtual impedance emulation. For this, the output current of each phase of the whole system is measured and used as feedback for the virtual impedance emulation. The determination of the voltage drop, caused by the virtual impedance, is part of the control algorithm and and has an impact on the AC-simulator output voltage.

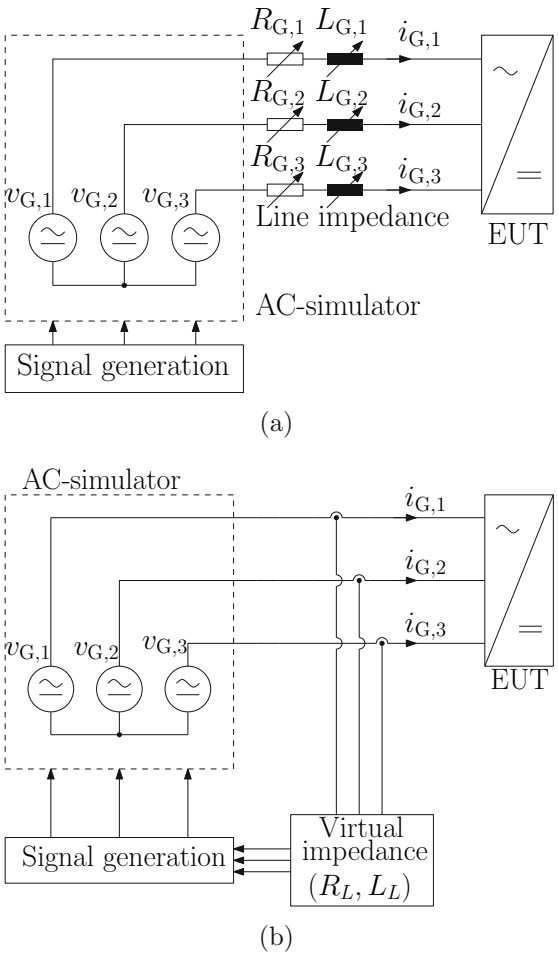


Figure 1.1: Equivalent circuit of the concept of (a) conventional AC-simulator with passive impedance emulation and (b) advanced AC-simulator with virtual impedance emulation.

Today, switched mode power amplifiers and linear power amplifiers are used for AC-Simulator applications. Linear power amplifiers have a high bandwidth, very low THD, but an efficiency below $\eta_{\text{linear,max}} = 78,5\ \%$ (theoretically maximum for class B power amplifiers at ohmic loads [2]), the switched mode power amplifier has a theoretical efficiency $\eta_{\text{switchedmode,max}}$ of 100 %. A detailed discussion of the state of the art is given in chapter 2 to give an overview of already existing topologies. Chapter 3 introduces the advanced AC-simulator concept (single-stage and cascaded concept) and fundamental issues are highlighted. Furthermore, the hardware design and control algorithm are also discussed. The cascaded advanced AC-simulator was implemented as a laboratory prototype and is described in chapter 4 including measurement results. Finally, a non linear load operation is analysed and validated by measurement results.

1.1.1 AIT SmarTEST

The AIT Smart Electricity Systems and Technologies Laboratory (SmarTEST) is a unique research and simulation laboratory in Austria regarding its electrical specifications and its applications. It is also embedded in the European Distributed Energy Resources Laboratories (DERlab association), which is an association of leading laboratories and research institutes in the field of distributed energy resources equipment and systems, developing joint requirements and quality criteria for the connection and operation of DER and supporting consistent development of DER technologies [3].

The laboratory infrastructure of SmarTEST allows the simulation, validation and testing of grid-connected inverter systems with focus on DER-devices (e.g. PV-inverter or BESS). Therefore it provides adjustable DC- and AC- voltage sources, adjustable loads and passive line impedance emulation. The laboratory is designed for testing inverter systems, battery storage systems, electric vehicle (EV) charging with rated power up to 1 MW. The laboratory can be used for either development support and comprehensive tests of inverter systems or the standard and grid code compliance validation.

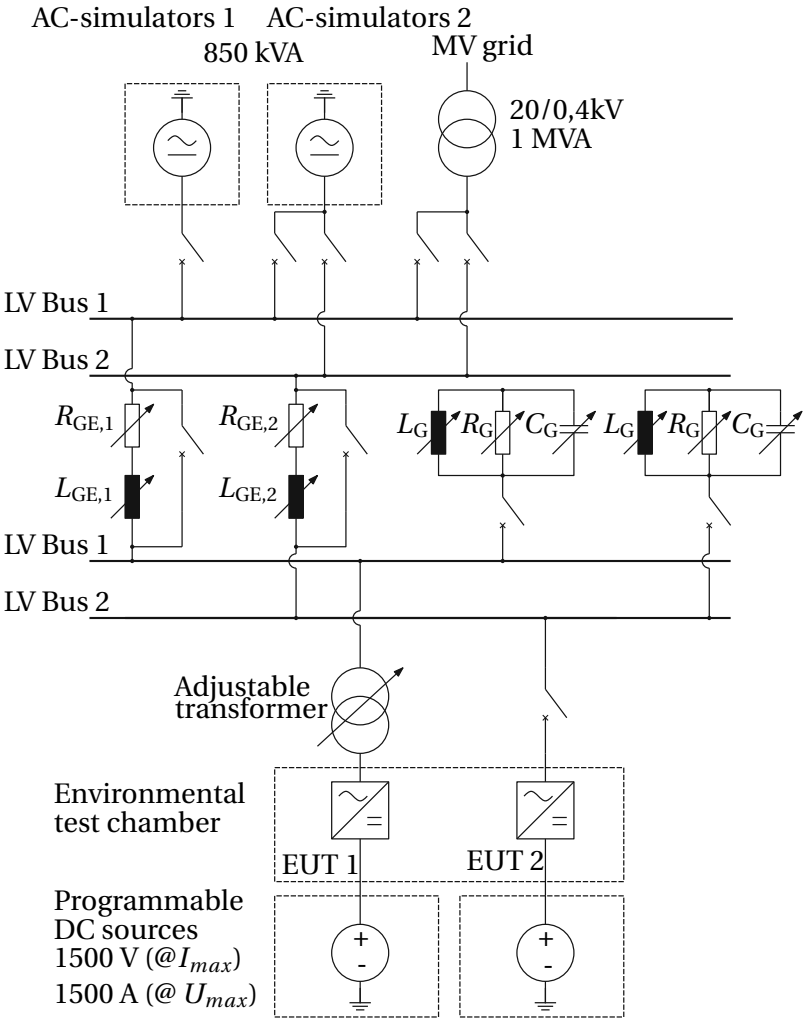


Figure 1.2: Single line diagram of AIT SmarTEST laboratory.

Fig. 1.2 shows the single line diagram of AIT SmarTEST laboratory, which

provides the following simulation and testing capabilities:

- Three-phase 4-Quadrant AC - Simulators (Grid Simulation) up to 850 kVA and 480 V
- DC-Simulators (PV-Array) up to 960 kW and 1500 V
- Line impedance emulation (adjustable passive impedances)
- Adjustable RLC loads up to 1 MW
- LVRT Test unit up to 1 MW according to IEC 61400-21

1.2 Relevant Standards

The test scenarios and the requirements for test equipment i.e. grid-tied inverters are defined by grid-codes as well as by technical standards. Based on the Low Voltage Directive (LVD) [4] and the Technical and organisational rules (TOR) [5], the following standards are relevant for grid tied inverters (e.g. PV inverter, BESS):

- Low Voltage Directive version of 2014/35/EU [4]
  - EN 62109-1:2010 - Safety of power converters for use in photovoltaic power systems - Part 1: General requirements
  - EN 62109-2:2011 - Safety of power converters for use in photovoltaic power systems - Part 2: Particular requirements for inverters
- Technical and organisational rules - Section D4: Operation of generating stations in parallel with distribution networks [5]
  - ÖVE/ÖNORM EN 50160 - Voltage characteristics of electricity supplied by public distribution networks
  - ÖVE/ÖNORM EN 50110-1 - Operation of electrical installations - Part 1: General requirements
  - ÖVE/ÖNORM EN ISO/IEC 17025 - General requirements for the competence of testing and calibration laboratories
  - ÖVE/ÖNORM EN ISO/IEC 17065 - Conformity assessment - Requirements for bodies certifying products, processes and services
  - ÖVE/ÖNORM EN 61000-4-7 Electromagnetic compatibility (EMC) - Testing and measurement techniques - General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto
  - ÖVE/ÖNORM EN 61000-4-30 - Electromagnetic compatibility (EMC) - Testing and measurement techniques – Power quality measurement methods

- ÖVE/ÖNORM EN 61000-3-2 - Electromagnetic compatibility (EMC) - Limits - Limits for harmonic current emissions (equipment input current $\leq$ 16 A per phase)
- ÖVE/ÖNORM EN 61000-3-3 - Electromagnetic compatibility (EMC) - Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current $\leq$ 16 A per phase and not subject to conditional connection
- ÖVE/ÖNORM EN 61000-3-11 - Electromagnetic compatibility (EMC) - Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems - Equipment with rated current $\leq$ 75 A and subject to conditional connection
- ÖVE/ÖNORM EN 61000-3-12 - Electromagnetic compatibility (EMC) - Limits – Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current $>$ 16 A and $\leq$ 75 A per phase
- ÖVE E 8101 Elektrische Niederspannungsanlagen
- EN 50549-1 - Requirements for generating plants to be connected in parallel with distribution networks - Connection to a LV distribution network - Generating plants up to and including Type B
- EN 50549-2 - Requirements for generating plants to be connected in parallel with distribution networks - Part 2: Connection to a MV distribution network - Generating plants up to and including Type B
- ÖVE-Richtlinie R 20 Stationäre elektrische Energiespeichersysteme vorgesehen zum Festanschluss an das Niederspannungsnetz
- OVE-Richtlinie R 25 Prüfanforderungen an Erzeugungseinheiten (Generatoren) vorgesehen zum Anschluss und Parallelbetrieb an Niederspannungs-Verteilernetzen
- VDE-AR-N 4105 Technische Mindestanforderungen für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Niederspannungsnetz
- DIN VDE V 0124-100 Niederspannung – Prüfanforderungen an Erzeugungseinheiten vorgesehen zum Anschluss und Parallelbetrieb am Niederspannungsnetz

The standard EN 61000-4-13 defines the requirements for the AC test generator. In order to fulfil this standard, such a generator has to provide a nominal fundamental voltage of $V_{\mathrm{LN}} = 230\ \mathrm{V} \pm 2\ \%$ at a nominal frequency of $f_{\mathrm{n}} = 50\ \mathrm{Hz} \pm 0.5\ \%$. Moreover, the emulation of harmonics up to the 40th harmonic of the 50 Hz fundamental signal is required. Thus, a small-signal bandwidth of up to 2 kHz is mandatory.
Another important standard is the DIN VDE V 0124-100, which defines the test requirements for grid-tied power generators. In addition to the required voltage signal accuracy, a maximum total harmonic distortion (THD) of 3% is required.
Apart from stability and grid fault tests, the EN 61000-4-13 Annex A describes an impedance network between the test generator and the EUT (according to IEC60725) for 50 Hz grids, which is relevant e.g. to identify any resonances between

the grid and the EUT caused by harmonics. For 50 Hz the following impedances are required

$$\text{Phase conductor } 0.24\ \Omega + j0.15\ \Omega \tag{1.1}$$
$$\text{Neutral conductor } \underline{0.16\ \Omega + j0.10\ \Omega} \tag{1.2}$$
$$0.40\ \Omega + j0.25\ \Omega \tag{1.3}$$

and for 60 Hz grids

$$\text{Phase conductor } 0.1\ \Omega + j0.04\ \Omega \tag{1.4}$$
$$\text{Neutral conductor } \underline{0.1\ \Omega + j0.03\ \Omega} \tag{1.5}$$
$$0.2\ \Omega + j0.07\ \Omega \tag{1.6}$$

which results in component values of

$$R_G = 0.4\ \Omega \text{ and } L_G = 795\ \mu\text{H} \tag{1.7}$$

for 50 Hz and

$$R_G = 0.2\ \Omega \text{ and } L_G = 223\ \mu\text{H} \tag{1.8}$$

for 60 Hz.

1.3 Objective and New Contributions of this Work

The main objective of this thesis is the investigation, development and validation of virtual/emulated output impedances of AC-/grid-simulators. The proposed approach reduces the volume of laboratory test infrastructure considerably, as various bulky passive RL impedance power network elements are avoided by implementation of the impedance voltage/current characteristic into the control of the AC-Simulator. A further advantage is, that such a system gives high testing flexibility, hence no manual modification of a passive impedance network is required resulting in a system which can be easily adapted to the specific test case scenario in a programmable manner.

The system discussed in this thesis is based on a series arrangement of a standard industrial AC power source providing the large-signal components (400 VAC, 50 Hz) combined with a dedicated small-signal "emulation inverter" (100 VAC, 2 kHz) intended to perform the impedance emulation. The primary research question was to clarify if virtual output impedances of the total system can be achieved with sufficient accuracy to comply with testing standards without any modification of the feeding industrial AC power source. It could be demonstrated that the implemented feed-forward compensation of the off-line determined AC power source output filter impedance and of the coupling transformer impedance results in a total system virtual test impedance precision being sufficient to perform the aimed tests according to the mentioned relevant EN/ÖVE grid testing standards. New contributions of this work are as follows:

- Comparison of a single stage approach and a cascaded system (Sec. 3.1.3)
- Design and development of a cascaded system (Sec. 3.2)
- Implementation of a small-signal inverter prototype for virtual impedance emulation (Sec.4.1)
- Analysis and development of a compensation algorithm of the large-signal inverter output impedance (Sec. 4.2)
- Time-domain and frequency domain analysis of the small signal inverter system (Sec. 4.2.1)
- Analysis of non-linear load operation of the advanced AC-simulator, demonstration of impedance precision (Sec. 4.3)

1.4 Publication and Patents

In the following the authors publications underlying this thesis shall be listed:

Jonke, P. ; Stöckl, J. ; Ertl, H.: Concept of a three phase AC power source with virtual output impedance for tests of grid connected components. In: *2015 International Symposium on Smart Electric Distribution Systems and Technologies (EDST)*, 2015, S. 399–404

Jonke, P. ; Stoeckl, J. ; Ertl, H.: Design and Performance Evaluation of a Three Phase AC Power Source with Virtual Impedance for Validation of Grid Connected Components. In: *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, S. 1–7

Jonke, P. ; Makoschitz, M. ; Sumanta, B. ; Stoeckl, J. ; Ertl, H.: AC-Sweep Analysis and Verification of an AC Power Source with Virtual Output Impedance for Validation of Grid Connected Components. In: *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, S. 1–7

Jonke, P. ; Makoschitz, M. ; Biswas, S. ; Stoeckl, J. ; Ertl, H.: Design and Verification of a Cascaded Advanced AC-Simulator with Virtual Output Impedance. In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, S. 1–8
Nominated for the Best Paper Award

Jonke, P. ; Makoschitz, M. ; Biswas, S. ; Stöckl, J. ; Ertl, H.: Output Impedance Compensation of a Cascaded Advanced AC-Simulator. In: *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, 2020, S. 761–766
Best Paper Award

Jonke, P. ; Makoschitz, M. ; Biswas, S. ; Stöckl, J. ; Ertl, H.: Analysis and Verification of a Cascaded Advanced AC-Simulator with Non-Linear Loads. In: *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, S. 1–7

Jonke, P. ; Makoschitz, M.: *Netzsimulator*. Januar 18 2018. – Patent AT 520835

Chapter 2

AC-Simulator Topologies

In the following chapter the state-of-the-art of power electronic amplifier topologies is described. For AC-simulator applications high dynamic and low output voltage distortions are required in order to comply with standards and to fulfill the requirements for the test setup (e.g. EN 61000-4-13, ÖVE-Richtlinie R25, VDE V 0124-100).

Power electronic amplifier systems can be classified into systems based on linear amplifiers or switched-mode amplifiers, depicted in Fig. 2.1.

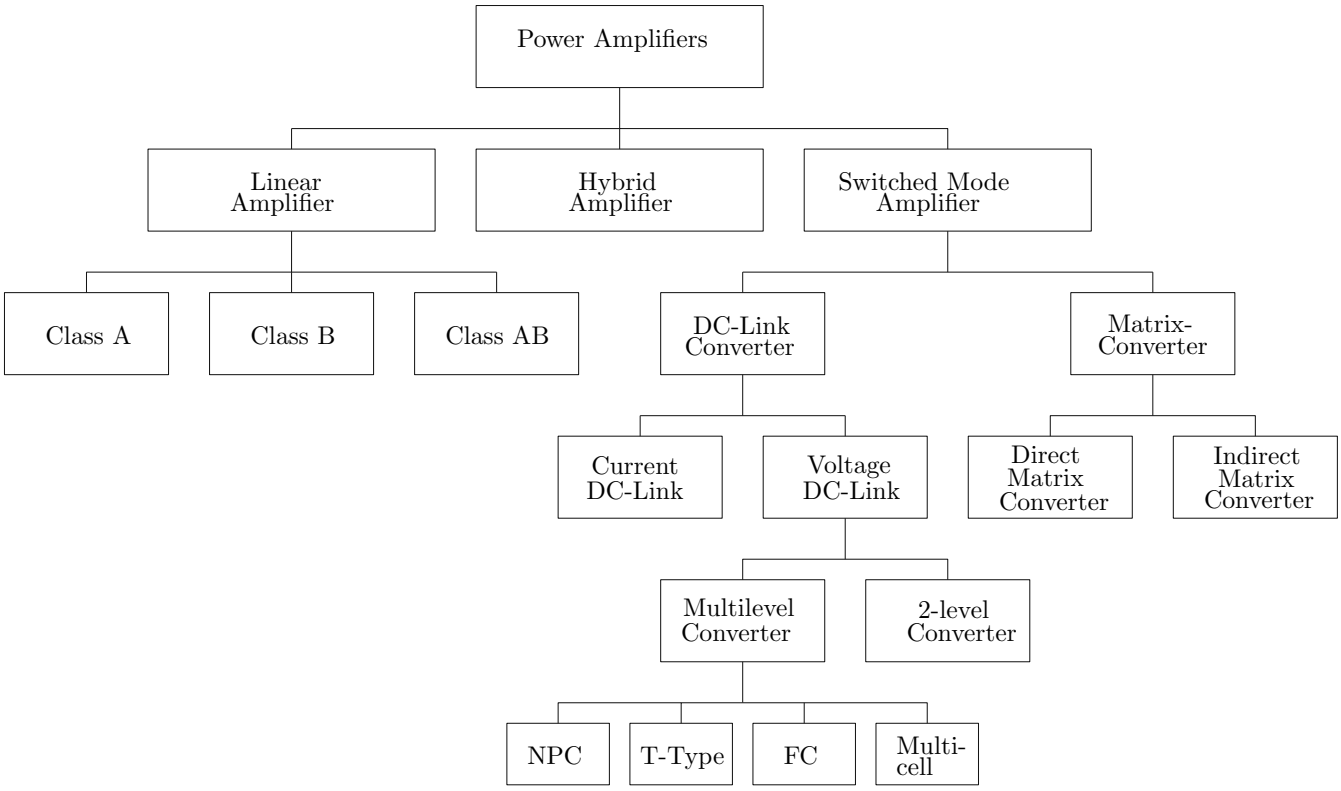


Figure 2.1: Overview of power electronic amplifier systems implemented as either linear or switched-mode amplifier as discussed in [13],[14].

Linear amplifiers are mainly based on discrete transistor circuits with two active devices (class-A amplifier, class-B amplifier, class-AB amplifier). In principle a bipolar power transistor or a specific MOSFET can be used for such power

amplifiers. The amplifier class is depending on the ratio between the current conduction time of the output transistor based on the input signal period.

- Class-A amplifiers: Are showing a conducting angle of $\theta = 360°$ which means that the full input signal is used. Therefore the class-A amplifier shows almost linear behaviour.
- Class-B amplifiers: Each output transistor of a class-B amplifier shows a conducting angle of $\theta = 180°$, therefore a complementary arrangement with two transistors is mandatory. The maximum efficiency of a class-B amplifier is defined by $\eta = 78.5\ \%$ (theoretical maximum at maximum output voltage).
- Class-AB amplifiers: Are less efficient than class-B amplifiers, but each output transistor has a conducting angle of $\theta \approx= 200°$ due to the quiescent current, which reduces the crossover distortion, but also the efficiency of the amplifier.

Switched-mode amplifiers which are also known as class-D amplifiers have a switched-mode converter stage and a low-pass output filter. The switched-mode converter can be a direct AC-AC converter topology (Matrix converter) or a DC-AC converter topology (e.g. voltage DC-link converter, current DC-Link converter).

- AC-AC Converter: A Matrix converter allows a direct energy conversion between the three-phase power grid (50 Hz/60 Hz) and the emulated low-voltage grid with the EUT. Since the topology as well as the control design of such matrix converters is quite elaborate and complex they are not widely used in industrial applications.
- DC-AC Converter: DC-link converters are a much more commonly used solution, where a DC-link capacitor or DC-link inductor is used as a decoupling energy storage between the input supply and the output load. The high efficiency of such a switched-mode amplifier is the main advantage of this system. MOSFETs or IGBTs are used as electronic switches which are operated in pulse-width modulation (PWM) and a subsequent passive output filter (e.g. LC filter) which averages the PWM output voltage to an analogue signal.

2.1 Linear Amplifiers

2.1.1 Class-A Amplifier

A class-A power amplifier based on the complementary emitter follower circuit with quiescent current is shown in Fig. 2.2. The circuit has a bipolar DC-supply voltage (V_S) and two active devices, a bipoloar npn-transistor and a pnp-transistor. In

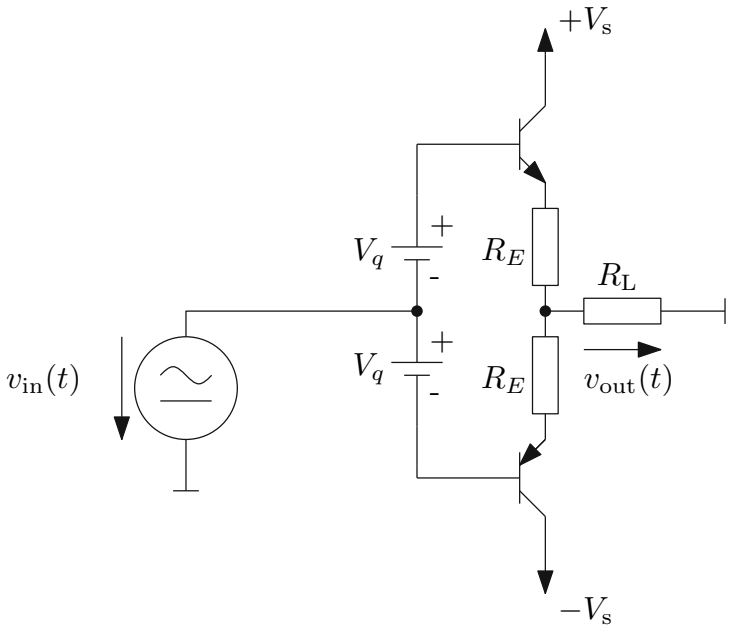


Figure 2.2: Class-A linear amplifier - complementary emitter follower circuit with quiescent current.

order to ensure a positive transistor current for the NPN transistor, the quiescent current is defined by

$$I_{\mathrm{q}} \geq \frac{\hat{I}_{\mathrm{out}}}{2} = \frac{1}{2}\frac{\hat{V}_{\mathrm{out}}}{R}. \tag{2.1}$$

However, the average power dissipated by the output resistor with an sinusoidal output voltage $v_{\mathrm{out}}(t) = \hat{V}_{\mathrm{out}} \cdot \sin(\omega t)$ and the corresponding output current $i_{\mathrm{out}}(t) = \frac{\hat{V}_{\mathrm{out}}}{R_{\mathrm{L}}} \cdot \sin(\omega t)$ results in

$$P_{\mathrm{out}} = \frac{\hat{V}_{\mathrm{out}}^2}{T \cdot R_{\mathrm{L}}} \int_0^T \sin^2(\omega t) dt = \frac{\hat{V}_{\mathrm{out}}^2}{2 \cdot R_{\mathrm{L}}}. \tag{2.2}$$

On the other hand the average output power of the DC-supply, assuming a sinusoidal output voltage, neglecting the base current ($I_{\mathrm{B}} \cong 0$) and the emitter resistance ($R_{\mathrm{E}} \cong 0$), is given by

$$\begin{aligned} P_{\mathrm{S}} =& \frac{2}{T} \int_0^T V_{\mathrm{S}} \cdot i_{\mathrm{s}}(t) dt = \frac{2}{T} \int_0^T V_{\mathrm{s}} \left(I_{\mathrm{q}} + \frac{1}{2} \frac{\hat{V}_{\mathrm{out}}}{R_{\mathrm{L}}} \sin(\omega t) \right) dt = \\ =& \frac{2}{T} \frac{V_{\mathrm{s}} \hat{V}_{\mathrm{out}}}{2 R_{\mathrm{L}}} \int_0^T (1 + \sin(\omega t))\, dt = \frac{V_{\mathrm{s}} \hat{V}_{\mathrm{out}}}{R_{\mathrm{L}}}. \end{aligned} \tag{2.3}$$

Thus, the theoretical maximum efficiency of a Class A amplifier results in

$$\eta_{\mathrm{A,max}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{s}}} = 50\%. \tag{2.4}$$

The common collector (emitter follower) would be another type a class-A amplifier. According to [15] the efficiency of a bipolar common collector circuit with impedance matching ($R_L = R_E$) however is given by only

$$\eta_{\mathrm{A,max}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{s}}} = \frac{2V_{\mathrm{s}}^2}{2 \cdot 16V_{\mathrm{s}}^2} = 6,25\%. \tag{2.5}$$

2.1.2 Class-B Amplifier

The low efficiency of the class-A amplifier is mainly caused by the permanent passing collector current, even at the quiescent operating point. The complementary emitter follower amplifier in class-B operation mode avoids this disadvantage of a class-A amplifier. The circuit for the class-B linear amplifier - complementary emitter follower amplifier can be seen in Fig. 2.3 and consists again of a high-side and a low-side bipolar transistor. Since a single transistor of the complementary emitter follower amplifier only conducts one half period, there is a cross-over region where the current commutates from the upper to the lower transistor. However, a crossover distortion appears which is caused by the emitter base threshold voltage of the transistors.

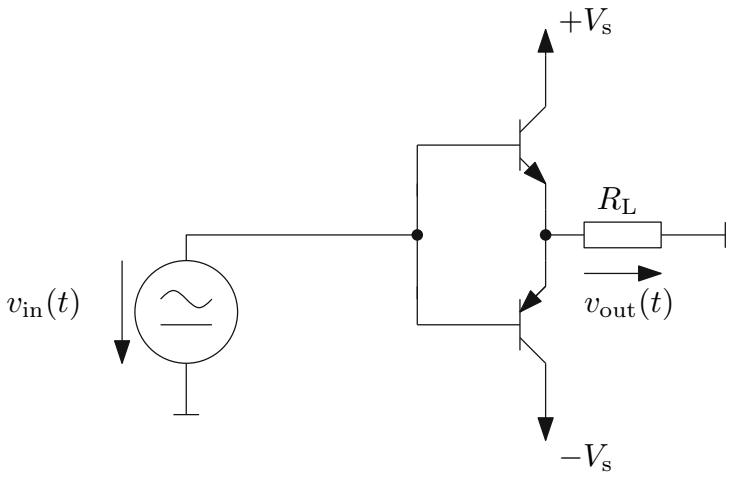


Figure 2.3: Class B linear amplifier - complementary emitter follower amplifier.

The average power dissipated by the output transistor with an sinusoidal output voltage $v_{\mathrm{out}}(t) = \hat{V}_{\mathrm{out}} \cdot \sin(\omega t)$ and the corresponding output current $i_{\mathrm{out}}(t) = \frac{\hat{V}_{\mathrm{out}}}{R_{\mathrm{L}}} \cdot \sin(\omega t)$ results in

$$P_{\mathrm{out}} = \frac{\hat{V}_{\mathrm{out}}^2}{T \cdot R_{\mathrm{L}}} \int_0^T \sin^2(\omega t) dt = \frac{\hat{V}_{\mathrm{out}}^2}{2 \cdot R_{\mathrm{L}}}. \tag{2.6}$$

The output power of the DC-supply is given by

$$P_{\mathrm{s}} = \frac{1}{T/2} \int_0^{T/2} V_{\mathrm{S}} \cdot i_{\mathrm{out}}(t) dt = \frac{2 \cdot V_{\mathrm{S}} \hat{V}_{\mathrm{out}}}{\pi R_{\mathrm{L}}}. \tag{2.7}$$

For $\hat{V}_{out} = V_s$ the theoretical maximum efficiency can be derived by

$$\eta_{\mathrm{B,max}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{s}}} = \frac{\pi}{4} = 78,5\ \%. \tag{2.8}$$

2.1.3 Class-AB Amplifier

The crossover distortion of a pure class-B amplifier can be reduced, if each transistor conducts the current more than half of the period ($\theta > 180°$). Due to the extended conducting angle the dead zone of the amplifier is reduced and also the crossover distortion is reduced. This can be achieved by applying a bias voltage V_{q}, which causes a small quiescent current on each transistor. For very low output currents the class-AB amplifier (circuit identical to Fig. 2.2) in fact operates in class-A mode. The bias voltage of the transistor can be achieved in various ways via a preset bias voltage, a voltage divider network or diodes connected in series. The additional quiescent current causes also somewhat more losses compared to a pure class-B amplifier operation and thus realistic efficiencies are in the range of $\eta_{AB,max} \cong 65\ \%$.

2.2 Switched-Mode Amplifiers

2.2.1 DC-link Two-Level

The principle of a switched-mode amplifier, also known as Class D amplifier, is based on a pulsed power semiconductor switch (IGBT or MOSFET) with a corresponding passive output filter. Since an ideal switching element has no losses, the theoretical maximum efficiency of a switched-mode amplifier is $\eta_{\mathrm{D,max}} = 100\ \%$. Considering conduction losses, switching losses and passive filter losses the typical efficiency of a switched-mode inverter is in a range of $\eta_{\mathrm{D}} = 92\ \% \ldots 99\ \%$. Therefore such amplifiers are preferred for high power applications. The topology of the bidirectional DC-link two-level inverter is shown in Fig. 2.4. Such an inverter is widely used for low-voltage grid applications (e.g. PV-inverters, BESS). The DC-link of the proposed inverter has a midpoint connection, benefiting from symmetrical voltage generation, however, causing the disadvantage of increasing current ripple with switching frequency. In order to control the semiconductor switches a pulse-width-modulation (PWM) signal is used to turn on and off the active switches according to the applied modulation signal. The switching frequency $f_{\mathrm{s}} = \frac{1}{T_{\mathrm{s}}}$ is depending on the switching speed of the power semiconductor devices and is typically in the range of 1 kHz ... 1 MHz [16]. The output voltage of the inverter is determined by the duty cycle which is defined by

$$\delta = \frac{T_{\mathrm{on}}}{T_{\mathrm{s}}} \tag{2.9}$$

where T_{on} is the pulse active time and T_{s} the total period time of the signal. For

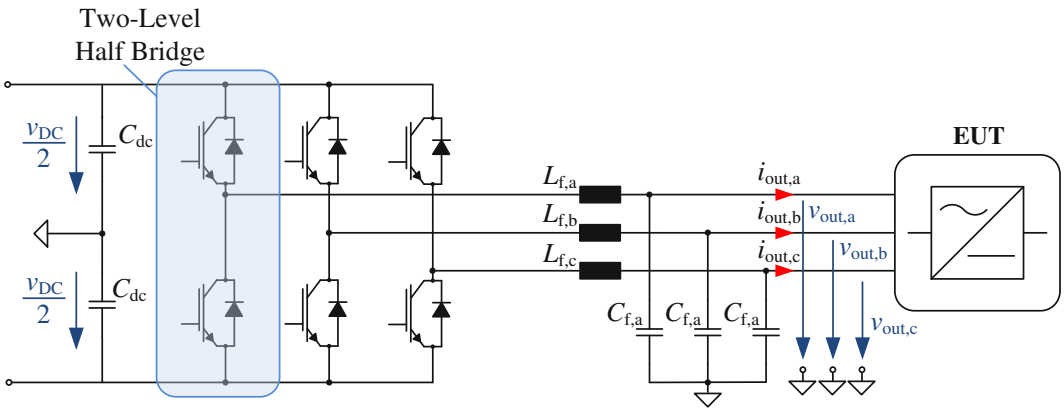


Figure 2.4: DC-link two-level inverter.

single half bridge circuits a PWM signal with the duty cycle δ is used for the high side switch and the complement of the duty cycle $1 - \delta$ is used for the low-side counterpart. Therefore the output voltage of a half bridge is defined by

$$v_{\mathrm{out,HB}} = \begin{cases} +\frac{V_{\mathrm{DC}}}{2}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ -\frac{V_{\mathrm{DC}}}{2}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{2.10}$$

In order to generate sinusoidal output voltages with a maximum peak voltage of $\hat{V}_{\text{out,LN,max}} = 325$ V, a DC-link voltage of 800 V is required, thus the power semiconductors are rated for a blocking voltage of 1200 V to allow an additional safety margin for high voltage spikes during commutation activity. Moreover, such an inverter requires a passive LC output filter, in order to obtain a clean sinusoidal output voltage without harmonic content. The cut-off frequency $f_{\text{c,LC}}$ of such a filter depends on the switching frequency f_{s} and the signal bandwidth f_{bw} of the inverter system, in order to reduce the noise caused by the switching power semiconductors. To avoid significant phase shift and amplitude reduction of the output signal the cut-off frequency has to be in the range of $f_{\text{c,LC}} \approx 10 \cdot f_{\text{bw}}$. However, a two-level inverter represents a simple option for the implementation of an AC-simulator with high efficiency.

2.2.2 DC-link Multilevel

Multilevel inverter are gaining more and more importance in scientific as well as in industrial applications. In general, multilevel inverter usually show improved power density because of the reduced output filter volume and less harmonic distortion compared to a conventional two-level inverter [17, 18]. As opposed to a two-level inverter, a multilevel inverter has several intermediate voltage levels which enables a more accurate signal modulation with lower harmonic distortion. However, the number of power semiconductors also increases with the voltage levels, which results in a more complex modulation and control scheme. Fig. 2.5 shows the basic principle of a three-level inverter. It has to be noted, that a vari-

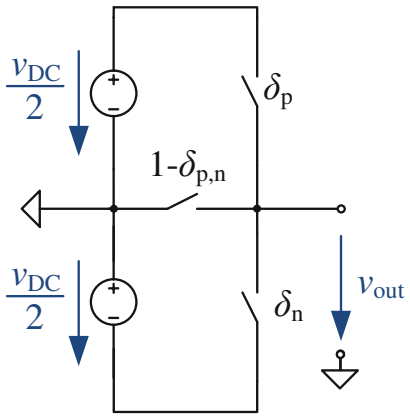


Figure 2.5: DC-link three-level basic principle based on ideal switches

ety of multilevel topologies exist, but for further consideration only the two most common three-level types (neutral point clamped (NPC) inverter [19–21] Fig. 2.6 and three-level T-type inverter [22] Fig. 2.7) are considered . The output voltage

of a three-level leg in general is defined by

$$v_{\text{out,3-level}} = \begin{cases} +\frac{V_{\text{DC}}}{2}, 0 \leq t < \delta_{\text{p}} \cdot T_{\text{s}}, v^*_{\text{out}} > 0 \\ -\frac{V_{\text{DC}}}{2}, 0 \leq t < \delta_{\text{n}} \cdot T_{\text{s}}, v^*_{\text{out}} < 0 \\ 0, \delta_{\text{p}} \cdot T_{\text{s}} \leq t < T_{\text{s}} \;\&\; \delta_{\text{n}} \cdot T_{\text{s}} \leq t < T_{\text{s}}. \end{cases} \tag{2.11}$$

where δ_{p} denotes the duty cycle for positive output voltages and δ_{n} denotes the duty cycle for negative output voltages. Fig. 2.6 shows a three-phase three-level neutral point clamped (NPC) inverter, where one bridge-leg consists of four power semiconductor switches and two additional clamping diodes. The operating

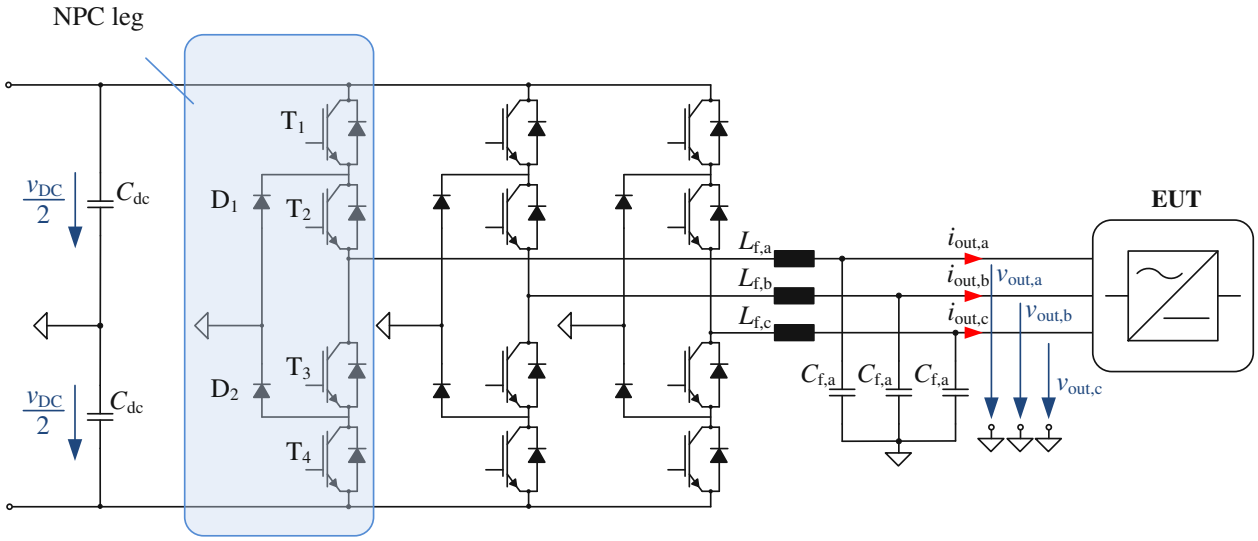


Figure 2.6: DC-link three-level neutral point clamped inverter.

principle can be described as follows:

- T_1 and T_2 are closed: The phase output voltage results to $v_{\text{out}} = +\frac{V_{\text{DC}}}{2}$. Depending on the output current direction the current flows either through the power semiconductors T_1 and T_2 or their anti-parallel freewheeling diodes.
- T_3 and T_4 are closed: The phase output voltage now is $v_{\text{out}} = -\frac{V_{\text{DC}}}{2}$. Depending on the output current direction the current flows either through the semiconductors T_3 and T_4 or the freewheeling diodes of T_3 and T_4.
- T_2 and T_3 are closed: Depending on the output current direction the current flows either through the power semiconductors T_2 and the clamping diode D_1 or the power semiconductors T_3 and the clamping diode D_2. In any case the the output voltage results in $v_{\text{out}} = 0$ V.

The switching states of the three-level neutral point clamped inverter are summarized in Tab.2.1.

Table 2.1: Switching states of the three-level neutral point clamped inverter.

T_1	T_2	T_3	T_4	v_{out}
1	1	0	0	$\frac{V_{\text{DC}}}{2}$
0	1	1	0	0 V
0	0	1	1	$-\frac{V_{\text{DC}}}{2}$

A second approach for the realization of a three-level topology is the T-type inverter shown in Fig. 2.7. The three-level T-type leg is based on the conventional two-level topology, which is extended by two power semiconductors in series (bidirectional switch) which connect the leg output directly to the DC-link midpoint. For this topology also four power semiconductors are needed for one leg, but in contrast to NPC inverter the additional clamping diodes are not needed. However, T_1 and T_4 has to be chosen regarding the total DC-link voltage V_{DC}.

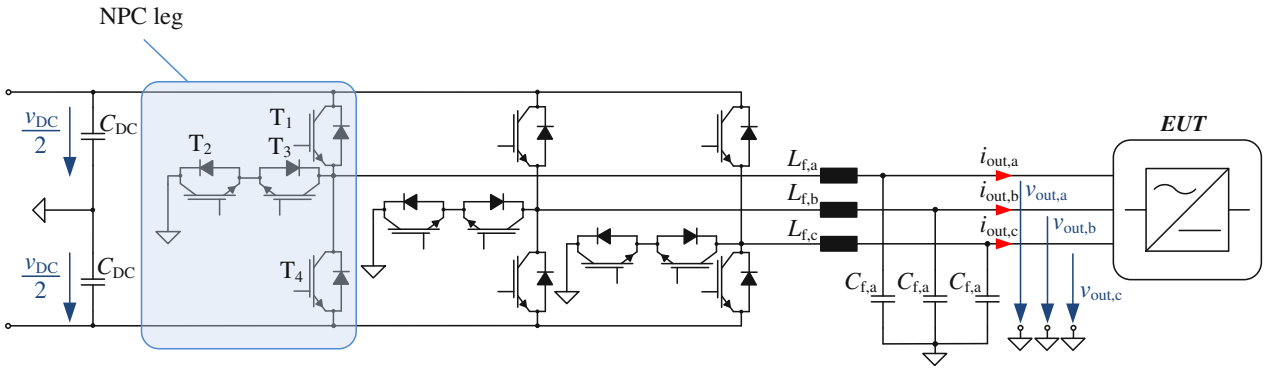


Figure 2.7: DC-link three-level T-type inverter.

In order to achieve a current-independent commutation sequence, the power semiconductors T_1 and T_2 has to be closed for the positive voltage level and T_3 and T_4 has to be closed for the negative voltage level, which enables a naturally current commutation [23]. The operation principle can be described as follows:

- T_1 is closed: The phase output voltage results in $v_{\text{out}} = +\frac{V_{\text{DC}}}{2}$. Depending on the output current direction the current flows either through the power semiconductor T_1 or the freewheeling diode of T_1.

- T_2 and T_3 are closed: The phase output voltage now is $v_{\text{out,3-level}} = 0$ V. Depending on the output current direction the current flows either through T_2 and the diode D_3 or T_3 and the diode D_2 .

- T_4 is closed: The output voltage $v_{\text{out,3-level}} = -\frac{V_{\text{DC}}}{2}$, depending on the output current direction the current flows either through the power semiconductor T_4 or the freewheeling diode of T_4.

Table 2.2: Switching states of the three-level T-type inverter.

T_1	T_2	T_3	T_4	v_{out}
1	1	0	0	$\frac{V_{\text{DC}}}{2}$
0	1	1	0	0 V
0	0	1	1	$-\frac{V_{\text{DC}}}{2}$

The switching states of the three-level T-type inverter are summarized in Tab.2.2. Beyond the switching states, the current commutation has to be analysed for the controller implementation but is not discussed in this work.

2.3 Grid Emulation Concepts

According to Sec.1.1 controllable AC power sources (AC-simulators) with adjustable grid characteristics (e.g. frequency, voltage, harmonics) are required [24] during development phase of (power) electronic components or standard compliance tests. With more sophisticated grid connected units like photovoltaic inverters, electric vehicles etc., not only the output voltage or output current is required as test parameters, additionally the output (grid) impedance emulation is needed which further affects the performance of the application. Fig. 2.8 shows a field trial test setup for grid connected components (EUT). Such a setup represents a realistic environment, but the variation of test parameters and thus of test cases is very limited. The voltage source v_g together with the resistive-inductive grid impedance are forming the equivalent circuit of the power grid. The impedance Z_{load} represents an additional load, which is connected to same low-voltage grid node as the EUT. In order to provide a sophisticated test environment for the validation of

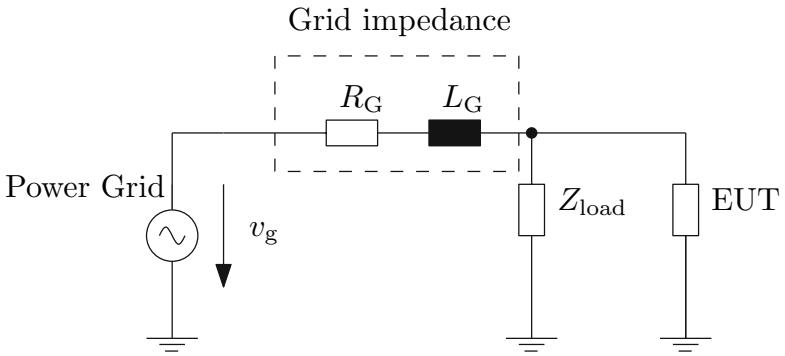


Figure 2.8: Field trial test setup for grid connected devices (EUT).

grid-connected converters, grid emulation concepts allow extensive testing of grid support functions, such as droop control, stabilizer for frequency and grid voltage, power factor correction (PFC), low voltage ride through (LVRT), virutal inertia (VI), primary frequency control as well as smart communication functions. Grid emulation based on a programmable AC-source and real discrete passive power impedance elements (R_G, L_G) is a common approach for the implementation of such an testing environment. The AIT SmarTEST laboratory, presented in Sec. 1.1.1, is based on such a concept depicted in Fig. 2.9. With a programmable

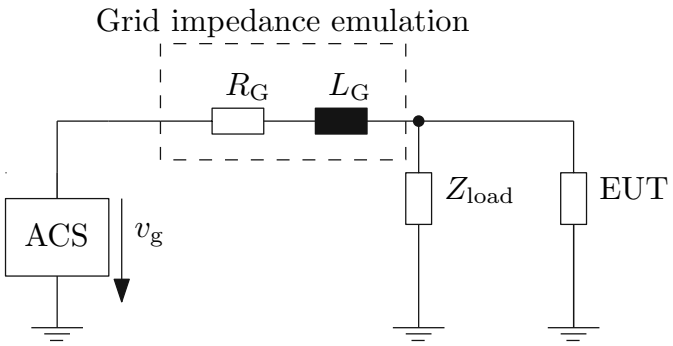


Figure 2.9: Grid emulation concept based on a programmable AC-source and real passive power impedance emulation.

AC-source used as AC-simulator the emulation of voltage dips, harmonic injection and frequency profiles/characteristics is supported by such devices. AC-simulators are widely used in industry and research laboratories. Different concepts for various applications have been developed so far. One example are single phase AC power sources for high quality signal generation [25, 26]. Furthermore, three-phase AC-simulators for grid connected converter testing [27–35] as well as induction machine emulation [36] have been developed. In either of these applications, the grid impedance is emulated by using real inductors and resistors in order to provide an equivalent grid situation. However, this approach requires bulky and expensive hardware, which leads to high costs and huge spatial effort. For this reason, the reconfiguration or extension of such a physical impedance network would be also difficult. Furthermore, an impedance emulation based on real hardware causes additional electrical losses resulting in

$$P = P_{\mathrm{ACS}} + P_{\mathrm{R}} + P_{\mathrm{L}} + P_{\mathrm{load}} + P_{\mathrm{EUT}} \tag{2.12}$$

compared to

$$P = P_{\mathrm{ACS}} + P_{\mathrm{load}} + P_{\mathrm{EUT}}. \tag{2.13}$$

On the other hand, such testing environments are robust and stable compared to other concepts.

In order to achieve higher flexibility in the use of different network topologies and configurations, a concept based on a real-time system (RTS) represents a promising approach. Fig. 2.10 shows the grid emulation concept based on a real-time system, also known as power hardware-in-the-loop (P-HIL) setup [37, 38]. The network topologies to be emulated is therefore modelled and simulated digitally in the RTS. The resulting output voltage signal is transmitted to a power amplifier, which is directly connected to the EUT. Current sensors are used within the power circuit and serve as a feedback signals for the RTS. It is also possible to generate an output current signal. In this specific case a voltage measurement for the feedback would be mandatory. Therefore different interface algorithms can be used, such as the ideal transformer method (ITM) or damping impedance method (DIM) [39]. The bandwidth of a P-HIL setup depends on the sample

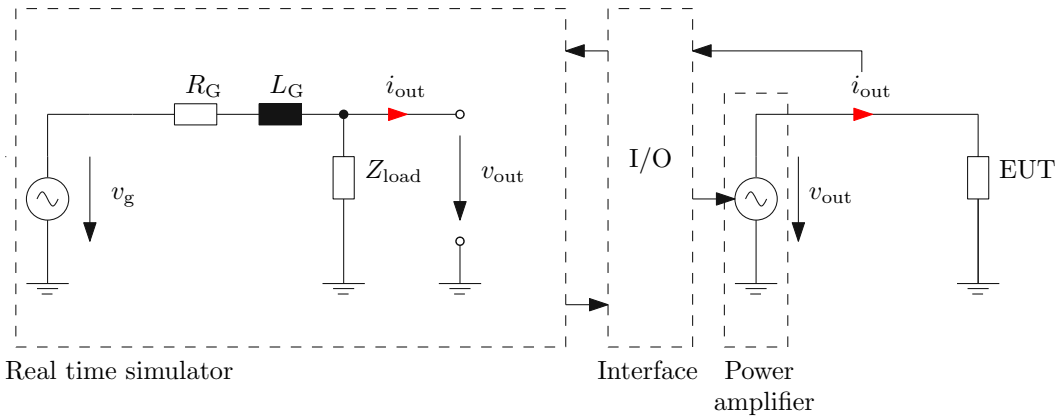


Figure 2.10: Grid emulation concept based on a real-time system and a power amplifier.

frequency of the RTS which is typically in the range of 200 ns – 2 μs as well as

the bandwidth of the power amplifier. Thus, the bandwidth of such HIL setups is typically lower than the bandwidth of a system which consists of real passive resistors and inductors. Also the robustness and stability of such system is lower, compared to other concepts, since the stability depends on the model of the emulated network. On the other hand such a concept enables the implementation of any network topology, without the need of bulky hardware, which also reduces investment costs. Furthermore no additional electrical losses are caused, since the emulated grid impedance is simulated on a RTS, which reduces operating cost. It can be concluded that a RTS based grid emulation concept offers high flexibility and comes with reduced capital expenses, but the stability of has to be analysed with every modification of the setup ([40–42]).

A different approach to reduce hardware costs and spatial effort can be achieved by using an advanced AC-simulator concept, also known as power function emulator. Such a system uses advanced control algorithms, in order to emulate also impedance networks in addition to the voltage source [43, 44]. In Fig. 2.11 the basic concept of such an advanced AC-simulator is depicted. The emulated network is implemented into the control algorithm of the total system. Therefore, the output characteristics are observed, used as feedback for the grid impedance emulation. As with the RTS based concept, additional output current measurements might required unless they are not implemented for the voltage controller. Also a proper interface algorithm (e.g. ITM, DIM etc.) has to be considered for the implementation of the network model. In principle, the advanced AC-simulator

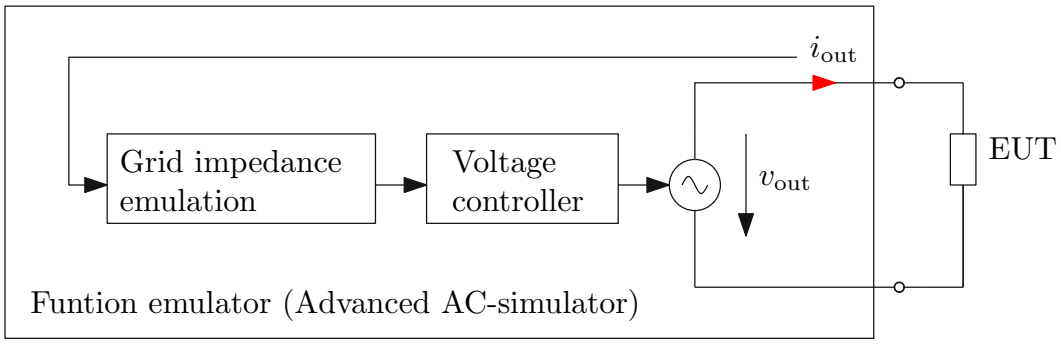


Figure 2.11: Grid emulation concept based on a advanced AC-simulator concept (power function emulator).

concept has strong affinity with the P-HIL concept. However, for this concept no additional RTS has to be used, therefore the investment costs can be even further reduced. Also in terms of bandwidth, such a concept can be beneficial, since it is a closed-loop system, which can optimized for each application. In terms of flexibility a minor disadvantage becomes apparent, due to the fact that the network model of the virtual impedance has to be implemented into the control algorithm. At the same time the stability of the advanced control algorithm must be ensured before implementation, which increases the robustness of the total system. The efficiency of such an advanced AC-simulator system is about equal to the conventional P-HIL setup since agian no losses of the virtual impedance will occur. Hence, the advanced AC-simulator concept (power function emulator) is the most promising approach for the AC-grid emulation and will be further investigated in this thesis.

Chapter 3

Advanced AC-Simulator Topologies

3.1 Single Stage

In this section a six-switch inverter topology for advanced AC-simulator (AACS) (cf., Fig. 3.1) is presented. Major benefits of this topology for AACS applications are robustness and relatively high efficiency. To reduce switching losses and allow blocking voltage capability up to 1.2 kV Silicon-Carbide (SiC) MOSFETs are applied.

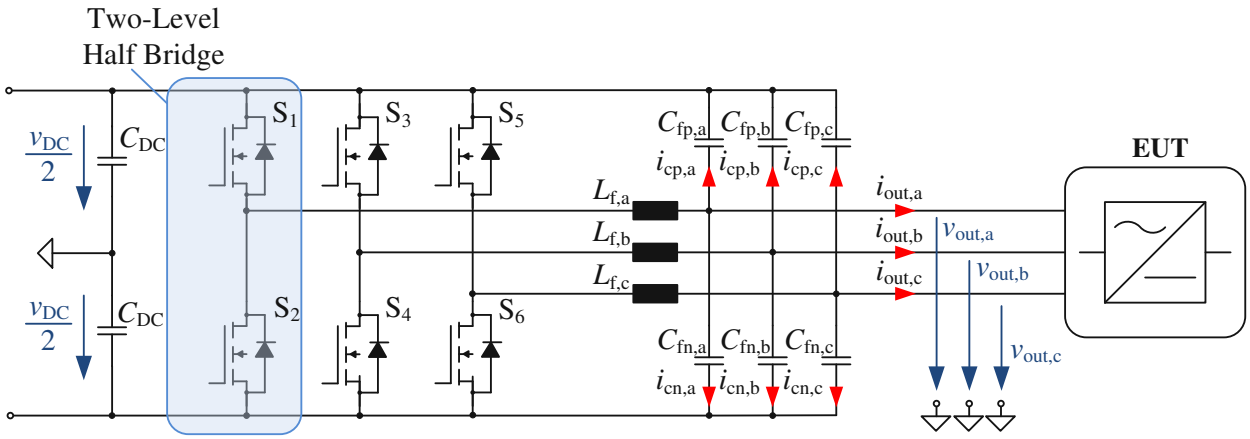


Figure 3.1: Single stage advanced AC-simulator (AACS)

The proposed topology is used for the emulation of low voltage power grid ($V_{LN} = 230\ V_{rms}/V_{LL} = 400\ V_{rms}$). Hence, a DC-link voltage set to $V_{DC} = 800$ V has been chosen, which results in a maximum modulation factor of $\delta_{max} = 0.8125$. In principle the topology of the single stage AACS is based on a two-level inverter according to Fig. 2.4, but the output filter is implemented as a decoupled output filter. The filter capacitors are directly connected to the DC-link capacitors, which enables independent control of each phase. In Table 3.1 the design specifications

of the AACS are summarized.

Table 3.1: Design specifications of the advanced AC-simulator

Parameter	Value
Phases:	3P
Operation mode:	4-Quadrant
Nominal output power:	$S_\mathrm{n} = 10$ kVA
Power Factor:	0 - 1
Nominal rms output voltage:	$V_\mathrm{out,LN} = 230$ V_rms
Nominal DC-link voltage:	$V_\mathrm{DC} = 800$ V
Max. DC-link voltage:	$V_\mathrm{DC,max} = 900$ V
Nominal frequency:	$f_\mathrm{n} = 50$ Hz
Small-signal bandwidth:	$f_\mathrm{bw} = 2$ kHz
Emulated resistance range:	$R_\mathrm{V} = 0\ \Omega - 1\ \Omega$
Emulated inductance range:	$L_\mathrm{V} = 0$ mH $- 5$ mH

In order to fulfil the requirements of the small-signal bandwidth of $f_\mathrm{bw} = 2$ kHz the output LC-filter has to be designed accordingly. Therefore, the LC-filter has to be designed in such a way that the output impedance has only a minor impact on the virtual impedance emulation. In Fig. 3.2 the effect of increasing inductor and capacitor values on the LC-filter output impedance is depicted. While an increased filter inductor value L_f can be compensated in the proposed virtual impedance control algorithm, an increased filter capacitor value C_f would require an additional compensation algorithm. Therefore the filter capacitor value is limited and has to be considered in the output filter design.

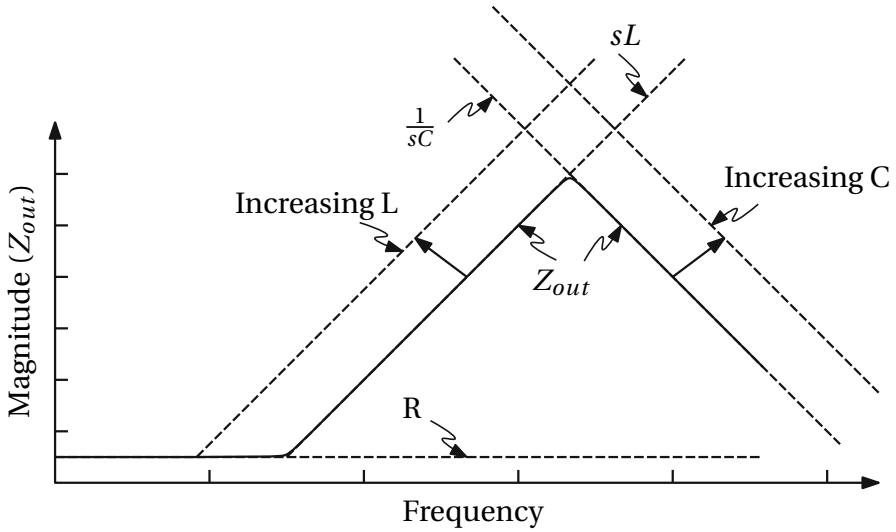


Figure 3.2: Bode plot of the effect of increasing inductor and capacitor values of the LC-filter output impedance.

3.1.1 Output Filter Design

A comparison of different filter designs, based on an analysis of the frequency response, is presented in this section. In a first step the switching frequency, the current ripple and the voltage ripple must be specified. Therefore, Fig. 3.3 shows the equivalent circuit of a DC-link two-level leg based on ideal switches.

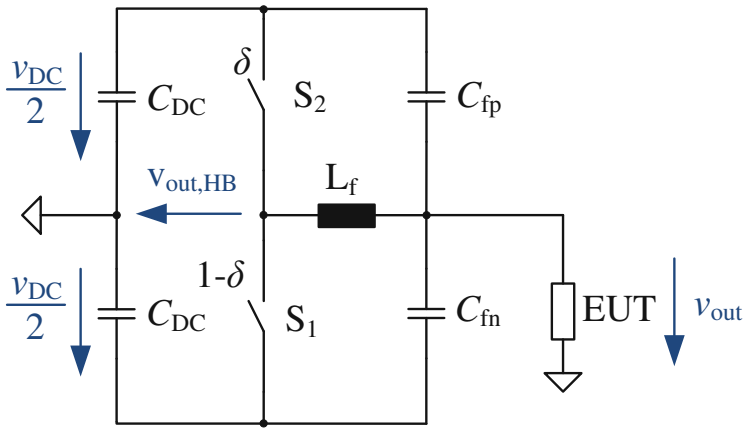


Figure 3.3: Equivalent circuit of a DC-link two-level leg based on ideal switches

Switching frequency

Switching frequencies for state of the art AC-simulators are in the range of 10 kHz− 50 kHz [1],[31], [45]. With respect of the requested small-signal bandwidth $f_{\mathrm{bw}} \leq$ 2 kHz and the resulting cut-off frequency of the LC-filter $f_{\mathrm{c,LC}} > 10 \cdot f_{\mathrm{bw}}$, the initial switching frequency value for the AACS is set to $f_{\mathrm{s}} = 10 \cdot f_{\mathrm{c,LC}} = 200$ kHz.

Current ripple

According to Eq. 2.10 the output voltage of a half bridge is given by

$$v_{out,HB}(t) = \begin{cases} +\frac{V_{\mathrm{DC}}}{2}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ -\frac{V_{\mathrm{DC}}}{2}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}} \end{cases} \tag{3.1}$$

which yields to the mean value of the output voltage of a half bridge of

$$\bar{v}_{\mathrm{out,HB}}(t) = \frac{1}{T_{\mathrm{s}}} \int_0^{\delta \cdot T_{\mathrm{s}}} \frac{V_{\mathrm{DC}}}{2} dt + \int_{\delta \cdot T_{\mathrm{s}}}^{T_{\mathrm{S}}} -\frac{V_{\mathrm{DC}}}{2} dt = V_{\mathrm{DC}} \left(\delta(t) - \frac{1}{2} \right). \tag{3.2}$$

Assuming closed-loop operation of the system the inductor voltage (according

to Fig. 3.3) is derived by

$$v_{\mathrm{L}}(t) = \begin{cases} +\frac{V_{\mathrm{DC}}}{2} - v_{out}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ -\frac{V_{\mathrm{DC}}}{2} - v_{out}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{3.3}$$

Thus, the filter inductor current of L_{f}, which is defined by

$$i_{\mathrm{L}}(t) = \int \frac{1}{L_{\mathrm{f}}} \cdot v_{\mathrm{L}}(t) dt \tag{3.4}$$

and computes to

$$i_{\mathrm{L}}(t) = \begin{cases} \frac{\Delta I_{\mathrm{L,pp}}}{\delta \cdot T_{\mathrm{s}}} t - \frac{\Delta I_{\mathrm{L,pp}}}{2} + I_{\mathrm{L}}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ \frac{-\Delta I_{\mathrm{L,pp}}}{(1-\delta) \cdot T_{\mathrm{s}}} t + \Delta I_{\mathrm{L,pp}} \cdot (\frac{\delta}{1-\delta} + \frac{1}{2}) + I_{\mathrm{L}}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}} \end{cases} \tag{3.5}$$

with the peak to peak current ripple $\Delta I_{\mathrm{L,pp}}$, which is defined by

$$\Delta I_{\mathrm{L,pp}} = \frac{V_{\mathrm{DC}} \cdot \delta \cdot (1-\delta)}{L_{\mathrm{f}} \cdot f_{\mathrm{s}}}. \tag{3.6}$$

Fig. 3.4 shows the qualitative current ripple characteristics of the output filter inductor L_{f}, which is derived in Eq.3.5.

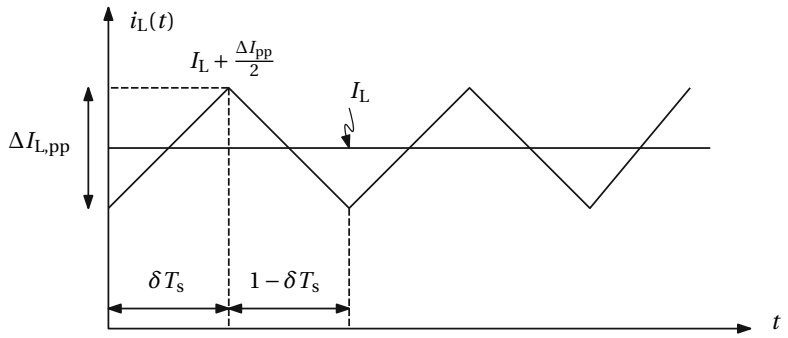


Figure 3.4: Qualitative current ripple characteristics of the output filter inductor L_f

The initial current ripple was set to 15 % of the peak output current $\hat{I}_{\mathrm{out,n}} = 20.5$ A which results in a peak to peak current ripple for $V_{\mathrm{DC,max}} = 900$ V of

$$\Delta I_{\mathrm{L,pp}} = 15\ \% \cdot \hat{I}_{\mathrm{out,n}} = 15\ \% \cdot 20.5\ \mathrm{A} = 2.77\ \mathrm{A} \tag{3.7}$$

According to 3.6 the output filter inductor value can be obtained by

$$L_{\mathrm{f}} \geq \frac{V_{\mathrm{DC,max}} \cdot T_{\mathrm{s}} \cdot \delta \cdot (1-\delta)}{\Delta I_{\mathrm{L,pp}}} \underset{\delta=0.5}{=} \frac{V_{\mathrm{DC,max}} \cdot T_{\mathrm{s}}}{4 \cdot \Delta I_{\mathrm{L,pp}}} \tag{3.8}$$

where the maximum value is reached with a duty cycle value of $\delta = 0.5$. This results in an the initial filter inductance value of $L_{\mathrm{f}} = 360\ \mu$H.

Voltage ripple

According to Kirchhoff's law the inductor current $i_{\mathrm{L}}(t)$ is defined by

$$i_{\mathrm{L}}(t) = \Delta i_{\mathrm{L}}(t) + I_{\mathrm{L}} = i_{\mathrm{C}}(t) + I_{\mathrm{L}} \tag{3.9}$$

and therefore the capacitor current $i_{\mathrm{C}}(t)$ is equal to the inductor ripple current $\Delta i_{\mathrm{L}}(t)$. Thus the output filter capacitor voltage $v_{\mathrm{C}}(t)$ can be derived by

$$v_{\mathrm{C}}(t) = \int \frac{1}{C_{\mathrm{f}}} \cdot i_{\mathrm{C}}(t) dt \tag{3.10}$$

and computes to

$$v_{\mathrm{C}}(t) = \begin{cases} \frac{8}{T_{\mathrm{s}}} \cdot \left(\frac{\Delta V_{\mathrm{c,pp}}}{2 \cdot \delta \cdot T_{\mathrm{s}}} t^2 - \frac{\Delta V_{\mathrm{c,pp}}}{2} t \right) + V_{\mathrm{C}}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ \frac{8}{T_{\mathrm{s}}} \cdot \left(\frac{-\Delta V_{\mathrm{c,pp}}}{2 \cdot (1-\delta) \cdot T_{\mathrm{s}}} t^2 - \frac{\Delta V_{\mathrm{c,pp}}}{2} t \left(1 + 2 \cdot \frac{\delta}{1-\delta}\right) - \frac{\Delta V_{\mathrm{c,pp}} \cdot \delta \cdot T_{\mathrm{s}}}{2} \cdot \left(1 + \frac{\delta}{1-\delta}\right) \right) + V_{\mathrm{C}}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{3.11}$$

The peak to peak voltage ripple $\Delta V_{\mathrm{c,pp}}$ at the output filter capacitor of a three-phase inverter with split DC-link capacitor is defined by

$$\Delta V_{\mathrm{c,pp}} = \frac{V_{\mathrm{DC,max}} \cdot \delta \cdot (1-\delta)}{8 \cdot L_{\mathrm{f}} \cdot C_{\mathrm{f}} \cdot f_{\mathrm{s}}^2}. \tag{3.12}$$

In order to meet the requirements of EN61000-3-3 and IEEE 1547, where a maximum THD of 2.5 % is required, the initial voltage ripple was set to 1.5 % of the nominal peak voltage $\hat{V}_{\mathrm{out,n}} = 325$ V. The initial filter capacitor value is therefore calculated to $C_f = C_{f,\frac{p}{n}} = 220$ nF.

Frequency response analysis of the LC-filter output impedance

In the following, the impact of the LC-filter output impedance on the emulation of a resistive-inductive grid impedance is analysed. The main goal is to achieve a small signal bandwidth up to $f_{\mathrm{s}} = 2$ kHz without significant deviations from the required RL-characteristic (maximum relative phase displacement less than 2° for the open-loop system). The output impedance of the LC-filter however directly affects and substantially reduces the maximum bandwidth. Therefore the frequency response of an ideal resistive-inductive impedance is used as a reference system and compared with the frequency response of an ideal VSC including resistive-inductive impedance emulation with additional LC-output filter. For simulating the small-signal response of the reference resistive-inductive model, a controlled current source injects the small-signal current perturbation. The output voltage then represents the small-signal output impedance. The equivalent circuit of the ideal resistive-inductive grid impedance model is depicted in Fig. 3.5.

The model of an ideal VSC including resistive-inductive impedance emulation with LC-output filter is shown in Fig. 3.6. The virtual impedance is based on a current measurement and a first order low-pass (PT1) element for the resistive

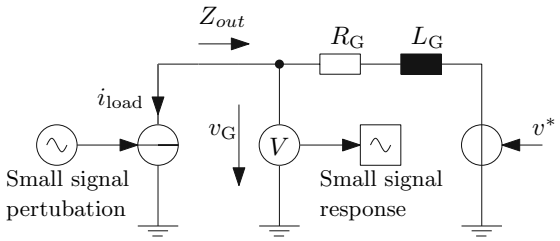


Figure 3.5: Reference circuit for the frequency response analysis of a RL impedance [6].

part

$$G_{R,V} = \frac{R_V}{1 + s \cdot T} \tag{3.13}$$

and a first order derivative element for the inductive part (DT1)

$$G_{L,V} = \frac{s \cdot L_V}{1 + s \cdot T} \tag{3.14}$$

of the emulated impedance. The low-pass filter with the corresponding time constant T, in order to omit amplification of high frequency noise especially for the derivative element (DT1). The idealized VSC is modeled as a controlled voltage source.

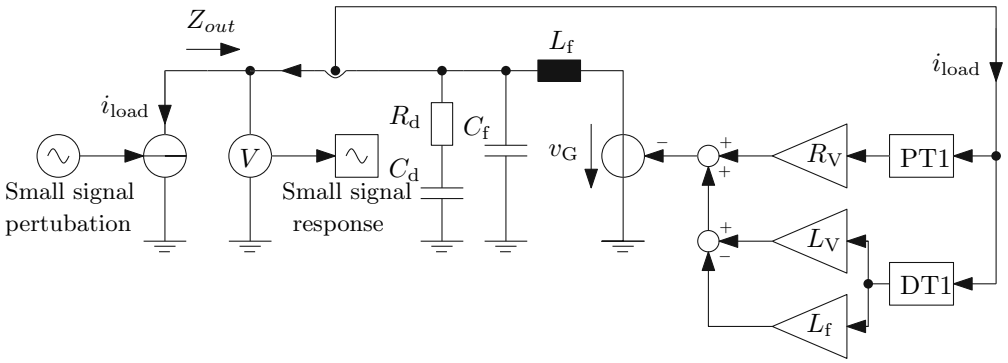


Figure 3.6: Schematic of a LC-output filter for the frequency response analysis with virtual RL impedance.

For the design process of the LC-filter, the small signal bandwidth of the LC-filter output impedance with virtual grid impedance is analysed in the following. A comparison with different filter capacitor values C_f is also presented. In order to retain the voltage ripple requirements Eq. 3.12 has to be considered, which shows a quadratic relationship between capacity and switching frequency. In a first attempt, a $L_f = 360\ \mu$H filter inductor and a $C_f = 220$ nF filter capacitor are used. For the grid impedance of the ideal model and the virtual impedance, impedance values according to IEC 60725 are used, which results in

$$R_G = R_V = 0,4\ \Omega \text{ and } L_G = L_V = 796\ \mu\text{H} \tag{3.15}$$

for a 50 Hz power grid. For frequencies below 2 kHz, the simulation results revealed that the magnitude plot of the LC-filter output impedance with virtual

grid impedance shows almost an identical characteristic compared to the reference system (see Fig. 3.7), as long as the value of C_f is equal or below 220 nF. However, the phase plot of the reference and the ideal VSC shows deviations for filter capacitor values $C_\mathrm{f} = 4,2\ \mu$F and $C_\mathrm{f} = 1\ \mu$F for frequencies higher than 900 Hz. Only the results for $C_\mathrm{f} = 220$ nF and $C_\mathrm{f} = 47$ nF revealed that the LC-filter shows no significant impact on the phase plot for frequencies up to 2 kHz. Due to the results of the initial selection of 3.7, the filter parameters of $C_\mathrm{f} = 220$ nF and $L_\mathrm{f} = 360\ \mu$H at the corresponding switching frequency of $f_\mathrm{s} = 200$ kHz can be confirmed. In Sec. 3.2.4 the design of the RC-snubber damping element is described, in order to minimize the occurring resonance. In Table 3.2 the specification of the LC-output filter are summarized.

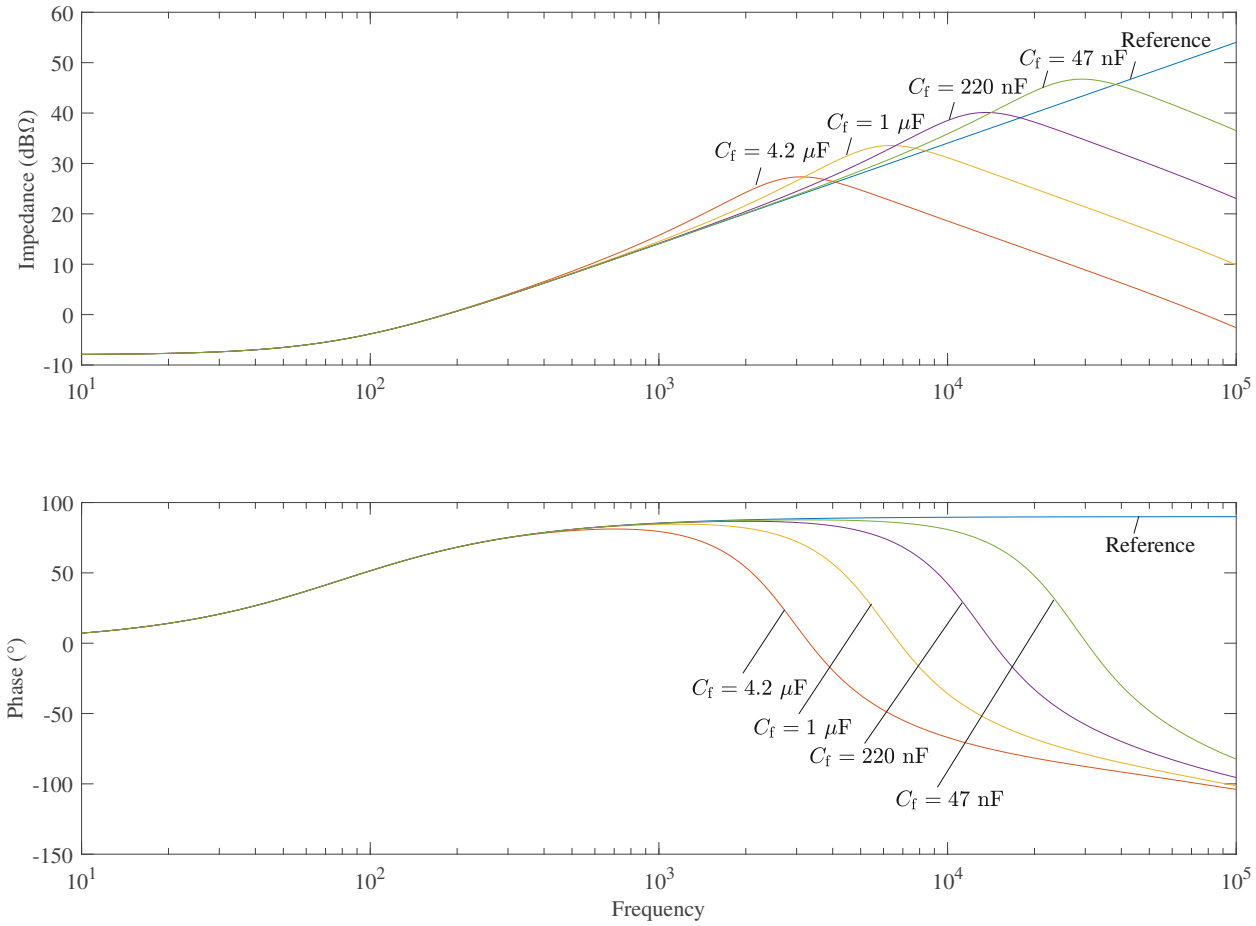


Figure 3.7: Bode diagram of the frequency response of the reference and the ideal VSC including resistive-inductive impedance emulation with additional LC-output filter.

Table 3.2: LC-output filter specification

Parameter	Value
Switching frequency:	$f_s = 200$ kHz
Filter capacitance:	$C_f = 220$ nF
Filter inductance:	$L_f = 360$ μH
Snubber resistor:	$R_D = 38$ Ω
Snubber capacitor:	$C_D = 660$ μnF
Time constant:	$T = 1$ μs

3.1.2 Impedance Based Stability Criterion

In order to investigate the stability of the AACS system with a corresponding EUT, equivalent circuits are used. Therefore the AACS system is modelled by its Thevenin equivalent circuit consisting of an ideal voltage source with resistive-inductive impedance Z_G, while the EUT (e.g. a grid-connected inverter) is modelled by its Norton equivalent consisting of an ideal current source in parallel with an output impedance Z_{EUT}. The overall system can be depicted by the equivalent circuit shown in Fig. 3.8.

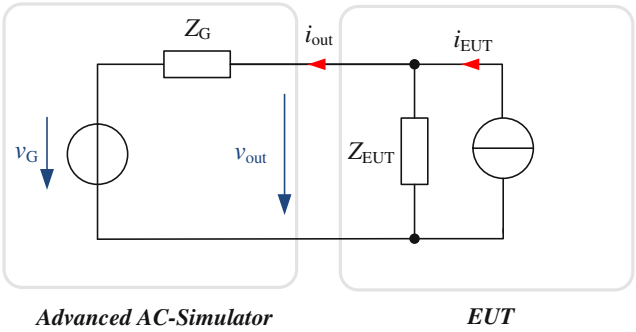


Figure 3.8: Equivalent circuit of a single phase advanced AC-simulator (AACS) with a grid connected inverter (EUT).

To assess whether the system is stable, the impedance based stability criterion is used [46, 47]. The criterion is based on the assumption that the current i_{out} between the AACS system and the DUT must be stable. Applying the superposition theorem, the current i_{out} is calculated by

$$\begin{aligned} I_{out,1}(s) &= I_{EUT}(s) \cdot \frac{Z_{EUT}}{Z_G + Z_{EUT}} \\ I_{out,2}(s) &= \frac{-V_G}{Z_G + Z_{EUT}} \\ \Longrightarrow I_{out}(s) = I_{out,1}(s) + I_{out,2}(s) &= \frac{1}{1 + \frac{Z_G}{Z_{EUT}}} \left[I_{EUT}(s) - \frac{V_G(s)}{Z_{EUT}} \right]. \end{aligned} \tag{3.16}$$

On the assumption that the output current I_{EUT} and the emulated grid voltage

V_G are stable (i.e. there are no unstable poles), the stability of $I_{out}(s)$ depends only on the first term

$$G = \frac{1}{1 + \frac{Z_G}{Z_{EUT}}} = \frac{1}{1 + G_O} \tag{3.17}$$

where $G_O = Z_G/Z_{EUT}$ represents the open loop transfer function, which can be assessed by applying the Nyquist stability criterion. The stability is determined by evaluating the number of encirclements of the critical $-1+j0$ point. In order to determine the power system stability, both the grid impedance Z_G and the EUT impedance Z_{EUT} must be specified for an AACS test setup. Since the emulated grid impedance is implemented as a resistive-inductive grid equivalent model, the grid impedance is given by

$$Z_G(s) = R_G + sL_G. \tag{3.18}$$

In [48] an analytical approximation of the impedance of an inverter is presented and thus the EUT impedance can be calculated by

$$Z_{EUT}(s) \approx \frac{1}{g_{eq} V_O G_{PI}} \left(sL_L + R_L + V_O G_{PI}\right). \tag{3.19}$$

Additional effects, such as the impact of the AACS LC-output filter on Z_G are neglected in this initial investigation. For the implementation of the EUT impedance model the following characteristics are defined in Tab. 3.3.

Table 3.3: Inverter parameters for the EUT impedance model.

Parameter	Value
Nominal power:	$P_N = 50$ kW
Output voltage:	$V_O = 800$ V_{DC}
Input voltage:	$V_{N,LL} = 400$ V_{rms}
PI-Controller:	$G_{PI} = k_p + \frac{1}{s}k_i$ with $k_p = 1.7e^{-4}$ and $k_i = 3.33e^{-1}$
Conductance:	$g_{eq} = \frac{P_N}{V_N^2} = 0.3125$ A/V
Output filter EUT:	$R_L = 10$ mΩ $L_L = 1200$ μH

Fig. 3.9 depicts the comparison of Nyquist diagrams of the transfer function $G_O = Z_G/Z_{EUT}$ with different grid inductor values based on a resistive-inductive equivalent impedance. Even for higher grid inductance values L_g the stability criterion is satisfied and no instability was detected by using a resistive-inductive grid impedance model. Furthermore, a comparison of Nyquist diagrams of the transfer function $G_O = Z_G/Z_{EUT}$ with different nominal power values P_N is shown in Fig. 3.10. Also for increased output power values P_N the stability criterion is satisfied and no unstable condition occurred. Even if the inverter is modelled with an LCL-output filter, no instability can be detected by emulating the grid with a resistive-inductive impedance. According to [49], an intersection of an extended grid impedance (e.g. cable model with additional capacitor) and inverter output impedance resonance frequency might result in unstable conditions. Since the AACS has only a resistive-inductive impedance implemented, this further in-

vestigations are not part of this work.

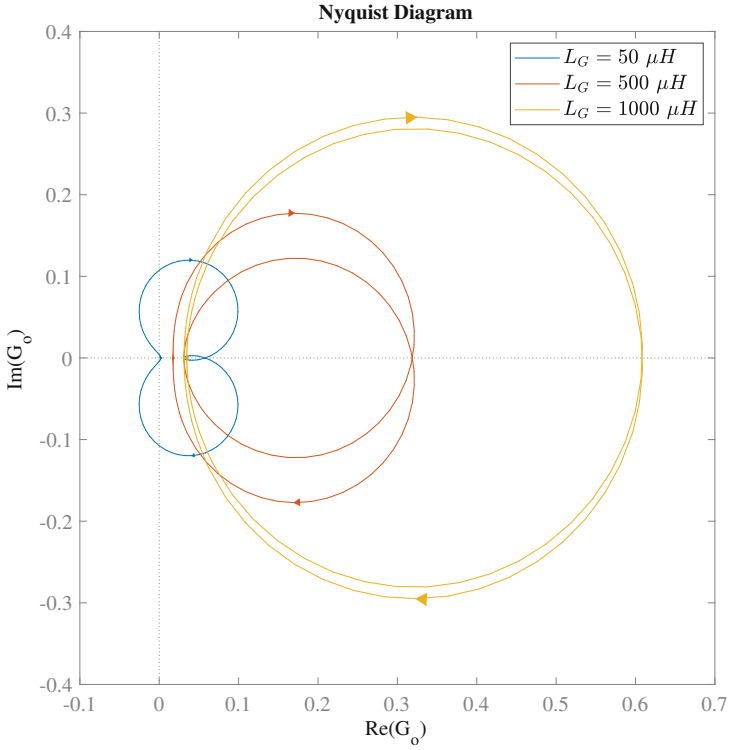


Figure 3.9: Comparison of Nyquist diagrams of the transfer function $G_{\mathrm{O}} = Z_{\mathrm{G}}/Z_{\mathrm{EUT}}$ with different grid inductor values L_{G} based on a resistive-inductive equivalent impedance.

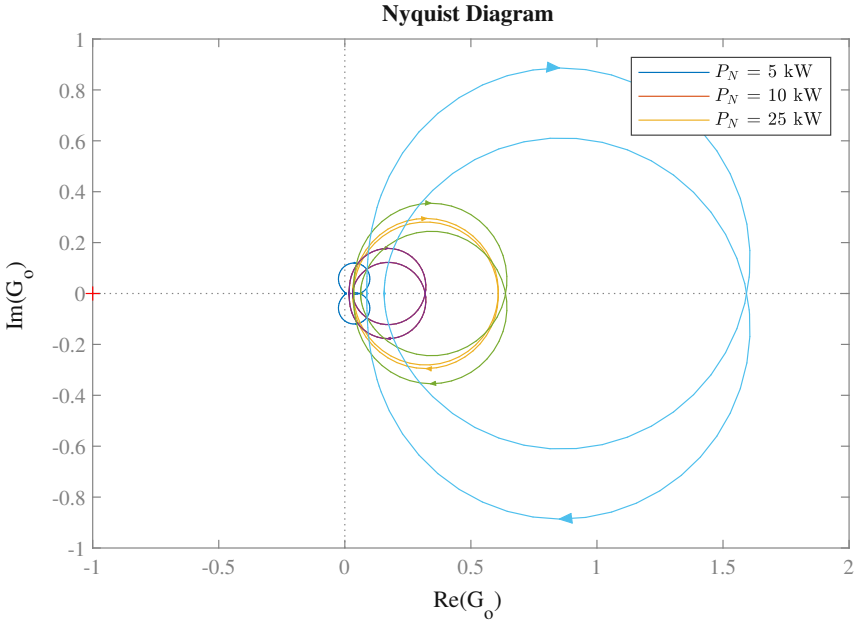


Figure 3.10: Comparison of Nyquist diagrams of the transfer function $G_{\mathrm{O}} = Z_{\mathrm{G}}/Z_{\mathrm{EUT}}$ with different output power P_{N} values based on a resistive-inductive equivalent impedance.

3.1.3 Fundamental Topology Issues

The proposed system is able to emulate resistive-inductive impedance values which are in the range of $0\ \Omega - 1\ \Omega$ and $0\ \text{mH} - 5\ \text{mH}$. For a three-phase application with a nominal voltage of $V_{\text{out,LN}} = 230\ \text{V}_{\text{rms}}$ (phase-neutral) and nominal power of $P_{\text{N}} = 10\ \text{kVA}$, the nominal current is given by

$$I_{\text{out}} = \frac{P_{\text{N}}}{3V_{\text{out,LN}}} = 14.49\ \text{A}_{\text{rms}}, \tag{3.20}$$

which results in rather small voltage drops of the virtual impedance compared to its fundamental value (for sinusoidal system operation). Even for the maximum impedance values of $R_{\text{V}} = 1\ \Omega$ and $L_{\text{V}} = 5\ \text{mH}$, the emulated peak voltage drop caused by virtual impedance, for sinusoidal fundamental voltage and a nominal frequency $f_{\text{n}} = 50\ \text{Hz}$ results in

$$\hat{V}_{\text{V}} = \sqrt{2} \cdot Z_{\text{V}} \cdot I_{\text{out}} = \sqrt{2 \cdot (R_{\text{V}}^2 + (\omega L)^2)} \cdot I_{\text{out}} = 38.17\ \text{V} \tag{3.21}$$

which is $\approx 10.3\ \%$ of the fundamental peak voltage.

If smaller values e.g. $R_{\text{V}} = 100\ \text{m}\Omega$ and $L_{\text{V}} = 500\ \mu\text{H}$ (10 % of the maximum impedance value) are emulated, the required peak voltage drop shrinks to 3.2 V which is around 1 % of the corresponding fundamental peak voltage. Therefore, the resolution of the voltage measurement circuits and analog signal conditioning has a major impact on the emulation of the small-signal voltage. To fulfill the accuracy, which is required for small signal waveform generation, low noise/high precision operational amplifiers and a high resolution anlog-to-digital converter (ADC) should be used. Assuming an accuracy of $\pm 1\ \%$ has to be achieved then the least-significant-bit (LSB) voltage can be approximated $V_{\text{LSB}} \approx 32\ \text{mV}$, which results in a required minimum ADC resolution of

$$N_{\text{min}} = log_2 \frac{\hat{V}_{\text{n}}}{V_{\text{LSB}}} = 14\ bit. \tag{3.22}$$

Furthermore, switching frequencies beyond $f_{\text{s}} \geq 200\ \text{kHz}$ are required to enable a LC filter design with a correspondingly high cut-off frequency of $f_{\text{c}} \approx 20\ \text{kHz}$. Such a filter design is mandatory, in order to guarantee an emulation bandwidth of at least 2 kHz to emulate distortions up to the 40^{th} harmonics of a 50 Hz grid. The high switching frequency as well as the DC-link voltage $V_{\text{DC}} = 800\ \text{V}$ result in high semiconductor switching losses, even if SiC power MOSFETs are employed.

3.2 Cascaded Advanced AC-Simulator

In order to remedy the disadvantages of the single stage AACS, a cascaded system was designed. For this purpose the AACS has been separated into two different inverter systems, one for the fundamental grid voltage (V_N = 230 V_{rms}/50 Hz) - the large-signal inverter and the second one for the virtual impedance emulation as well as harmonics injection - the small-signal inverter. Since the generation of the fundamental grid voltage requires no high bandwidth, a conventional grid emulator or even the mains grid can be used. Thus, the large signal inverter is designed for DC-link voltages of $V_{DC,LSI}$ = 800 V and switching frequencies in the range of $f_{s,ls}$ = 10 kHz − 50 kHz.

The second inverter has to inject harmonics and emulates the voltage drop of the virtual impedance, which results in output voltages of the small-signal inverter below $V_{out,SSI} \approx 10\ \%V_N$. Therefore, the small signal inverter can be operated at lower input DC voltage levels ($V_{DC,SSI}$ = 100 V) , which enables to implement fast switching devices with switching frequencies of $f_{s,SSI}$ = 200 kHz or higher. A further benefit of the reduced voltage levels is the smaller measurement range, which enables a higher measurement accuracy. Fig. 3.11 shows the principle of the cascaded advanced AC-Simulator (CAACS). In order to avoid additional DC-supplies,

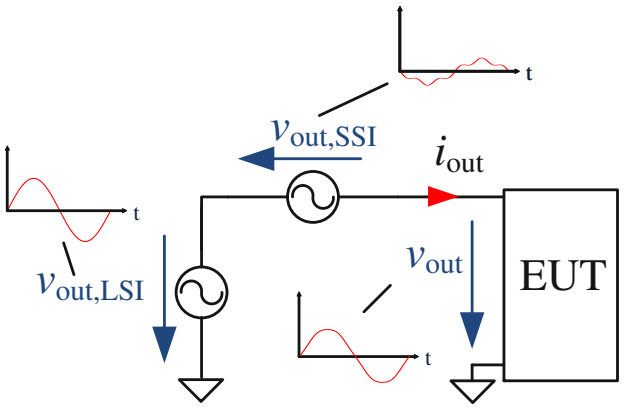


Figure 3.11: Principle of the cascaded advanced AC-Simulator (CAACS), consisting of a large-signal inverter and a small-signal inverter.

both inverters should be supplied from the same DC-source. A DC/DC converter therefore is used to reduce the DC-link voltage for the small-signal inverter accordingly. However, since the inverters are connected in series on the AC-side, a galvanic isolation is mandatory. The galvanic isolation can be realized by a transformer at the output of the large-signal inverter. Therefore a galvanic isolation of the DC/DC converters is not needed, which enables a design of a relatively simple bidirectional DC/DC converter. The transformer (e.g. YY0-transformer) is connected to the output of the large-signal inverter, in such a way that the bandwidth of the small-signal inverter is not affected and can be connected directly to the EUT.

However, it must be considered that the current implementation of the small signal inverter is not inherently able to compensate the output impedance of the large signal inverter and the parasitic impedance of the transformer. Therefore,

an embedded algorithm in the controller of the cascaded system would be needed, in order to compensate any parasitic components despite the emulated virtual impedance.

Fig. 3.12 shows the topology of the CAACS with a YY0 coupling transformer on the AC-side. A multiphase buck (MPB) converter is used as bidirectional DC/DC converter in order to step down the DC-link voltage of the large signal inverter to supply the DC-link of the small signal inverter.

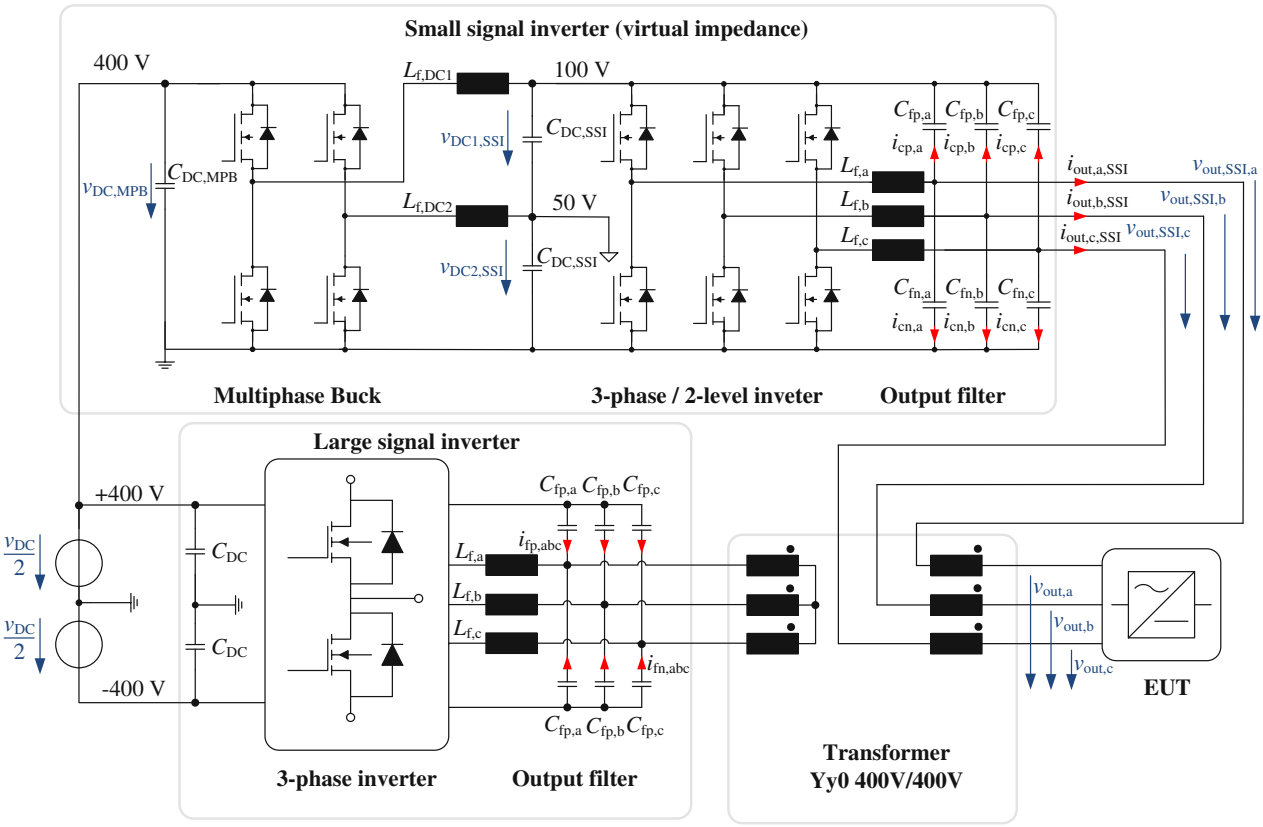


Figure 3.12: CAACS with a YY0 coupling transformer on the AC-side. A bidirectional DC/DC converter is used to supply the DC-link of the small signal inverter.

Since a conventional grid emulator can be used as large signal inverter, the further design process is focused on the small signal inverter and the MPB converter. In order to meet the nominal power specification of $S_N = 10$ kVA of the advanced AC simulator, the corresponding nominal current $I_{out,LSI} = I_{out,SSI} = 14.5$ A_{eff} is used for the design of the small-signal inverter.

According to Eq.3.21 the maximum emulated peak voltage drop caused by virtual impedance calculates to $\hat{V}_V = 38.17$ V. The maximum peak output voltage for the small signal inverter design was set to $\hat{V}_{out,LN,max} = 40$ V.

In Tab. 3.4 the design specifications for the small signal inverter of the CAACS are summarized.

Table 3.4: Design specifications for the small signal inverter of the cascaded of the advanced AC-simulator with a bidirectional MPB converter as input-stage.

Parameter	Value
Phases:	3P
Operation mode:	4-Quadrant
Nominal output power:	$S_{\mathrm{n}} = 1230$ W
Power Factor:	0 - 1
Nominal rms output voltage:	$V_{\mathrm{out,LN}} = 25$ V_{rms}
Maximum peak output voltage:	$\hat{V}_{\mathrm{out,LN,max}} = 40$ V
Nominal DC-link voltage MPB:	$V_{\mathrm{DC,MPB}} = 400$ V
Nominal DC-link voltage:	$V_{\mathrm{DC,SSI}} = 100$ V
Max. DC-link voltage:	$V_{\mathrm{DC,SSI,max}} = 150$ V
Switching frequency:	$f_{\mathrm{s,SSI}} = 200$ kHz
Small-signal bandwidth:	$f_{\mathrm{bw}} = 2$ kHz
Emulated resistance range:	$R_{\mathrm{V}} = 0\ \Omega - 1\ \Omega$
Emulated inductance range:	$L_{\mathrm{V}} = 0$ mH $- 5$ mH

3.2.1 Output filter Design - Inverter

Current ripple

Taking into account that the current ripple of the advanced AC-simulator finally results in $\Delta I_{\mathrm{L,pp}} = 15$ % and in order not to bring further disturbances into the CAACS system the current ripple of the small signal inverter was set to 5 % of the peak output current $\hat{I}_{\mathrm{out,n}} = 20.5$ A. Thus, the peak to peak current ripple for $V_{\mathrm{DC,SSI,max}} = 150$ V results in

$$\Delta I_{\mathrm{L,pp,SSI}} = 5\ \% \cdot \hat{I}_{\mathrm{out,n}} = 5\ \% \cdot 20.5\ \mathrm{A} = 1.025\ \mathrm{A}. \tag{3.23}$$

According to Eq. 3.6 the output filter inductor value can be obtained by

$$L_{\mathrm{f,SSI}} \geq \frac{V_{\mathrm{DC,SSI,max}} \cdot T_{\mathrm{s}} \cdot \delta \cdot (1-\delta)}{\Delta I_{\mathrm{L,pp,SSI}}} \underset{\delta=0.5}{=} \frac{V_{\mathrm{DC,SSI}} \cdot T_{\mathrm{s}}}{4 \cdot \Delta I_{\mathrm{L,pp,SSI}}} \tag{3.24}$$

where the maximum value is reached with a duty cycle value of $\delta = 0.5$ and from this follows the initial filter inductance value of $L_{\mathrm{f,SSI}} = 180$ μH.

Voltage ripple

In order to meet the requirements the same value are used for the design of the filter capacitors as for the advanced AC-simulator design, which results according to Eq.3.12 in a peak to peak voltage ripple for $C_{\mathrm{f,SSI}} = 220$ nF

$$\Delta V_{\mathrm{c,pp,SSI}} = \frac{V_{\mathrm{DC,SSI,max}} \cdot \delta \cdot (1-\delta)(T_{\mathrm{s}})^2}{8 \cdot L_{\mathrm{f,SSI}} \cdot C_{\mathrm{f,SSI}}} = 0.986\ \mathrm{V}. \tag{3.25}$$

3.2.2 Output Stage - Inverter

The further design of the two-level inverter output stage is based on the LC filter values summarized in Tab. 3.5.

Table 3.5: LC output filter specification of the CAACS.

Parameter	Value
Switching frequency:	$f_{\mathrm{s,SSI}} = 200$ kHz
Sample time:	$T_{\mathrm{s,SSI}} = 5$ μs
Filter capacitance:	$C_{\mathrm{f}} = 220$ nF
Filter inductance:	$L_{\mathrm{f}} = 180$ μH

Current Stress of Semiconductor

For the heat sink design of the two-level inverter output stage, the semiconductor stress has to be determined. Based on the mean and the RMS values of the power semiconductor currents the switching and conduction losses can be calculated. For further calculations, a sinusoidal output voltage, in phase with sinusoidal output current is assumed. This results in

$$\bar{v}_{\mathrm{out,HB}}(t) = \hat{V}\sin(\omega t). \tag{3.26}$$

Based on Eq.3.2 the duty cylce $\delta(t)$ obtained by

$$\delta(t) = \underbrace{\frac{\hat{V}}{V_{\mathrm{DC}}}}_{M/2}\sin(\omega t) + \frac{1}{2} = \frac{1 + M\sin(\omega t)}{2} \quad \text{for} \quad M \in [0\ldots 1]. \tag{3.27}$$

The expected sinusoidal output current, normally drawn by the EUT (e.g. while charging a battery storage system), of the output stage is given by

$$i_{\mathrm{out}}(t) = \hat{I}\sin(\omega t - \phi). \tag{3.28}$$

Since MOSFETs are bidirectional devices and the body diode conducts only during the dead time (interlock delay) of the PWM, the conduction losses of the diodes can be neglected. Furthermore, the angular frequency is replaced by $\omega t = \varphi$. The mean value of the high-side MOSFET current computes to (c.f. [50])

$$\bar{i}_{\mathrm{HS}} = \frac{1}{2\pi}\int_{\phi}^{\phi+2\pi} i_{\mathrm{out}}(\varphi)\cdot\delta(\varphi)d\varphi = \frac{\hat{I}\cdot M\cdot\cos(\phi)}{4}. \tag{3.29}$$

The corresponding RMS value of the high-side MOSFET current calculates to

$$I_{\mathrm{HS,rms}} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\phi+2\pi} i_{\mathrm{out}}^2(\varphi)\cdot\delta(\varphi)d\varphi} = \sqrt{\frac{\hat{I}^2}{4}} = \frac{\hat{I}}{2}. \tag{3.30}$$

Applying the same procedure for the low-side MOSFET (considering the complement of the duty cycle $(1-\delta)$), the mean value results in

$$\bar{i}_{\mathrm{LS}} = \frac{1}{2\pi}\int_{\phi}^{\phi+2\pi} i_{\mathrm{out}}(\varphi)\cdot(1-\delta(\varphi))d\varphi = \frac{\hat{I}\cdot M\cdot\cos(\phi)}{4}. \tag{3.31}$$

The corresponding RMS value of the low-side MOSFET current computes to

$$I_{\mathrm{LS,rms}} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\phi+2\pi} i_{\mathrm{out}}^2(\varphi)\cdot(1-\delta(\varphi))d\varphi} = \sqrt{\frac{\hat{I}^2}{4}} = \frac{\hat{I}}{2}. \tag{3.32}$$

In Tab.3.6 the parameters for the determination of the mean and the RMS current values are summarized.

Table 3.6: Parameters of the two-level inverter output stage operation point for the determination of the mean and the RMS current values

Parameter	Value
Nominal power:	$S_{\mathrm{N}} = 1230$ W
Maximum peak output voltage:	$\hat{V}_{\mathrm{out,LN,max}} = 40$ V
Maximum peak output current:	$\hat{I}_{\mathrm{out,n}} = 20.5$ A
Displacement angle	$\phi = 0°$

Conduction Losses

Based on the semiconductor stress and according to Eq.3.30 the conduction losses of the MOSFET can be determined by

$$P_{\mathrm{Cond,MOS}} = I_{\mathrm{ds,rms}}^2 \cdot R_{\mathrm{DS,on}} \tag{3.33}$$

and results for the IXSYS IXFP36N20X3 with a drain-source on-state resistance value of $R_{\mathrm{DS,on}} = 45\ m\Omega$ (25°) and RMS current value of $I_{\mathrm{HS,rms}} = I_{\mathrm{LS,rms}} = 10.25$ A in

$$P_{\mathrm{Cond,MOS}} = 4.728\ \mathrm{W}. \tag{3.34}$$

However, the body diode conduction losses can be determined by

$$\begin{aligned} P_{\mathrm{Cond,D}} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} t_{\mathrm{D}}\cdot f_{\mathrm{s}}(u_{\mathrm{f}}\cdot I_{\mathrm{ds,on}}(\varphi) + u_{\mathrm{f}}\cdot I_{\mathrm{ds,off}}(\varphi) + \ldots \\ \ldots R_{\mathrm{D}}\cdot I_{\mathrm{ds,on}}^2(\varphi) + R_{\mathrm{D}}\cdot I_{\mathrm{ds,off}}^2(\varphi))d\varphi. \end{aligned} \tag{3.35}$$

which results for a dead time value of $t_{\mathrm{D}} = 200$ ns, the diode forward voltage $u_{\mathrm{f}} = 0.85$ V and an approximated diode resistance of $R_{\mathrm{D}} = 45$ mΩ in

$$P_{\mathrm{Cond,D}} = 0.378\ \mathrm{W}. \tag{3.36}$$

Switching Losses

Since the switching frequency $f_{s,SSI}$ of the output stage is relatively high, the switching losses will represent an important part of the total losses. The determination of the switching losses is based on the specification of the energy losses during turn-on transition (E_{on}) during turn-off transition (E_{off}). As there are no corresponding losses given in the specification of the power semiconductor, the energy losses must be approximated according to [51]. The energy losses during turn-on transition in the MOSFET can be calculated as the sum of the switch-on energy without taking the reverse recovery process into account and the switch-on energy caused by the reverse-recovery of the free-wheeling diode given by

$$\bar{E}_{on,MOS} = \frac{1}{2\pi}\int_{\phi}^{\phi+\pi} V_{DC,SSI}\,|I_{ds,on}(\varphi)|\,\frac{t_{ri}+t_{fu}}{2}d\varphi + Q_{rr}\cdot V_{DC,SSI}. \tag{3.37}$$

The energy losses during turn-off transition calculates to

$$\bar{E}_{off,MOS} = \frac{1}{2\pi}\int_{\phi}^{\phi+\pi} V_{DC,SSI}\,|I_{ds,off}(\varphi)|\,\frac{t_{ru}+t_{fi}}{2}d\varphi. \tag{3.38}$$

The sinusoidal MOSFET current during turn-on transition $I_{ds,on}$ can be calculated according to Eq. 3.41

$$I_{ds,on}(t) = \hat{I}\sin(\varphi-\phi) - \frac{V_{DC,SSI}\cdot T_s\cdot\delta(\varphi)\cdot(1-\delta(\varphi))}{L_f} \tag{3.39}$$

and the during turn-off transition $I_{D,off}$ according to Eq. 3.42

$$I_{ds,off}(t) = \hat{I}\sin(\varphi-\phi) + \frac{V_{DC,SSI}\cdot T_s\cdot\delta(\varphi)\cdot(1-\delta(\varphi))}{L_f}. \tag{3.40}$$

The sinusoidal MOSFET current during turn-on transition $I_{ds,on}$ can be approximated with an enveloped function

$$I_{ds,on}(\varphi) = i_{out}(\varphi) - \frac{\Delta I_{L,pp}(\varphi)}{2} = \hat{I}\sin(\varphi-\phi) - \frac{V_{DC}\cdot T_s\cdot\delta(\varphi)\cdot(1-\delta(\varphi))}{L_f}. \tag{3.41}$$

The same procedure can be applied for the approximation of the MOSFET current $I_{D,off}$ which results in

$$I_{ds,off}(\varphi) = i_{out}(\varphi) + \frac{\Delta I_{L,pp}(\varphi)}{2} = \hat{I}\sin(\varphi-\phi) + \frac{V_{DC}\cdot T_s\cdot\delta(\varphi)\cdot(1-\delta(\varphi))}{L_f}. \tag{3.42}$$

Furthermore, the current rise time t_{ri} and the current fall time t_{fi} of the power MOSFET current are given in the specification, whereas the voltage rise time t_{ru} and the voltage fall time t_{fu} of the power MOSFET voltage has to be calculated.

During turn-on transition the voltage fall-time can be calculated as average value of the fall times defined through, the drain-source voltage, the gate current and the capacitances C_{GD1} and C_{GD2}, where C_{GD1} represents the gate-drain capacitance for if the drain-source voltage is in the range of $\frac{V_{DC,SSI}}{2}\ldots V_{DC,SSI}$ and

C_{GD2} if the drain-source voltage is in the range of $0 \ldots \frac{V_{\mathrm{DC,SSI}}}{2}$. Thus, the voltage fall time is given by

$$\begin{aligned} t_{\mathrm{fu}} &= \frac{t_{\mathrm{fu,1}} + t_{\mathrm{fu,2}}}{2} \\ t_{\mathrm{fu,1}} &= \frac{1}{\pi} \int_{\phi}^{\phi+\pi} (V_{\mathrm{DC,SSI}} - R_{\mathrm{DS,on}} \cdot |I_{\mathrm{D,on}}(\varphi)|) \cdot R_{\mathrm{Gate}} \cdot \frac{C_{\mathrm{GD1}}}{V_{\mathrm{Driver}} - V_{\mathrm{Plateau}}} d\varphi \\ t_{\mathrm{fu,2}} &= \frac{1}{\pi} \int_{\phi}^{\phi+\pi} (V_{\mathrm{DC,SSI}} - R_{\mathrm{DS,on}} \cdot |I_{\mathrm{D,on}}(\varphi)|) \cdot R_{\mathrm{Gate}} \cdot \frac{C_{\mathrm{GD2}}}{V_{\mathrm{Driver}} - V_{\mathrm{Plateau}}} d\varphi \end{aligned} \tag{3.43}$$

for dedicated values $R_{\mathrm{Gate}} = 5\ \Omega$, $C_{\mathrm{GD1}} = 3$ pF, $C_{\mathrm{GD2}} = 400$ pF, $V_{\mathrm{Driver}} = 12$ V $V_{\mathrm{Plateau}} = 6.7$ V. The voltage rise-time during turn-off can be derived by applying the same procedure and results in

$$\begin{aligned} t_{\mathrm{ru}} &= \frac{t_{\mathrm{ru,1}} + t_{\mathrm{ru,2}}}{2} \\ t_{\mathrm{ru,1}} &= \frac{1}{\pi} \int_{\phi}^{\phi+\pi} (V_{\mathrm{DC,SSI}} - R_{\mathrm{DS,on}} \cdot |I_{\mathrm{D,on}}(\varphi)|) \cdot R_{\mathrm{Gate}} \cdot \frac{C_{\mathrm{GD1}}}{V_{\mathrm{Driver}}} d\varphi \\ t_{\mathrm{ru,2}} &= \frac{1}{\pi} \int_{\phi}^{\phi+\pi} (V_{\mathrm{DC,SSI}} - R_{\mathrm{DS,on}} \cdot |I_{\mathrm{D,on}}(\varphi)|) \cdot R_{\mathrm{Gate}} \cdot \frac{C_{\mathrm{GD2}}}{V_{\mathrm{Driver}}} d\varphi. \end{aligned} \tag{3.44}$$

According to Eq. 3.37 the average energy losses during turn-on transition results in

$$\bar{E}_{\mathrm{on,MOS}} = 37.71\ \mu\mathrm{J} \tag{3.45}$$

and the average energy losses during turn-off transition results in

$$\bar{E}_{\mathrm{off,MOS}} = 11.61\ \mu\mathrm{J} \tag{3.46}$$

according to 3.38.

Therefore the total switching losses of the MOSFET for a switching frequency of $f_s = 200$ kHz resulting in

$$P_{\mathrm{sw,MOS}} = P_{\mathrm{on}} + P_{\mathrm{off}} = \bar{E}_{\mathrm{on}} \cdot f_{\mathrm{s}} + \bar{E}_{\mathrm{off}} \cdot f_{\mathrm{s}} = 9.864\ \mathrm{W}. \tag{3.47}$$

However, the switching energy of the diode can be calculated based on the total reverse recovered charge Q_{rr} and the DC-link voltage $V_{\mathrm{DC,SSI}}$ is given by

$$E_{\mathrm{sw,D}} = \frac{Q_{\mathrm{rr}} \cdot V_{\mathrm{DC,SSI}}}{4} \tag{3.48}$$

which results for $Q_{\mathrm{rr}} = 230$ nC, $f_{\mathrm{s}} = 200$ kHz and $V_{\mathrm{DC,SSI}} = 100$ V in

$$P_{\mathrm{sw,D}} = \frac{f_{\mathrm{s}} \cdot E_{\mathrm{sw,D}}}{2} = 0.575\ \mathrm{W}. \tag{3.49}$$

Total Semiconductor Losses and Efficiency

Based on the conduction losses, switching losses and the body diode losses the total losses can be calculated. Thus, the losses for either the high-side or the low side Power MOSFET results in

$$P_{\text{Total,Semi}} = P_{\text{Cond,MOS}} + P_{\text{Cond,D}} + P_{\text{sw,MOS}} + P_{\text{sw,D}} = 15.545 \text{ W} \tag{3.50}$$

and the total semiconductor losses of the system resulting in $P_{\text{Total}} = 93.27$ W.

Inductor Design and Loss Calculation

In Sec. 3.2.1 the required output filter inductance value of $L_{\text{f,SSI}} = 180$ μH is determined. For the output filter inductor, the Kool Mμ powder core toroid (0077615A7) with an inductance factor of $A_{\text{L}} = 82$ $\frac{nH}{T^2}$ is used. This allows to calculate the number of turns of the inductor by

$$N_{\text{L,f,SSI}} = \sqrt{\frac{L_{\text{f,SSI}}}{A_{\text{L}}}} = 47. \tag{3.51}$$

The inductor losses are comprised of copper losses and core losses. In order to calculate the copper losses the DC-resistance value and the AC-resistance value has to be considered. A solid enamelled copper wire ($d_{\text{W}} = 1.45$ mm, $d_{\text{iso}} = 10$ μm) has been chosen for the inductor. The DC-resistance of the coil calculates to

$$R_{\text{DC}} = N \frac{\rho_{\text{cu}} l_{\text{T}}}{d_{\text{W}}^2 \frac{\pi}{4}} = 52 \text{ m}\Omega \tag{3.52}$$

with the electrical resistivity of copper which is given by $\rho_{\text{cu}} = 0.02$ $\frac{\Omega \text{mm}^2}{\text{m}}$ and the length of a single turn $l_{\text{T}} = 91.3$ mm. However, for high-frequency applications the skin and the proximity effect have to be considered. The skin depth for a switching frequency of $f_{\text{s}} = 200$ kHz is given by

$$\delta_{\text{W}} = \sqrt{\frac{\rho_{\text{cu}}}{\pi \mu_0 f_{\text{s}}}} = 0.159 \text{ mm}. \tag{3.53}$$

According to [52] the high-frequency AC-resistance results in

$$R_{\text{AC}} = R_{\text{DC}} \cdot A_0 \left[\frac{\sinh(2A_0) + \sin(2A_0)}{\cosh(2A_0) - \cos(2A_0)} + \frac{2(N_{\text{l}} - 1)}{3} \frac{\sinh(2A_0) - \sin(2A_0)}{\cosh(2A_0) + \cos(2A_0)} \right] = 395 \text{ m}\Omega \tag{3.54}$$

where N_{l} represents the number of layers $N_{\text{l}} = 1$ and with the coefficient A_0 defined by

$$A_0 = \left(\frac{\pi}{4}^{\frac{3}{4}} \right) \frac{d_{\text{W}}}{\delta_{\text{W}}} \sqrt{\frac{d_{\text{W}}}{d_{\text{W}} + 2 d_{\text{iso}}}} = 7.601. \tag{3.55}$$

Thus, the copper losses results in

$$P_{\text{Copper}} = R_{\text{DC}} I_{\text{L,rms,SSI}}^2 + R_{\text{AC}} \left(\frac{\Delta I_{\text{L,pp,SSI}}}{2\sqrt{3}} \right)^2 = 10.956 \text{ W} \tag{3.56}$$

with the specified current $I_{\text{L,rms,SSI}} = 14.5 \text{ A}_{\text{rms}}$ and the current ripple $\Delta I_{\text{L,pp,SSI}} = 1.025$ A.

According to [53] the core losses calculate to $P_{\text{Core}} = 1.6$ W considering the high-frequency current ripple and the large-signal current. The total inductor losses therefore results in

$$P_{\text{Total,L}} = P_{\text{Copper}} + P_{\text{Core}} = 12.56 \text{ W}. \tag{3.57}$$

The total losses of the small-signal inverter are resulting in

$$P_{\text{Total,SSI}} = 3 \cdot P_{\text{Total,L}} + 6 \cdot P_{\text{Total,Semi}} = 130.95 \text{ W}, \tag{3.58}$$

which leads to an efficiency of $\eta = 89.4$ %.

3.2.3 Input Stage - Multiphase Buck

Since the DC-link voltage of the small-signal inverter must not exceed $V_{\mathrm{DC,SSI}} = 100$ V due to to resistive-inductive emulation requirements, a simple step-down converter can be used, if $V_{\mathrm{DC}} > V_{\mathrm{DC,SSI}}$. Due to the common split DC-link a multiphase buck has to be applied, which enables independent control of each partial DC-link voltage. In addition the input stage has to be designed as bidirectional converter, since the impedance emulation may be feeding power back from the inverter to the DC supply.

MPB Inductor Design

The design of the MPB inductor is based on its output current ripple. Therefore the inductor current $i_{\mathrm{Lf,dc1}}$ is calculated based on the corresponding inductor voltage $u_{\mathrm{Lf,dc1}}$. However, the output voltage of one half bridge of the MPB is given by

$$\bar{v}_{\mathrm{DC1,SSI}} = \delta \cdot V_{\mathrm{DC,MPB}} \tag{3.59}$$

Therefore the inductor voltage can be calculated by

$$v_{\mathrm{L}}(t) = \begin{cases} V_{\mathrm{DC,MPB}} - \bar{v}_{\mathrm{DC1,SSI}}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ -\bar{v}_{\mathrm{DC1,SSI}}, \delta \cdot T_{\mathrm{s}} \leq t < T_s. \end{cases} \tag{3.60}$$

According to Eq. 3.4 the filter inductor current of $L_{\mathrm{f,DC1}}$ can be derived by

$$i_{\mathrm{Lf,DC1}}(t) = \begin{cases} \frac{\Delta I_{\mathrm{Lf,DC1,pp}}}{\delta \cdot T_{\mathrm{s}}} t - \frac{\Delta I_{\mathrm{Lf,DC1,pp}}}{2} + I_{\mathrm{L}}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ \frac{-\Delta I_{\mathrm{Lf,DC1,pp}}}{(1-\delta) \cdot T_{\mathrm{s}}} t + \Delta I_{\mathrm{Lf,DC1,pp}} \cdot (\frac{\delta}{1-\delta} + \frac{1}{2}) + I_{\mathrm{L}}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{3.61}$$

with the peak to peak current ripple $\Delta I_{\mathrm{Lf,DC1,pp}}$, which is defined by

$$\Delta I_{\mathrm{Lf,DC1,pp}} = \frac{V_{\mathrm{DC,MPB}} \cdot \delta \cdot (1-\delta)}{f_{\mathrm{s}} \cdot L_{\mathrm{f,DC1}}}. \tag{3.62}$$

On the assumption that only a single half bridge has to supply the nominal power which results in a maximum output current $i_{\mathrm{Lf,DC1,max}} = 12.3$ A and a that the peak-to-peak current ripple should not exceed 15 % of the maximum output current, the current ripple results in

$$\Delta I_{\mathrm{Lf,DC1,pp}} = 15\ \% \cdot i_{\mathrm{Lf,DC1,max}} = 15\ \% \cdot 12.3\ \mathrm{A} = 1.845\ \mathrm{A} \tag{3.63}$$

Based on the specification of the maximum output current, the MPB filter inductor can be obtained according to Eq. 3.62 with $V_{\mathrm{DC,MPB}} = 400$ V

$$L_{\mathrm{f,DC1}} \geq \frac{V_{\mathrm{DC}} \cdot \delta \cdot (1-\delta)}{f_{\mathrm{s}} \cdot \Delta I_{\mathrm{Lf,DC1,pp}}} \underset{\delta=0.25}{=} \frac{V_{\mathrm{DC}} \cdot T_{\mathrm{s}} \cdot}{4 \cdot \Delta I_{\mathrm{Lf,DC1,pp}}} = 830\ \mu\mathrm{H}. \tag{3.64}$$

Current Stress of the Semiconductor

The current stress of MPB power MOSFETs are defined by

$$i_{\mathrm{MPB,HS}}(t) = \begin{cases} i_{\mathrm{Lf,DC1}}, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ 0, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{3.65}$$

and

$$i_{\mathrm{MPB,LS}}(t) = \begin{cases} 0, 0 \leq t < \delta \cdot T_{\mathrm{s}} \\ i_{\mathrm{Lf,DC1}}, \delta \cdot T_{\mathrm{s}} \leq t < T_{\mathrm{s}}. \end{cases} \tag{3.66}$$

Since the nominal voltage of the small signal DC-link is set to $V_{\mathrm{DC,SSI}} = 100$ V and the input voltage of the MPB is defined by $V_{\mathrm{DC}} = 400$ V, the duty cycle $\delta = 0.25$ is used for further considerations.

The mean values $\bar{i}$ and RMS values of the high-side as well as the low-side MOSFET are summarized in Tab. 3.7.

Table 3.7: Mean current values and RMS current values of MPB MOSFETs with duty cycle $\delta = 0.25$

	$\bar{i}_{\mathrm{MPB}}$	I_{MPB}
High-side	$\bar{i}_{\mathrm{MPB,HS}} = 3.1$ A	$I_{\mathrm{MPB,HS}} = 6.16$ $\mathrm{A_{RMS}}$
Low-side	$\bar{i}_{\mathrm{MPB,LS}} = 9.23$ A	$I_{\mathrm{MPB,LS}} = 10.66$ $\mathrm{A_{RMS}}$

Conduction losses

According to Eq. 3.33 the conduction losses of Rohm - SCT3080AL (SiC-MOSFET) with a drain-source on-state resistance $R_{\mathrm{DS,on}} = 80\ m\Omega$ and the corresponding RMS value for $I_{\mathrm{MPB,HS}}$ and $I_{\mathrm{MPB,LS}}$, results in

$$\begin{aligned} P_{\mathrm{Cond,MPB,HS}} &= I^2_{\mathrm{MPB,HS}} \cdot R_{\mathrm{DS,on}} = 3.03 \text{ W} \\ P_{\mathrm{Cond,MPB,LS}} &= I^2_{\mathrm{MPB,LS}} \cdot R_{\mathrm{DS,on}} = 9.09 \text{ W}. \end{aligned} \tag{3.67}$$

The body diode losses according to Eq. 3.35 are resulting in

$$P_{\mathrm{Cond,D}} = 0.319 \text{ W} \tag{3.68}$$

for a dead time value of $t_{\mathrm{D}} = 200$ ns, the diode forward voltage $u_{\mathrm{f}} = 3.2$ V and an approximated diode resistance of $R_{\mathrm{Diode}} = 375$ mΩ.

Switching losses

Since the small-signal inverter mainly operates as impedance emulator, the dissipated power from the output is feed back to the main DC-link. Therefore, the calculation of the MPB switching losses is based on the assumption, that the

output current $i_{\text{out,MPB}}$ is negative. Hence the switching losses occur mainly in the low-side MOSFET, because it operates as hard-switching device. Current dependent energy losses for turn-on $E_{\text{on}}(I_{\text{ds}})$ and turn-off $E_{\text{off}}(I_{\text{ds}})$ are specified in the datasheet of Rohms SCT3080AL. Based on this specifications a third-order function for the energy losses during turn-on transition $E_{\text{on}}(I_{\text{ds}})$ can be modeled as

$$E_{\text{on,MOS}}(I_{\text{ds}}) = k_{\text{on},3} \cdot I_{\text{ds}}^3 + k_{\text{on},2} \cdot I_{\text{ds}}^2 + k_{\text{on},1} \cdot I_{\text{ds}} + k_{\text{on},0} \tag{3.69}$$

and for the energy losses during turn-off transition $E_{\text{off}}(I_{\text{D}}))$ as

$$E_{\text{off,MOS}}(I_{\text{ds}}) = k_{\text{off},3} \cdot I_{\text{ds}}^3 + k_{\text{off},2} \cdot I_{\text{ds}}^2 + k_{\text{off},1} \cdot I_{\text{ds}} + k_{\text{off},0}. \tag{3.70}$$

In Tab. 3.8 the coefficients for the third-order function for the energy losses during turn-on transition $E_{\text{on}}(I_{\text{ds}})$ and for the energy losses during turn-off transition $E_{\text{off}}(I_{\text{D}}))$ are summarized.

Table 3.8: Coefficients for the third-order turn-off and and turn on switching transients energy loss function.

Index i	$k_{on,i}$	$k_{off,i}$
0	$1.318 \cdot 10^{-8}\ \frac{\text{J}}{\text{A}^3}$	$1.962 \cdot 10^{-9}\ \frac{\text{J}}{\text{A}^3}$
1	$-3.906 \cdot 10^{-7}\ \frac{\text{J}}{\text{A}^2}$	$-1.774 \cdot 10^{-8}\ \frac{\text{J}}{\text{A}^2}$
2	$7.483 \cdot 10^{-6}\ \frac{\text{J}}{\text{A}}$	$1.806 \cdot 10^{-6}\ \frac{\text{J}}{\text{A}}$
3	$1.175 \cdot 10^{-6}$ J	$2.83 \cdot 10^{-7}$ J

In addition, the drain source voltage V_{ds} and the gate resistance R_{g} must also be taken into account to obtain more accurate results. Therefore, two additional coefficients are introduced $k_{\text{ds}} = \frac{V_{\text{ds,applied}}}{V_{\text{ds,test}}}$ as well as $k_{\text{rg}} = \frac{R_{\text{g,application}}}{R_{\text{g,test}}}$.The high-side switching losses for any operating point are then given by

$$P_{\text{on,MOS}}(I_{\text{ds}}, V_{\text{ds}}, R_{\text{g}}) = k_{\text{ds}} \cdot k_{rg} \cdot f_{\text{s}} \cdot E_{\text{on,MOS}}(I_{ds}) \tag{3.71}$$

and

$$P_{\text{off,MOS}}(I_{\text{ds}}, V_{\text{ds}}, R_{\text{g}}) = k_{\text{ds}} \cdot k_{\text{rg}} \cdot f_{\text{s}} \cdot E_{\text{off,MOS}}(I_{\text{ds}}). \tag{3.72}$$

Therefore, the MOSFET current during turn-on and turn-off transition of the low-side MOSFET has to be calculated and results in

$$I_{\text{ds,on}} = I_{\text{ds}}(\frac{T_{\text{s}}}{4}) = -11.4 \text{ A} \tag{3.73}$$

$$I_{\text{ds,off}} = I_{\text{ds}}(T_{\text{s}}) = -13.2 \text{ A}. \tag{3.74}$$

Based on the derived MOSFET turn-on and turn-off current values the approximated energy losses lead to

$$E_{\text{on,MOS}}(I_{\text{ds,on}}) = 154.4\ \mu\text{J} \tag{3.75}$$

$$E_{\text{off,MOS}}(I_{\text{ds,off}}) = 31.16\ \mu\text{J}. \tag{3.76}$$

Repectively, based on the switching energy losses the total switching losses can be derived according to Eq. 3.71 and Eq. 3.72 for a switching frequency of $f_s = 50$ kHz by

$$P_{sw,MOS} = k_{ds} \cdot k_{rg} \cdot f_s \cdot (E_{on} + E_{off}) = 19.905 \text{ W} \tag{3.77}$$

However, applying Eq. 3.48 the diode switching losses with $Q_{rr} = 53$ nC, $f_s = 50$ kHz and $V_{DC,MPB} = 400$ V resulting in

$$P_{sw,D} = f_s \cdot E_{sw,D} = 0.066 \text{ W}. \tag{3.78}$$

Total losses

The total losses of a single MPB leg are calculated from the switching losses and the conduction losses of both the MOSFET and the body diode. Therefore the maximum total losses results in

$$P_{Total,Semi} = P_{Cond,MPB,HS} + P_{Cond,MPB,LS} + P_{Cond,D} + P_{sw,MOS} + P_{sw,D} = 32.455 \text{ W} \tag{3.79}$$

and the total losses of the system resulting in $P_{Total} = 64.91$ W.

Inductor Design and Loss Calculation

In Sec. 3.2.3 the required filter inductance value of $L_{f,DC1} = 830$ μH for the MPB is determined. As for the SSI output filter inductor, a Kool Mμ powder core toroid is used (0077735A7 with an inductance factor of $A_L = 88$ $\frac{nH}{T^2}$). Since a for the MPB inductor two powder cores are stacked, the number of turns is obtained by

$$N_{L,f,DC1} = \sqrt{\frac{L_{f,DC1}}{2 \cdot A_L}} = 69. \tag{3.80}$$

The DC-resistance of the coil calculates to

$$R_{DC} = N \frac{\rho_{cu} l_T}{d_W^2 \frac{\pi}{4}} = 142 \text{ m}\Omega \tag{3.81}$$

with the electrical resistivity of copper which is given by $\rho_{cu} = 0.02$ $\frac{\Omega mm^2}{m}$, the length of a single turn $l_T = 91.3$ mm and a solid enamelled copper wire ($d_W = 1.45$ mm, $d_{iso} = 10$ μm). Using Eq. 3.54 the high-frequency AC-resistance calculates to

$$R_{AC} = R_{DC} \cdot A_0 \left[\frac{\sinh(2A_0) + \sin(2A_0)}{\cosh(2A_0) - \cos(2A_0)} + \frac{2(N_l - 1)}{3} \frac{\sinh(2A_0) - \sin(2A_0)}{\cosh(2A_0) + \cos(2A_0)} \right] = 541 \text{ m}\Omega \tag{3.82}$$

with the skin depth $\delta_W = 0.318$ mm for a switching frequency of $f_s = 50$ kHz and $A_0 = 3.8$ according to Eq. 3.55. Thus, the copper losses results in

$$P_{Copper} = R_{DC} i_{Lf,DC1,max}^2 + R_{AC} \left(\frac{\Delta I_{Lf,DC1,pp}}{2\sqrt{3}} \right)^2 = 21.647 \text{ W} \tag{3.83}$$

with the specified current $i_{\mathrm{Lf,DC1,max}} = 12.3$ A and the current ripple $\Delta I_{\mathrm{Lf,DC1,pp}} = 1.845$ A. According to [53] the core losses calculate to $P_{\mathrm{Core}} = 1.304$ W considering the DC-current and the high-frequency current ripple. The total inductor losses therefore results in

$$P_{\mathrm{Total,L}} = P_{\mathrm{Copper}} + P_{\mathrm{Core}} = 22.951 \text{ W}. \tag{3.84}$$

The total losses of the MPB are resulting in

$$P_{\mathrm{Total,MPB}} = 2 \cdot P_{\mathrm{Total,L}} + 2 \cdot P_{\mathrm{Total,Semi}} = 110.81 \text{ W}, \tag{3.85}$$

which leads to an efficiency of $\eta = 91$ %.

3.2.4 Controller Design

MPB Controller Design

The MPB controller design of the CAACS is mainly separated into two parts,the MPB and the AACS voltage controller. This section is focussed on the MPB voltage controller. The MPB is used as bidirectional step-down converter to supply the DC-link of the small-signal inverter, with the DC-link voltage $V_{\mathrm{DC,MPB}}$ of the large signal inverter as input. Furthermore, the MPB has to balance the DC-link for the second stage in order to guarantee symmetrical supply. The output filter inductors $L_{\mathrm{f,DC1}} = L_{\mathrm{f,DC2}} = 833\ \mu\mathrm{H}$ of the MPB and the DC-link capacitors $C_{\mathrm{DC,SSI}} = 60\ \mu\mathrm{F}$ are forming a second order low-pass filter structure, which results in a resonance frequency of

$$f_{\mathrm{res,MPB}} = \frac{1}{2\pi\sqrt{L_{\mathrm{f,DC1}} C_{\mathrm{DC,SSI}}}} = 712\ \mathrm{Hz}. \tag{3.86}$$

This resonance frequency has to be damped accordingly for proper operation. An active damping method would require additional current sensors, which has to be connected in series with the small-signal DC-link capacitors. Since this is disadvantageous for a low impedance interconnection between the output stage and the small-signal inverter DC-link, a passive damping method is preferred. Furthermore a passive damping method would reduce computational effort of the digital controller which will be required for the high dynamic voltage controller of the small-signal inverter. One approach for the realization of the passive damping is the implementation of a RC-snubber, in parallel to the output DC-link capacitor $C_{\mathrm{DC,SSI}}$. Fig. 3.13 shows the control scheme of a single leg of the MPB input stage with a RC-snubber as passive damping method. The transfer function of a single

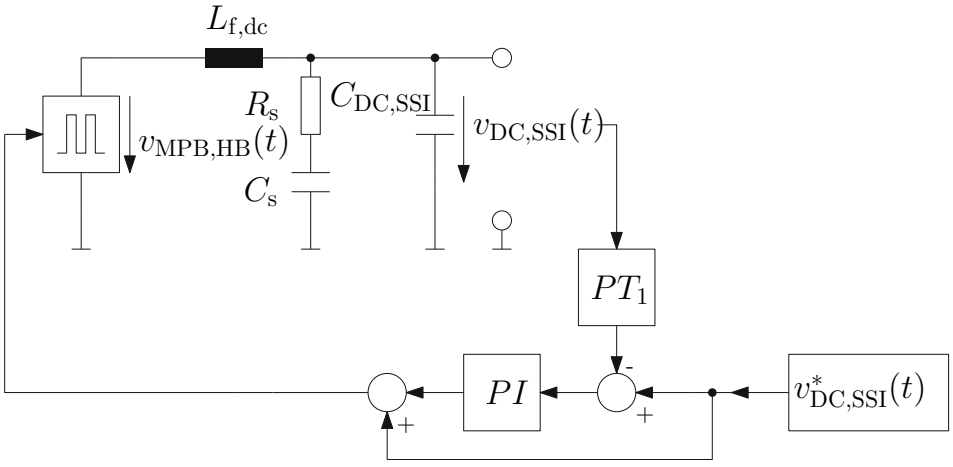


Figure 3.13: Control scheme of a single leg of the MPB input stage with passive damping [9].

leg of the MPB input stage including a RC-snubber and neglecting capacitor ESR

values and the ohmic part of the output filter inductors $L_{\mathrm{f,DC1}}$ is derived by

$$H_{\mathrm{MPB}}(s) = \frac{V_{\mathrm{DC,SSI}}(s)}{V_{\mathrm{MPB,HB}}(s)} = \frac{sR_{\mathrm{s}}C_{\mathrm{s}} + 1}{s^3 L_{\mathrm{f,DC1}} R_{\mathrm{s}} C_{\mathrm{DC,SSI}} C_{\mathrm{s}} + s^2 L_{\mathrm{f,DC1}}(C_{\mathrm{s}} + C_{\mathrm{DC,SSI}}) + sR_{\mathrm{s}}C_{\mathrm{s}} + 1}. \tag{3.87}$$

For the design of the snubber elements a comparison of coefficients is done between the MPB transfer function and a third order butterworth transfer function which is given by

$$H_{\mathrm{B}}(s) = \frac{1}{s_n^3 + 2s_n^2 + 2s_n + 1} \text{ with } s_n = \frac{s}{\omega_n}. \tag{3.88}$$

Equating the coefficients of the denominators the elements of the RC-snubber are derived by

$$R_{\mathrm{s}} = \sqrt{\frac{8L_{\mathrm{f,DC1}}}{9C_{\mathrm{DC,SSI}}}} = 3.51\ \Omega, \qquad C_{\mathrm{s}} = 3C_{\mathrm{DC,SSI}} = 180\ \mu\mathrm{F}. \tag{3.89}$$

The bode plots of the transfer function $H_{\mathrm{MPB}}(s)$ of the undamped and passive damped MPB LC low-pass filter structure are depicted in Fig. 3.14.

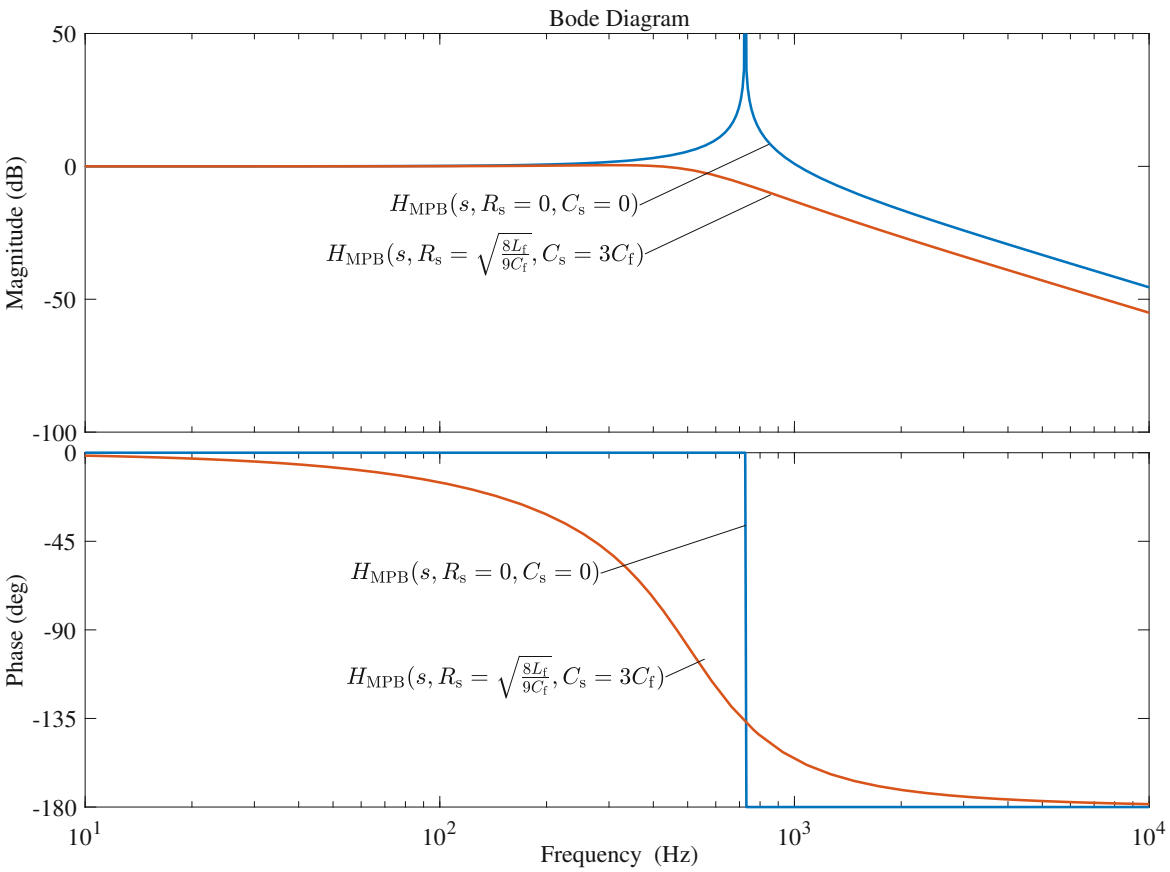


Figure 3.14: Bode plots of the input-to-output transfer function $H_{\mathrm{MPB}}(s)$ of the MPB LC low-pass filter structure. Comparison of undamped and passive damped ($R_{\mathrm{s}} = 3.51\ \Omega, C_{\mathrm{s}} = 180\ \mu\mathrm{F}$) transfer function.

For the calculation of the PI controller parameters, the Bode-plot design method is used [54]. The transient response of the closed-loop is now assessed based on the rise time t_r (dynamic behaviour), the percent overshoot $p_\mathrm{overshoot}$ of the the final value and the permanent control deviation e_∞ with the following parameters

$$t_\mathrm{r} = 600\ \mu\mathrm{s}, \qquad p_\mathrm{overshoot} = 10\ \%, \qquad e_\infty = 0. \tag{3.90}$$

Therefore the requirements of the open loop transfer function result in

$$\omega_\mathrm{c} = \frac{1.2}{t_\mathrm{r}} = 2000\ rad^{-1} \qquad \Delta\Phi = 70 - p_\mathrm{overshoot}. \tag{3.91}$$

A discrete frequency response of the input-to-output transfer function $H^{\#}_{filter}(q)$ has to be used for the digital controller design, to consider the digital sampling time T_S. Therefore, all transfer functions with their corresponding parameters are transferred with the inverse bilinear transform into the continuous q-domain given by

$$H^{\#}(q) = \frac{z-1}{z}\mathbf{Z}\left\{\frac{H(s)}{s}\right\}\Bigg|_{z=\frac{1+\frac{T_s}{2}q}{1-\frac{T_s}{2}q}}. \tag{3.92}$$

A PI-type controller with additional feed-forward signal is used for the output voltage controller, which is given by

$$R^{\#}_\mathrm{PI}(q) = k_\mathrm{p} + \frac{k_\mathrm{i}}{q} = k_\mathrm{c}(1 + \frac{1}{qT_\mathrm{N}}). \tag{3.93}$$

For the design of PI-type controller the open-loop transfer function $L_1(q)$ of the MPB including the integral term of the controller has to be calculated

$$L^{\#}_1(q) = \frac{H^{\#}_\mathrm{MPB}(q)}{q} \tag{3.94}$$

and evaluated at the crossover frequency

$$\arg(L_1(j\omega_\mathrm{c})) = -144.8°. \tag{3.95}$$

However, the phase margin of the open-loop system was specified with $\Delta\Phi = 60°$ and thus the phase margin has to be increased by $\Delta\Phi_\mathrm{PI} = 24.8°$. The time constant T_N results in

$$T_\mathrm{N} = \frac{\tan(\Delta\Phi_\mathrm{PI})}{\omega_\mathrm{c}} = 231\ \mu\mathrm{s}. \tag{3.96}$$

The gain of the integral term can be determined by

$$k_\mathrm{c} = \frac{T_\mathrm{N}}{\left|L^{\#}_1(q)(1+qT_\mathrm{N})\right|} = 0.3984. \tag{3.97}$$

The resulting controller parameters of the PI-type controller are summarized

in table 3.9.

Table 3.9: Controller parameters for the MPB of the CAACS with virtual impedance. The controller parameters are obtained by applying the the Bode-plot design method based on a passive damped LC filter structure.

Parameter	Value
Damping resistor	$R_S = 3.73\ \Omega$
Damping capacitor	$C_S = 180\ \mu\text{F}$
PI controller gain:	$k_c = 0.3984$
PI controller time constant:	$T_N = 231\ \mu s$

The frequency response of the closed-loop transfer function $T_{\text{r}}^{\#}(q)$ as well as the closed-loop transfer function with feed-forward $T_{\text{rf}}^{\#}(q)$ for the MPB of the CAACS without load is shown in Fig. 3.15. As can be seen, the Bode plot of the closed-loop transfer function with feed-forward $T_{\text{rf}}^{\#}(q)$ shows a reduced phase displacement but a slightly increased gain at the resonance frequency $f_{\text{res,MPB}}$.

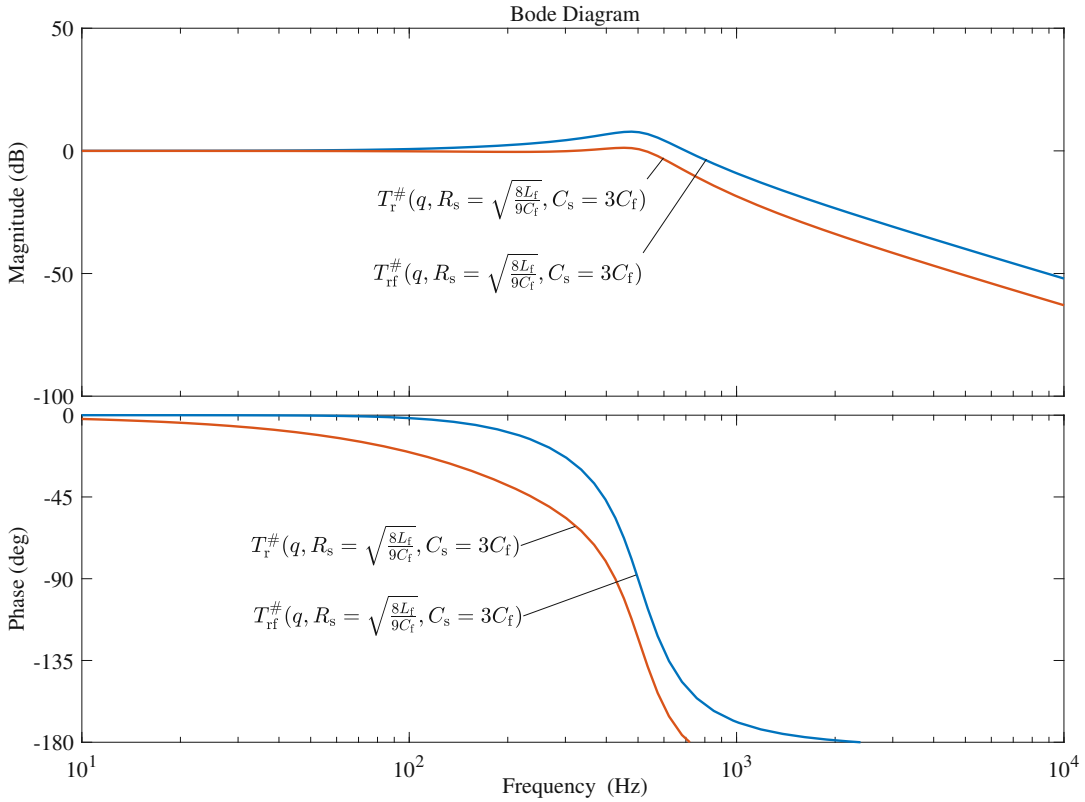


Figure 3.15: Bode plots of the closed-loop transfer function $T_{\text{r}}^{\#}(q)$ and closed-loop transfer function with feed-forward $T_{\text{rf}}^{\#}(q)$ of the MPB without load and corresponding controller PI-type controller parameters.

The designed controller $R_{\text{MPB,PI}}^{\#}(q)$ has to be transformed back into the z-domain to implement the digital controller on a DSP. Therefore the step response of

the closed-loop transfer function $T_r(z)$ and closed-loop transfer function with feed-forward $T_{\mathrm{rf}}(z)$ is shown in Fig. 3.16. As specified in the controller requirements in Eq.3.90 the maximum overshoot for the closed-loop transfer function $T_{\mathrm{r}}(z)$ doesn't exceed $p_{\mathrm{overshoot}} = 10\%$. However, the step response of the closed-loop transfer function with feed-forward $T_{rf}(z)$ shows a maximum overshoot of $p_{\mathrm{overshoot}} = 55\ \%$, which has to considered when the system is operated with load steps (e.g. non-linear loads).

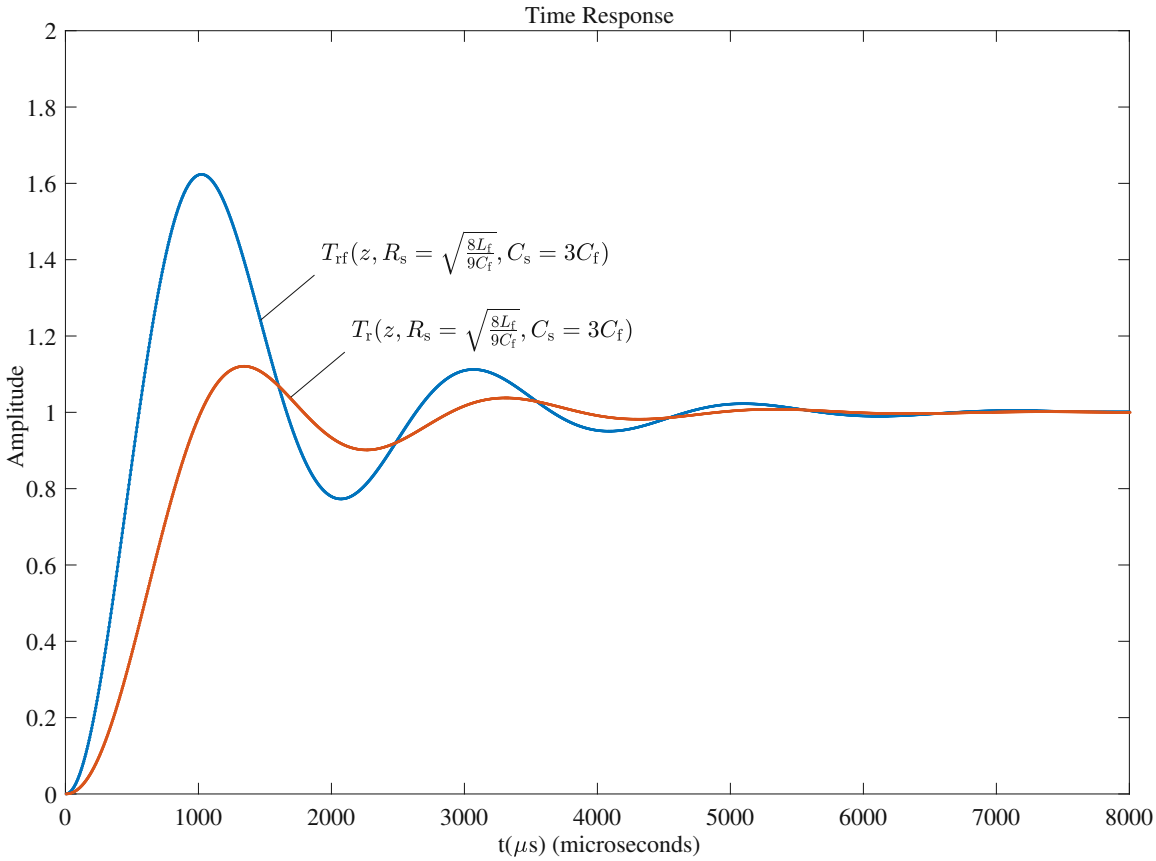


Figure 3.16: Step response of the closed-loop transfer function $T_{\mathrm{r}}(z)$ and closed-loop transfer function with feed-forward $T_{\mathrm{rf}}(z)$ of the MPB without load and corresponding controller PI-type controller parameters.

Fig. 3.17 shows the simulated MPB output voltage $v_{\mathrm{DC,SSI}}$ for a load step from 11.1 Ω to 8.3 Ω (resulting in a current step of 3 A).

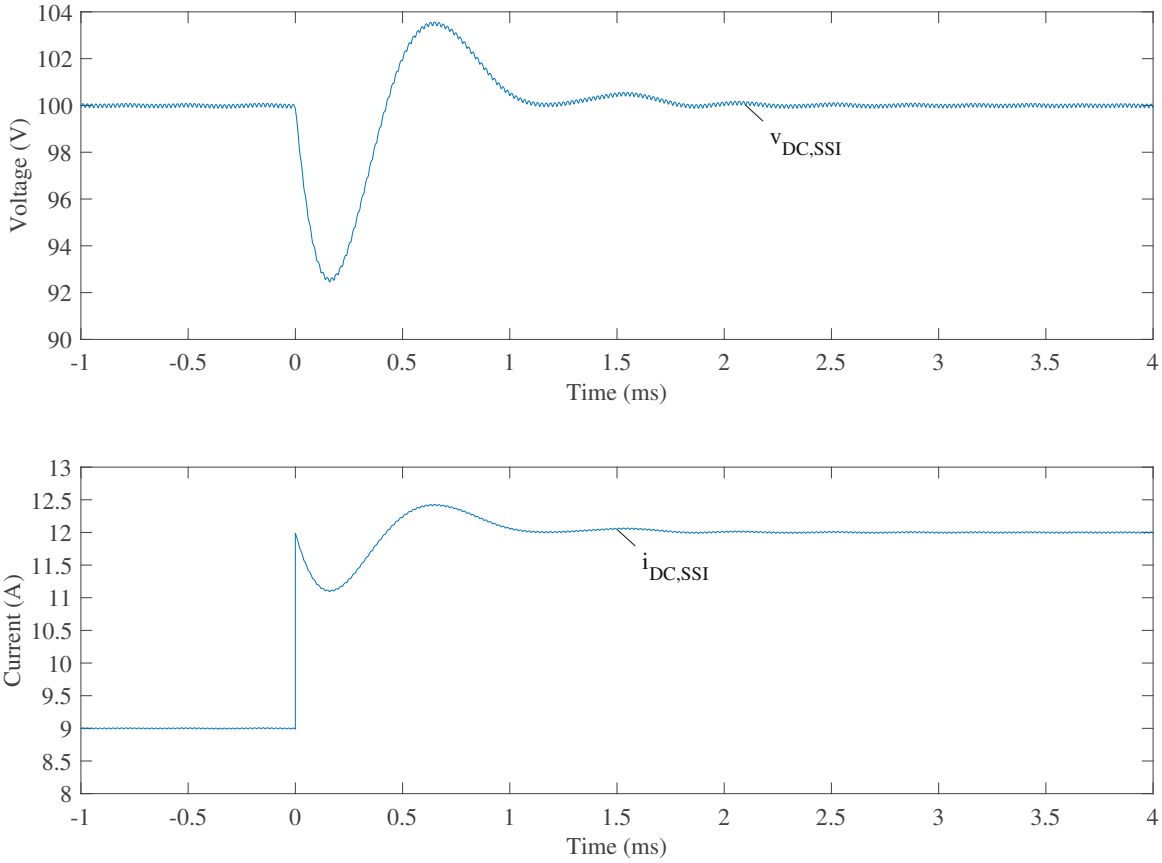


Figure 3.17: Simulated MPB output voltage $v_{\mathrm{DC,SSI}}$ for a load step from 11.1 Ω to 8.3 Ω.

Small-Signal Inverter Controller Design

For the controller design of the output stage the small-signal inverter has to be analysed. The small-signal inverter is mainly used for the injection of harmonics and the emulation of the virtual impedance. Therefore a fast sampling time ($T_{\mathrm{a}} = 5\ \mu$s) is needed to fulfil the requirements according to Tab. 3.4. For the attenuation of the critical resonance frequency of

$$f_{\mathrm{res,SSI}} = \frac{1}{2\pi\sqrt{L_{\mathrm{f}} \cdot C_{\mathrm{f}}}} = 25.3\ \mathrm{kHz}. \tag{3.98}$$

also a passive damping method has been chosen, with respect to the stability and the limited resources of the digital control system. The single-phase control scheme of the SSI with passive damped LC filter and virtual resistive-inductive impedance is shown in Fig. 3.18.

A parallel RL-passive damping was chosen as passive damping method and

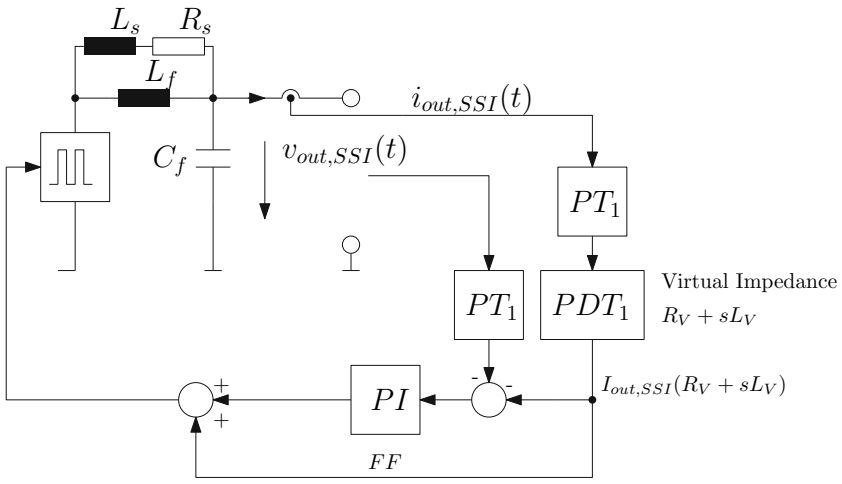


Figure 3.18: Single-phase control scheme of the SSI with passive damped LC filter and virtual resistive-inductive impedance [10].

therefore the calculation of the transfer function results in

$$H_{\mathrm{SSI}}(s) = \frac{V_{\mathrm{out,SSI}}(s)}{V_{\mathrm{SSI,HB}}(s)} = \frac{1 + s\frac{L_\mathrm{f}+L_\mathrm{S}}{R_\mathrm{S}}}{1 + s\frac{L_\mathrm{f}+L_\mathrm{S}}{R}_\mathrm{S} + s^2 L_\mathrm{f} C_\mathrm{f} + s^3 \frac{L_\mathrm{f}\cdot L_\mathrm{S}\cdot C_\mathrm{f}}{R_\mathrm{S}}}. \tag{3.99}$$

For the calculation of the damping components the same procedure as for the MPB design can by applied. The obtained transfer function $H_{\mathrm{SSI}}(s)$ is compared to an ideal third-order Butterworth characteristic, according to Eq. 3.88 and thus the values for the damping resistor R_S and inductor L_S results in

$$L_\mathrm{S} = \frac{L_\mathrm{f}}{3} = 60\ \mu\mathrm{H}, \qquad R_\mathrm{S} = \frac{8}{9}\sqrt{\frac{L_\mathrm{f}}{C_\mathrm{f}}} = 25\ \Omega. \tag{3.100}$$

A comparison of the undamped and parallel LR-passive damped Bode plots of the input-to-output transfer function H_{SSI} of the small signal inverter output filter is shown in Fig. 3.19.

The virtual resistor R_V in series with the virtual inductor L_V are forming the virtual grid impedance. This virtual impedance causes a voltage drop, which is dependent on the output current $i_\mathrm{out}(t)$ of the CAACS. The implementation of the virtual resistor can be realized with a simple multiplication of the value of the resistor R_V with the measured output current $i_\mathrm{out}(t)$. Since for the implementation of the virtual inductor the derivation of the output current $\frac{di_\mathrm{out}(t)}{dt}$ has to be used, the amplification of high frequency noise must be prevented, which can be achieved by implementing a corresponding filter (e.g. DT1 element). However, the DT1 control element transfer function in s-domain is given by

$$H_{\mathrm{DT1}}(s) = \frac{s}{1 + sT} \tag{3.101}$$

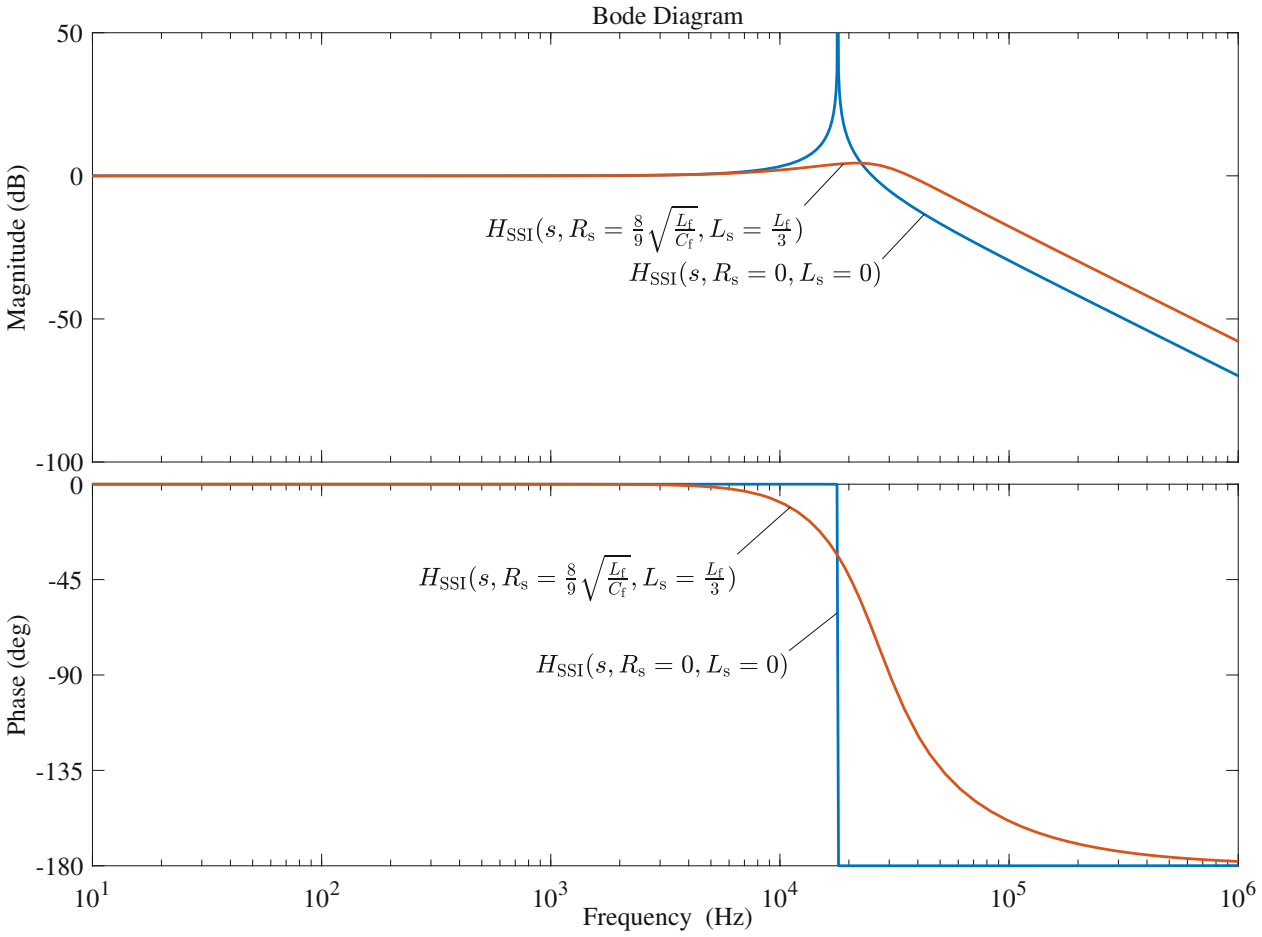


Figure 3.19: Bode plots of the input-to-output transfer function H_{SSI} of the small signal inverter output filter. Comparison of undamped and passive damped ($R_{\mathrm{s}} = 19\ \Omega, L_{\mathrm{s}} = 60\ \mu H$) transfer function.

and for the digital controller in z-domain is derived by

$$H_{\mathrm{DT1}}(z) = \frac{1 - z^{-1}}{\frac{1}{\omega_k} + (T_{\mathrm{s}} - \frac{1}{\omega_{\mathrm{k}}})z^{-1}}. \tag{3.102}$$

At the same time the virtual impedance enables the compensation of the coupling transformer (L_{T}) and also the impact of the output filter inductor (L_{f}) of the small signal inverter, which results in

$$L_{\mathrm{E}} = L_{\mathrm{V}} - L_{\mathrm{T}} - L_{\mathrm{f}}. \tag{3.103}$$

The control system of the small signal inverter is also based on a PI-type controller and for the calculation of the PI controller parameters the Bode-plot design method is used with following constraints

$$t_\mathrm{r} = 13\ \mu\mathrm{s}, \qquad p_\mathrm{overshoot} = 10\ \%, \qquad e_\infty = 0. \tag{3.104}$$

Now the same design procedure as for the MPB controller design can be applied. The requirements are transferred for the the open loop transfer function and design is done in the continuous q-domain. Therefore the time constant T_N results in

$$T_\mathrm{N} = 19\ \mu\mathrm{s} \tag{3.105}$$

according to Eq. 3.96. The gain of the integral term according to Eq. 3.97 can be determined by

$$k_\mathrm{c} = 0.871. \tag{3.106}$$

The resulting controller parameters of the PI-type controller for the small-signal inverter are summarized in table 3.10.

Table 3.10: Filter and control parameters of the small signal inverter output filter

Parameter	Value
Filter inductor	$L_\mathrm{f} = 180\ \mu\mathrm{H}$
Filter capacitors	$C_\mathrm{f} = 220\ \mathrm{nF}$
Damping resistor	$R_\mathrm{S} = 25\ \Omega$
Damping inductor	$L_\mathrm{S} = 60\ \mu\mathrm{H}$
PI controller gain	$k_\mathrm{p} = 0.871$
PI controller time constant	$T_\mathrm{N} = 19\ \mu\mathrm{s}$
PT1 cut off frequency	$f_\mathrm{c,PT1} = 100\ \mathrm{kHz}$

The frequency response of the the closed-loop transfer function with feed-forward $T_{\mathrm{rf}}^{\#}(q)$ (depicted in Fig. 3.20) shows a strongly improved phase displacement compared to frequency response of the closed-loop transfer function $T_{\mathrm{r}}^{\#}(q)$ without additional feed-forward. As can be seen the designed controller can fulfil the requirement of the small-signal bandwidth of $f_{\mathrm{bw}} = 2$ kHz for CAACS .

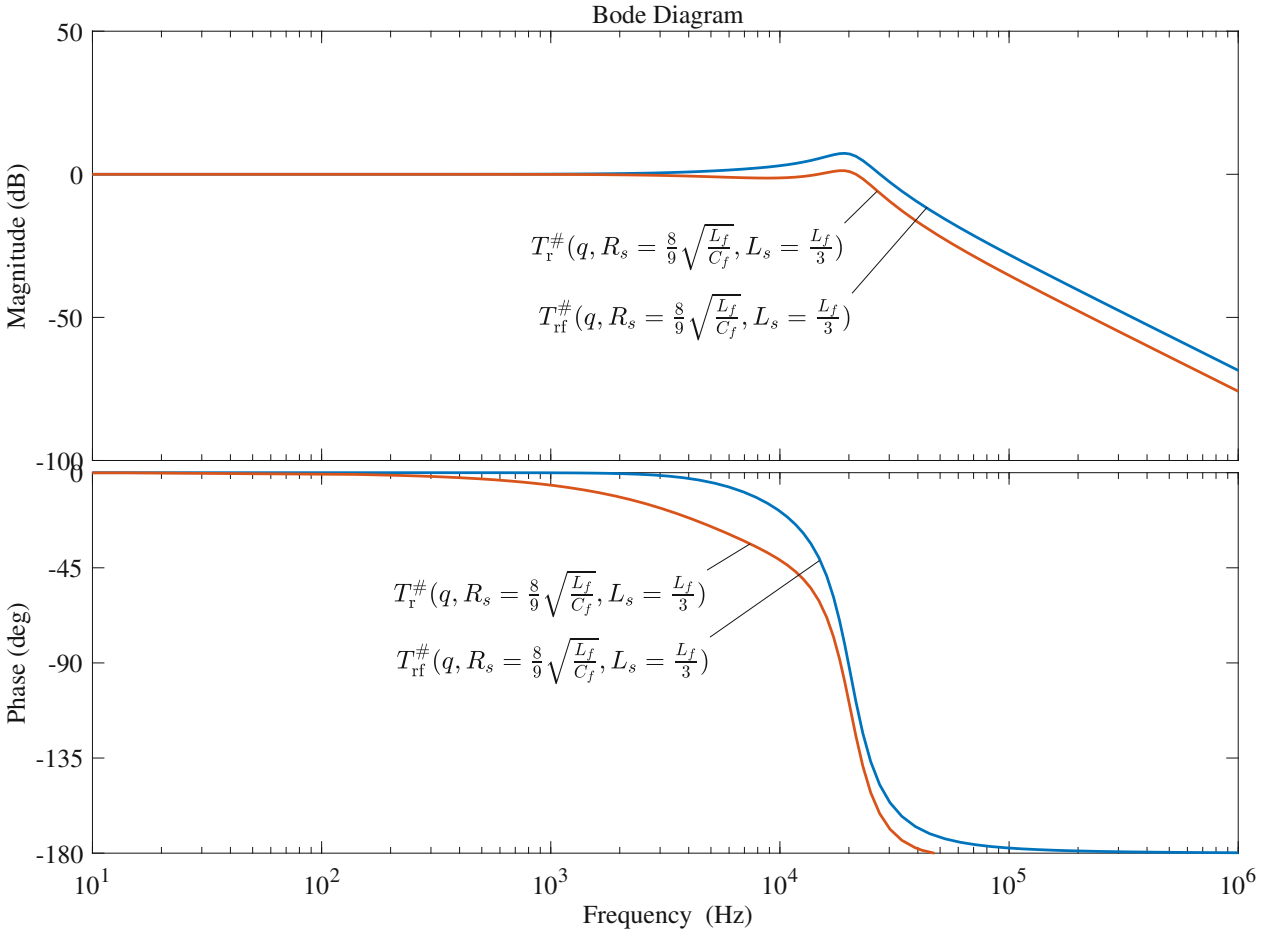


Figure 3.20: Bode plots of the closed-loop transfer function $T_{\mathrm{r}}^{\#}(q)$ and closed-loop transfer function with feed-forward $T_{\mathrm{rf}}^{\#}(q)$ of the small-signal inverter output stage without load and corresponding controller PI-type controller parameters.

The discrete step response of the closed-loop transfer function without feed-forward $T_{\mathrm{r}}(z)$ and closed-loop transfer function with feed-forward $T_{\mathrm{rf}}(z)$ is shown in Fig. 3.21. The closed-loop transfer function without feed-forward $T_{\mathrm{r}}(z)$ fulfils the requirement of the maximum overshoot, but since the controller is designed for fast response, the step response of the closed-loop transfer function with feed-forward $T_{\mathrm{rf}}(z)$ shows a maximum overshoot of $p_{\mathrm{overshoot}} = 70$ %. Fig. 3.22 shows the simulated SSI output voltage $v_{\mathrm{out,SSI}}$ for a load step from 2.8 Ω to 2.1 Ω (resulting in a current step of 3 A).

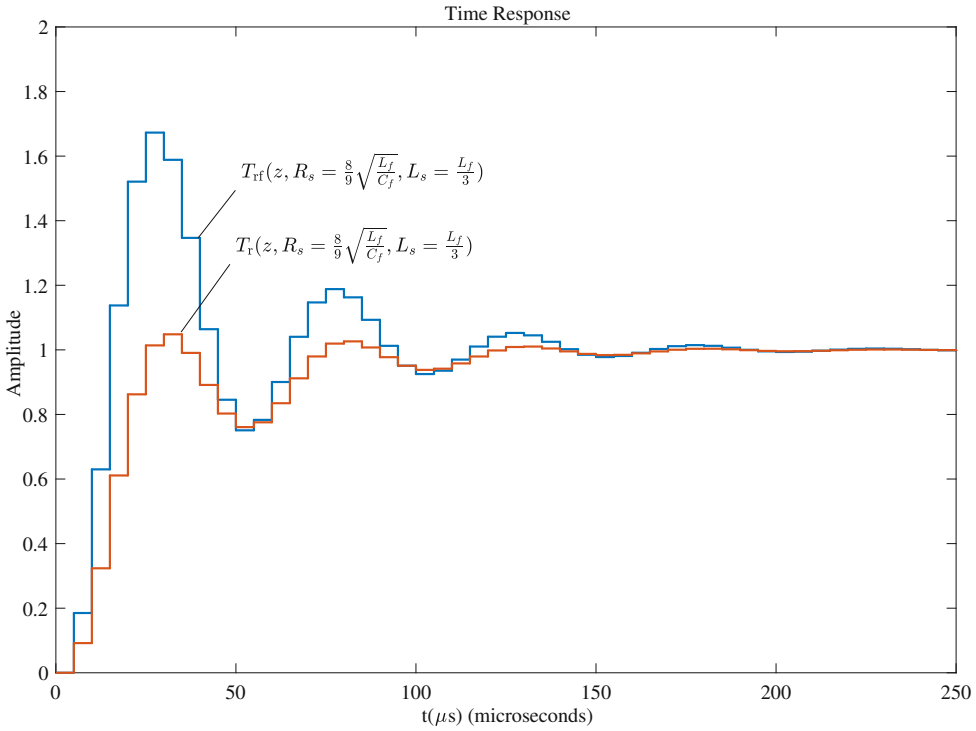


Figure 3.21: Step response of the closed-loop transfer function $T_{\mathrm{r}}(z)$ and closed-loop transfer function with feed-forward $T_{\mathrm{rf}}(z)$of the small-signal inverter output stage without load and corresponding controller PI-type controller parameters.

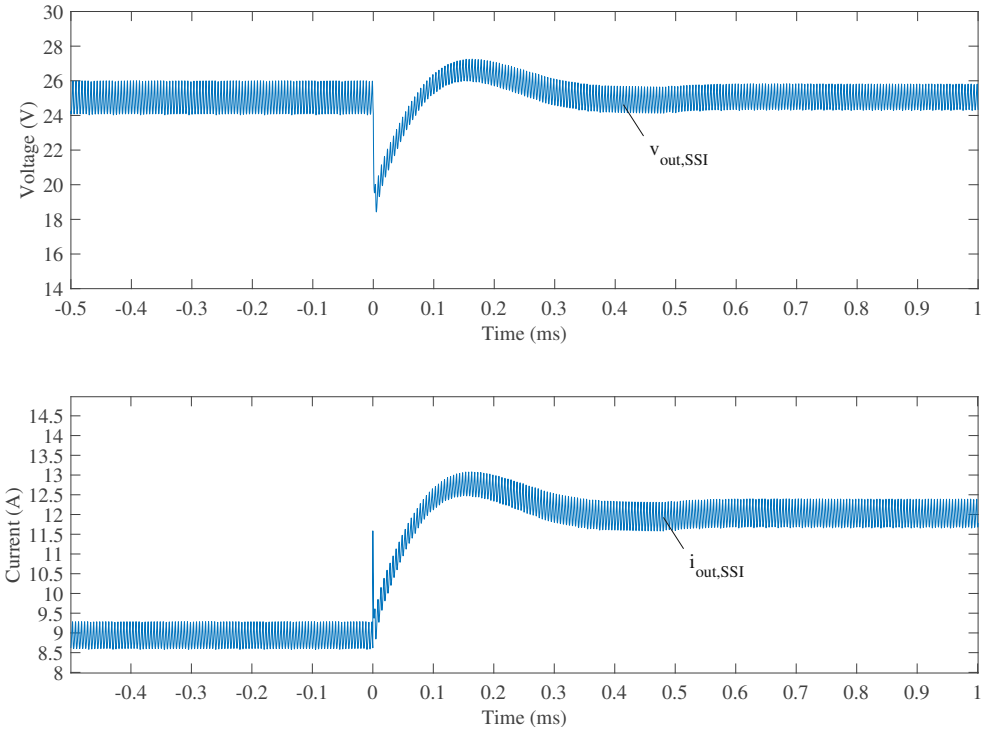


Figure 3.22: Simulated SSI output voltage $v_{\mathrm{out,SSI}}$ for a load step from 2.8 Ω to 2.1 Ω.

Fig. 3.23 shows the Bode diagram of the SSI output impedance, according to the control scheme of the CAACS in Fig. 3.18. It must be noted, that a a PI-type voltage controller and the LC-output filter is considered but an additional virtual impedance is not applied.

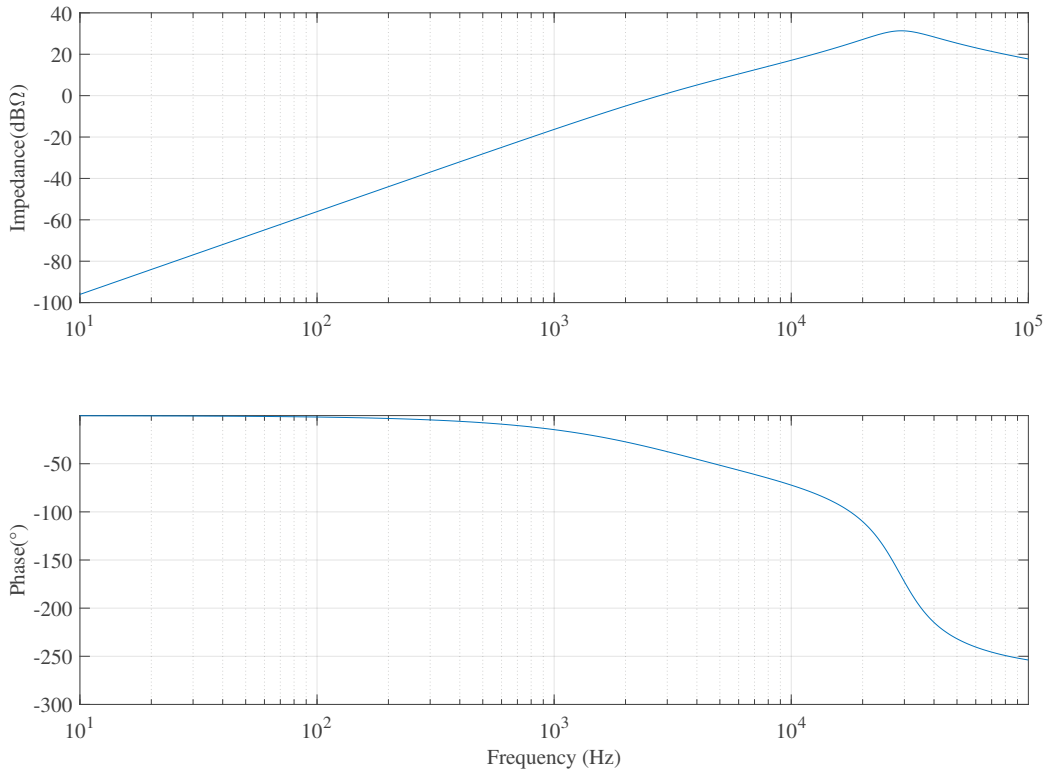


Figure 3.23: Bode diagram of the SSI output impedance including PI-type voltage controller and LC-output filter.

Chapter 4

Cascaded Advanced AC-Simulator - Prototype and Detailed Analysis

4.1 Prototype

As a result of the analysis in chapter 3, the cascaded advanced AC-simulator with coupling transformer is the most promising concept for the implementation of a grid simulator system with virtual impedance. Therefore this concept is prototypically implemented. For the laboratory setup consisting of a large-signal inverter and a small-signal inverter, a conventional AC-simulator (Regatron ACS) is used as large-signal inverter. The MPB with dedicated small-signal inverter has been designed and implemented separately based on the results in section 3.2.

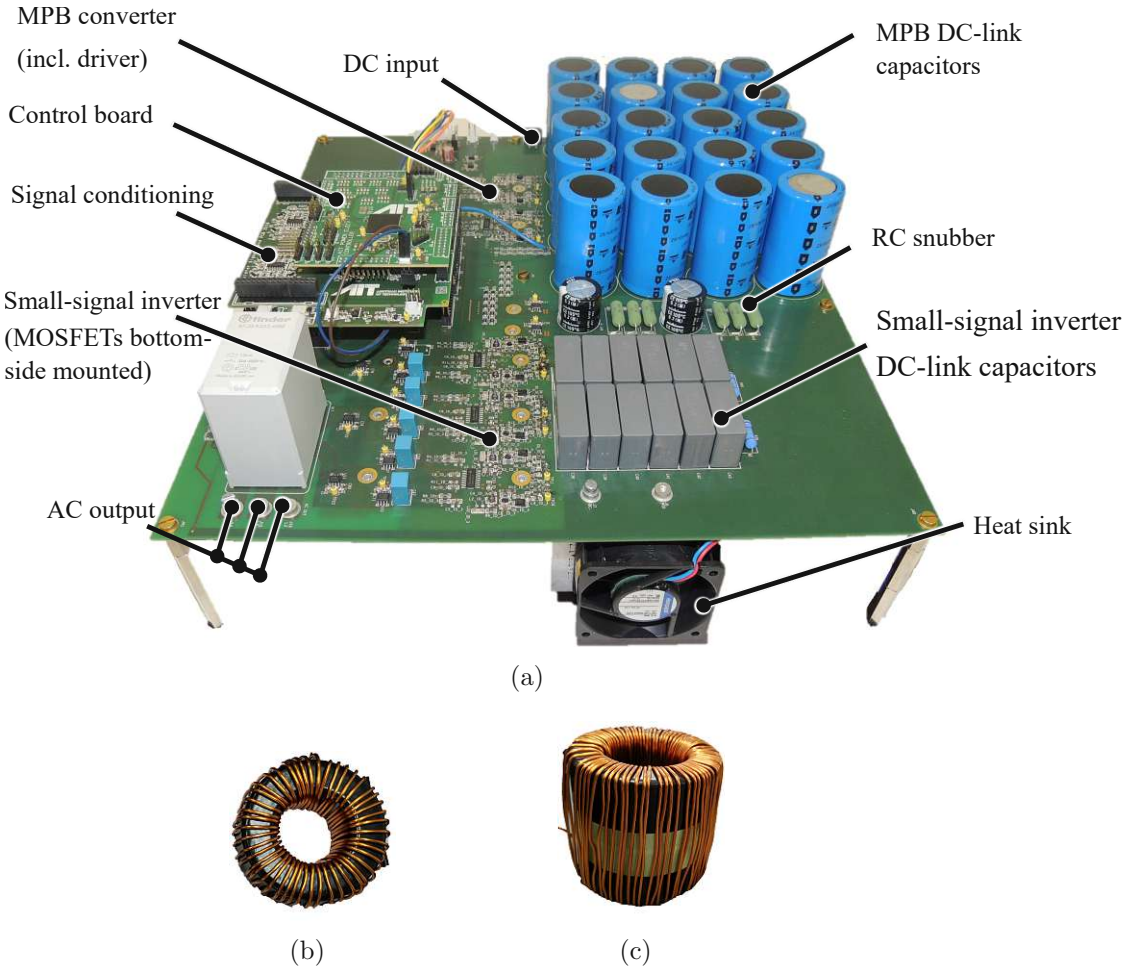
Detailed specifications of the small-signal inverter with bidirectional MPB are given in Tab. 4.1. Based on these specifications the power components for the laboratory prototype were selected according to Tab.4.2.

Table 4.1: Design specifications of the built three-phase small-signal inverter with a bidirectional MPB converter as input-stage.

Parameter	Value
Nominal output power:	$S_\mathrm{n} = 1230$ W
Nominal rms output voltage:	$V_\mathrm{out,LN} = 28$ $\mathrm{V_{rms}}$
Maximum peak output voltage:	$\hat{V}_\mathrm{out,LN,max} = 40$ V
Nominal DC-link voltage MPB:	$V_\mathrm{DC,MPB} = 400$ V
Nominal DC-link voltage:	$V_\mathrm{DC,SSI} = 100$ V
Nominal rms output current:	$I_\mathrm{out} = 14.5$ $\mathrm{A_{rms}}$
Maximum peak output current:	$\hat{I}_\mathrm{out,max} = 20.5$ A
Small-signal bandwidth:	$f_\mathrm{bw} = 2$ kHz
Emulated resistance range:	$R_\mathrm{V} = 0\ \Omega - 1\ \Omega$
Emulated inductance range:	$L_\mathrm{V} = 0$ mH $- 5$ mH

Table 4.2: Power components for the laboratory prototype of the small signal inverter with bidirectional MPB.

Parameter	Value
S_{MPB}	SiC-MOSFET SCT3080AL, Rohm
S_{SSI}	MOSFET IXFP36N20X3, IXSYS
$C_{\mathrm{DC,MPB}}$	470 $\mu F/500\ V$ $\times 20$, Elektrolyt, Kemet
$L_{\mathrm{f,dc}}$	830 μH, Kool Mu Torroid, Magnetics Inc., N=69 turns
$C_{\mathrm{DC,SSI}}$	10 $\mu F/250\ V$ $\times 12$,, MKP , Kemet
L_{f}	180 μH, Kool Mu Torroid, Magnetics Inc., N=47 turns
$C_{\mathrm{f,}\frac{\mathrm{p}}{\mathrm{n}}}$	220 $nF/250\ V$, MKP , TDK



(a)

(b) (c)

Figure 4.1: (a) Laboratory prototype of the small-signal inverter including MPB. Power board consisting of MPB & small-signal DC-link capacitors, MPB converter & small-signal inverter (MOSFETS bottom-side mounted), small-signal output capacitors, snubber circuits and driver circuits. Filter inductors are not mounted on the power board and depicted separately. (b) Small-signal inverter output filter inductor (180 μH). (c) MPB output filter inductor (830 μH)

The laboratory prototype of the small-signal inverter including MPB is shown in Fig. 4.1 (a). Corresponding output filter inductors for the small signal inverter and the MPB are shown in Fig. 4.1 (b) and 4.1 (c) respectively. The system consists mainly of three different boards - power-, controller- and signal conditioning-board. The power board includes both, the MPB as well as the small signal inverter power components, such as DC-link capacitors, MOSFETs, gate drives, voltage measurement circuits, current sensors and snubber circuits for proper damping of the output filters. The controller board contains the DSP (TI TMS320F28379D Dual Delphino with 200 MHz), auxiliary power supply as well as analogue and digital interfaces. The signal conditioning board is mainly consisting of differential amplifier circuits, in order to convert the current and voltage signals from the power board to lower voltage levels for the ADC channels of the controller board. The MPB is the first stage of the system and has been designed for input voltages of 400 V_{DC}. This enables the implementation of a SiC MOSFET (Rohm SCT3080AL) for the MPB converter, which results in lower switching losses compared to standard MOSFETs/IGBTs solutions, due to lower switching losses and conduction losses during partial load mode. The DC-link of the MPB is designed for a voltage ripple at rated current below 5 %, which results in a capacitor value of $C_{DC} = 10$ mF.

The three-phase small signal output stage is a fast switching power stage with a switching frequency of at least $f_{s,SSI} = 200$ kHz. Due to the relatively low DC-link voltage of $V_{DC,SSI} = 100$ V, MOSFETS with $V_{DS,max} = 200$ V are selected (IXFP36N20X3-ND). The DC-Link of the three-phase small-signal inverter is designed for filtering $f_{s,SSI} = 200$ kHz noise, with a DC-link capacitor value of $C_{DC} = 60$ μF. A RC parallel snubber circuit is used for damping the resonance frequency of the MPB output filter structure and a RL parallel snubber circuits are used for the small-signal output filter.

The digital control system is implemented on the DSP, which contains analogue signal conversion, state machine, MPB voltage controllers, small-signal voltage controllers and virtual impedance generation. Moreover, the DSP is used for PWM gate signal generation for the MPB as well as the small-signal voltage. Since the switching frequency was set to $f_{s,SSI} = 200$ kHz, the sample time of the controller results in $T_s = 5$ μs.

For the validation of the experimental setup, different tests were applied and evaluated in the time domain as well as in the frequency domain. Therefore, the following tests were performed:

- Time domain : Three-phase system with resistive loading. Regatron serves as large-signal AC-simulator and the small-signal inverter including the MPB providing the resistive-inductive impedance emulation (according to Fig. 3.12).
  - Analysis of the overall output voltage with different virtual impedance values.
  - Analysis of the small signal output (virtual impedance voltage drop) with different virtual impedance values.
- Frequency domain: Single phase AC-sweep analysis of the output impedance (emulated grid impedance).

4.1.1 Time Domain Analysis

As aforementioned the experimental setup of the cascaded advanced AC-simulator, for the time domain analysis, is implemented with a conventional Regatron ACS used as three-phase large-signal inverter, the three-phase laboratory prototype as small-signal inverter and three-phase power resistor as EUT. The laboratory prototype and the Regatron ACS are connected in series and are galvanically isolated with a YY0 transformer. Since only discrete values ($R_1 = 83\ \Omega$, $R_2 = 41\ \Omega$, $R_3 = 21\ \Omega$, ...) can be set with the power resistor and the measurements should be done under nominal conditions, $R_{\mathrm{EUT}} = 21\ \Omega$ has been chosen. Considering the nominal voltage of $V_{\mathrm{out,LN}} = 230\ \mathrm{V_{rms}}$ (phase to neutral) / $f_{\mathrm{nom}} = 50$ Hz, the output current results in $I_{\mathrm{out}} = 10.95$ A if no additional impedance is applied. Based on the maximum impedance, the tests were carried out with different impedance values listed in Tab. 4.3.

Table 4.3: Virtual impedance values for the time domain analysis of the cascaded advanced AC-simulator.

Parameter	R_v	L_v
$Z_{\mathrm{V},1}$	$1\ \Omega$	$5\ mH$
$Z_{\mathrm{V},2}$	$0.5\ \Omega$	$2.5\ mH$
$Z_{\mathrm{V},3}$	$0.25\ \Omega$	$1.25\ mH$
$Z_{\mathrm{V},4}$	$0.19\ \Omega$	$0.52\ mH$

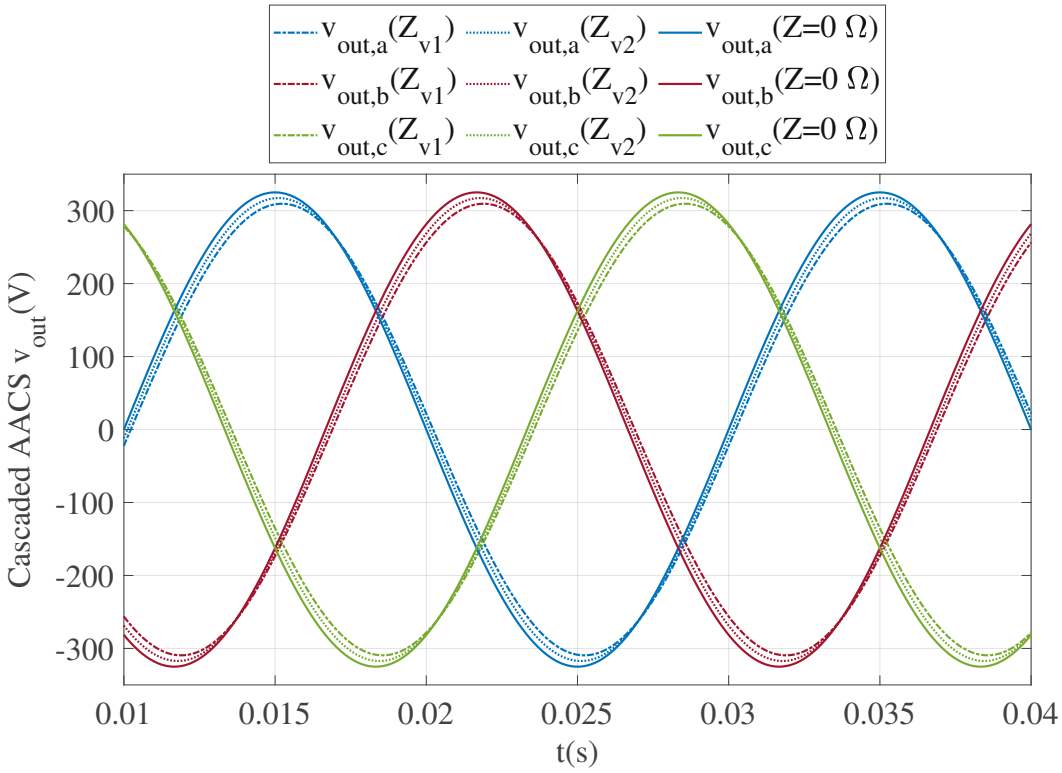


Figure 4.2: Three-phase time domain measurement signals of the overall output voltage with different virtual grid impedance values and nominal frequency $f_{\mathrm{nom}} = 50\ Hz$

The overall output voltage of the system and the generated voltage drop, caused by the virtual impedance of the small-signal inverter, were measured. The measurement results of the three-phase overall output voltages are depicted in Fig. 4.2 and more detailed single-phase measurements are shown in Fig. 4.3.

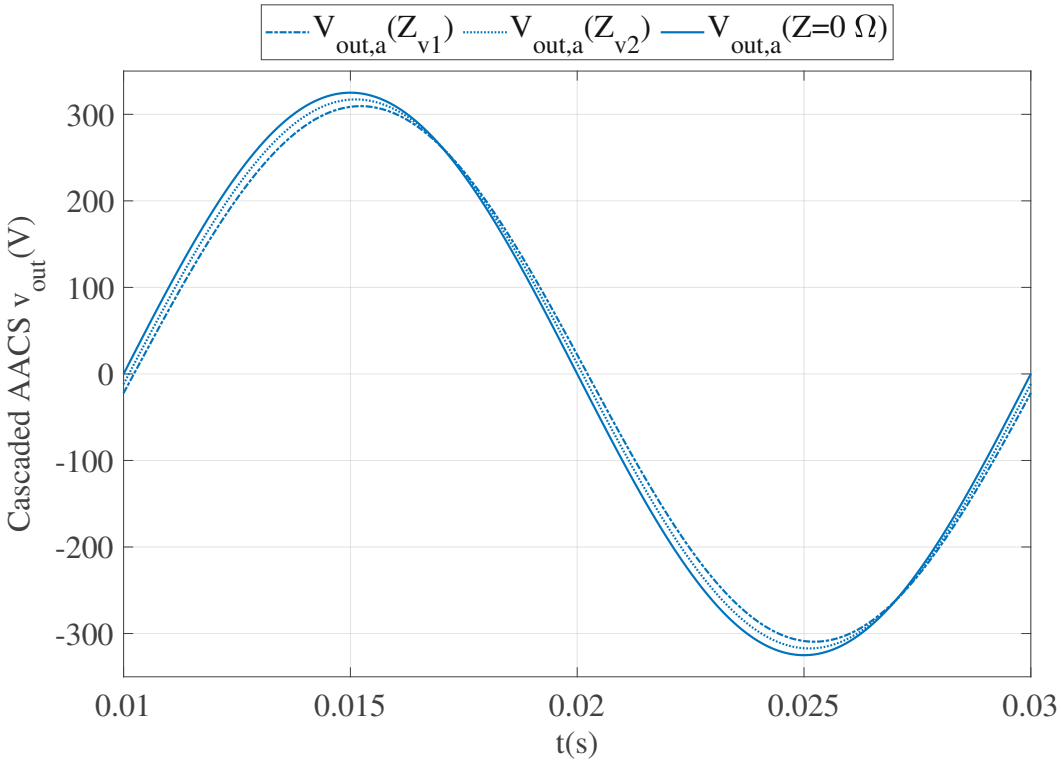


Figure 4.3: Singel-phase time domain measurement signals of the overall output voltage with different virtual grid impedance values and nominal frequency $f_{\text{nom}} = 50\ Hz$.

Furthermore, the measurement results of the experimental setup are validated against ideal reference values shown in Tab. 4.3.

Table 4.4: Validation of overall output voltage measurement results $V_{\text{out,LN}}$ compared to calculated values.

Z	Measured $V_{out,LN}$	Calculated $V_{out,LN}$
$Z_{\text{v},1}$	218.055 V	218.988 V
$Z_{\text{v},2}$	223.947 V	224.501 V
$Z_{\text{v}} = 0$	230 V	230.01 V

Since the small-signal inverter has to compensate the voltage drop of the coupling transformer, the voltage drop caused by the virtual impedance cannot be measured directly. In order to determine the accuracy of the virtual impedance, the voltage drop $v_{\text{out,VI}}(t)$ must be evaluated from the output voltage measurement of the large-signal inverter $v_{\text{out,LSI}}(t)$ and the total output voltage of the CAACS $v_{\text{out}}(t)$ according to

$$v_{\text{out,VI}}(t) = v_{\text{out,LSI}}(t) - v_{\text{out}}(t). \tag{4.1}$$

The results of the generated voltage drop of the virtual impedance are depicted in Fig. 4.4 and more detailed single-phase results are shown in Fig. 4.5.

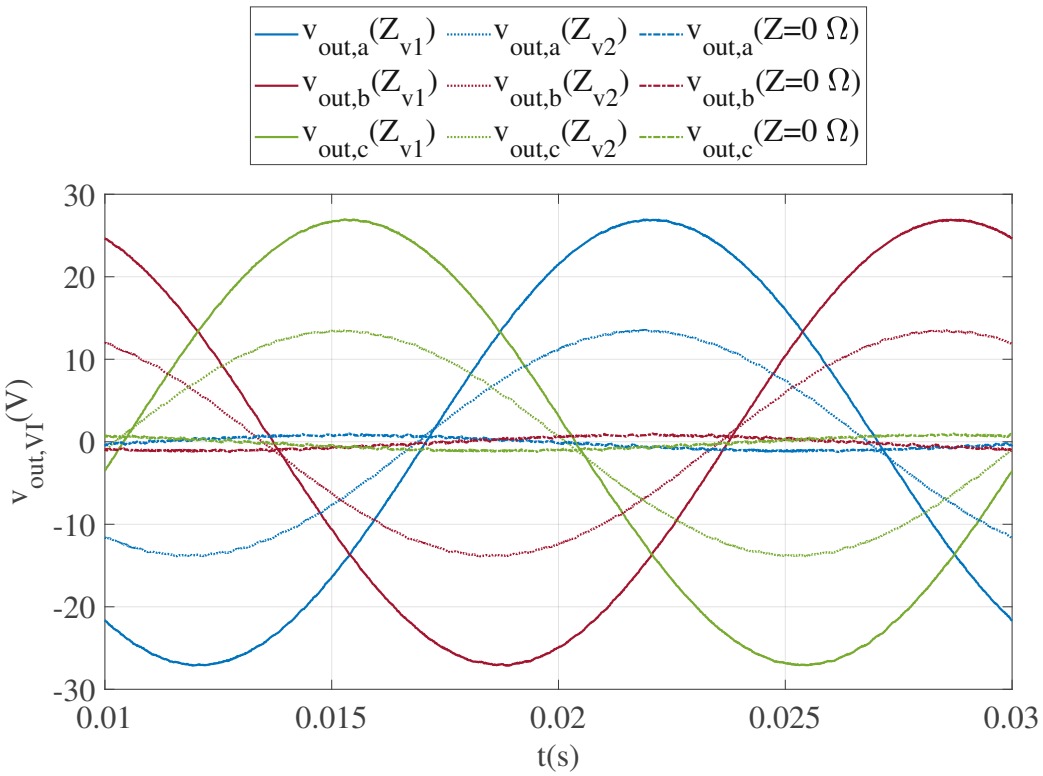


Figure 4.4: Three-phase time domain measurement signals of the voltage drop caused by the virtual impedance with nominal frequency $f_{\text{nom}} = 50$ Hz.

In Tab. 4.5 the validation of the virtual impedance voltage drop results $V_{\text{out,VI}}$ is shown. For this purpose the voltage drop of the virtual impedance is calculated by

$$V_{\text{out,VI,calc}} = V_{\text{out,LSI}} \frac{Z_{\text{v,i}}}{Z_{\text{Total}}} \tag{4.2}$$

where $Z_{\text{v,i}}$ represents the resistive-inductive impedance value and Z_{Total} the overall impedance of the circuit including R_{EUT} given by

$$Z_{\text{v,i}} = \sqrt{R_{\text{v,i}}^2 + (\omega \cdot L_{\text{v,i}})^2} \qquad Z_{\text{Total}} = \sqrt{(R_{\text{v,i}} + R_{\text{EUT}})^2 + (\omega \cdot L_{\text{v,i}})^2}. \tag{4.3}$$

As can be seen, the maximum relative error is 4.2 % at the lowest virtual impedance value of $Z_{\text{v,4}}$. Since the low impedance value $Z_{\text{v,4}}$ causes also a low voltage drop value, the relative error is caused by the measurement accuracy and

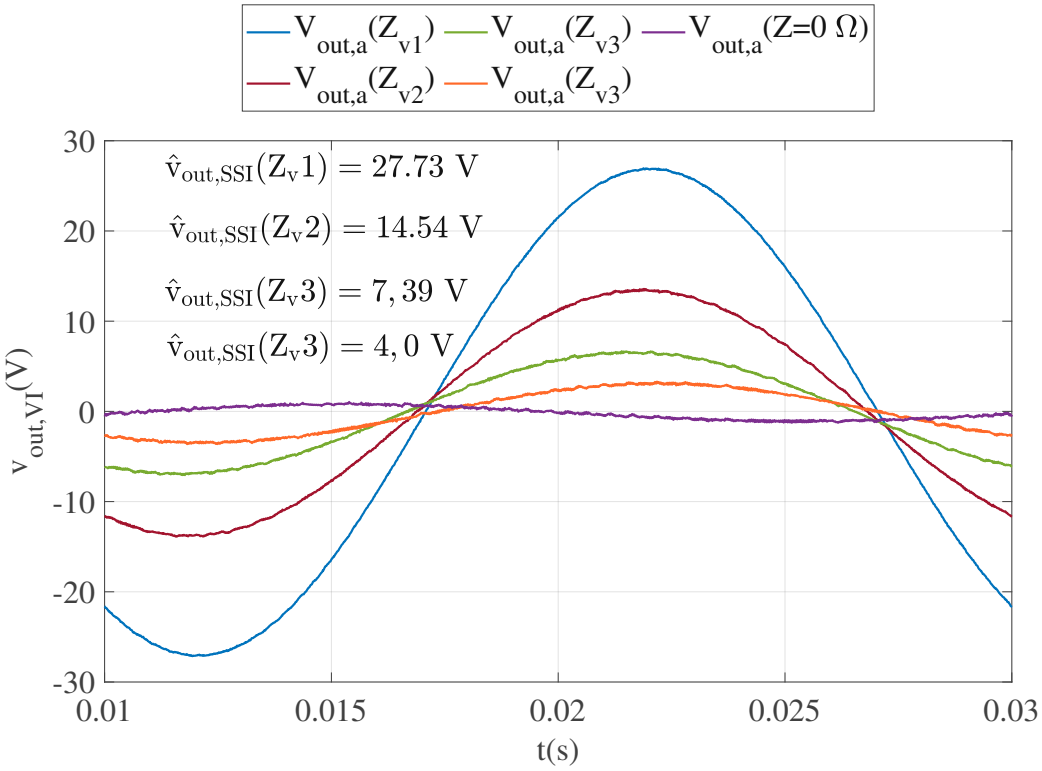


Figure 4.5: Single-phase time domain measurement signals of the voltage drop caused by the virtual impedance with nominal frequency $f_{\text{nom}} = 50$ Hz.

also the increasing impact of the output of the large-signal inverter.

Table 4.5: Validation of of the virtual impedance voltage drop results V_{SSI} with nominal frequency $f_{\text{nom}} = 50$ Hz compared to calculated values.

Z	$V_{\text{out,VI}}$	$V_{\text{out,VI,calc}}$	Rel. error
$Z_{\text{v},1}$	19.605 V	19.418 V	0.96 %
$Z_{\text{v},2}$	10.278 V	9.953 V	3.26 %
$Z_{\text{v},3}$	5.229 V	5.037 V	3.8 %
$Z_{\text{v},4}$	2.834 V	2.720 V	4.2 %

4.1.2 Frequency Domain Analysis of the laboratory prototype (small-signal inverter)

The frequency domain analysis is based on a comparison between ideal simulation results and measurement results of the following environments:

- Frequency domain analysis of a reference output impedance based on a PLECS offline simulation of an ideal RL-series element model (Fig. 4.7) - blue curve)
- Frequency domain analysis of the resulting measurements of the laboratory prototype (Fig. 4.7) - green curve)
- Frequency domain analysis of the resulting measurements of the laboratory prototype with filter impedance compensation (Fig. 4.7) - red curve)

In order to obtain a bode plot from the measurement data the Fast Fourier Transformation (FFT) has to be applied. Since only voltage and current measurements are available the logarithmic magnitude of the output impedance is then derived by

$$|Z|_{\mathrm{db}} = 20log\left(\frac{|U(e^{j\theta}|}{|I(e^{j\theta}|}\right) \tag{4.4}$$

and the corresponding argument of the phase is calculated by

$$arg(Z)) = arctan\left(\frac{\Im\left(\frac{U(e^{j\theta}}{I(e^{j\theta}}\right)}{\Re\left(\frac{U(e^{j\theta}}{I(e^{j\theta}}\right)}\right) \tag{4.5}$$

For the frequency domain analysis of the small-signal inverter, which is based on an voltage source converter topology, a current has to be injected as small-signal distortion. Together with the voltage response at a specific frequency, the output impedance characteristics can be determined according to Eq. 4.4 and Eq. 4.5. For the validation of the measurement results an ideal inductive-resistive series element is used as reference system. Therefore an offline simulation was performed with an ideal current source acting as small-signal perturbation and appropriate voltage measurement to evaluate the voltage response.

In order to apply the small-signal perturbation on the laboratory prototype several methods are for disposal ([8]):

- High bandwidth current source connected directly at the output of the advanced AC-simulator.
- High bandwidth voltage source connected via power resistor at the output of the cascaded advanced AC-simulator. Therefore the voltage source has to be synchronized with the large-signal inverter and must provide the large signal fundamental (230 V / 50 Hz) and must inject also the small-signals at the same time.
- High bandwidth voltage source connected via power resistor at the output of the cascaded advanced AC-simulator without generating a large signal.

Due to the absence of the large-signal only small-signal distortions has to be injected.

Fig. 4.6 shows the measurement setup for the AC-sweep analysis and validation of the small-signal inverter. Since all three phases are designed to operate independently, a single-phase measurement is performed. A Regatron ACS is used as high bandwidth voltage source, which is connected via a $R_L = 15\ \Omega$ power resistor. The voltage as well as the current is measured directly at the output of the small-signal inverter.

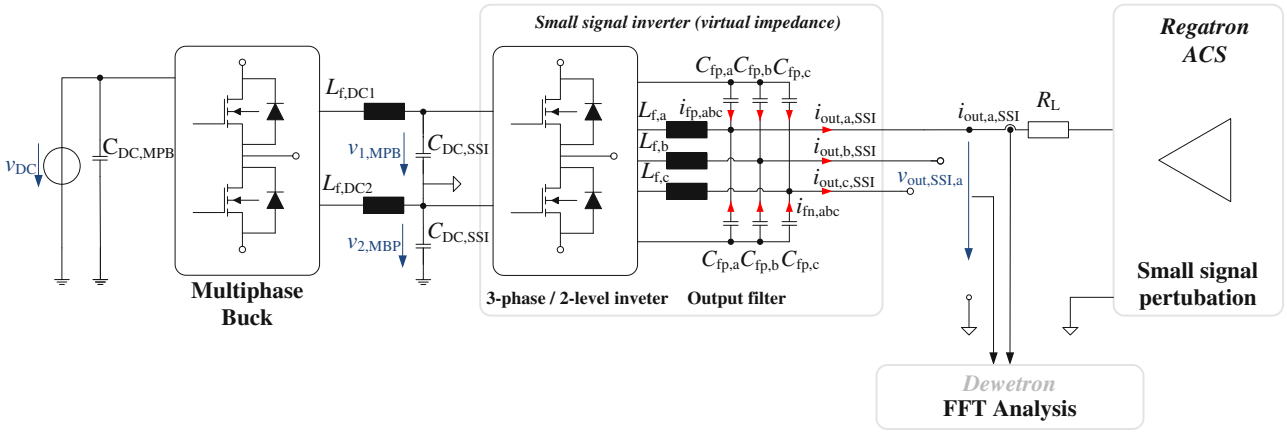
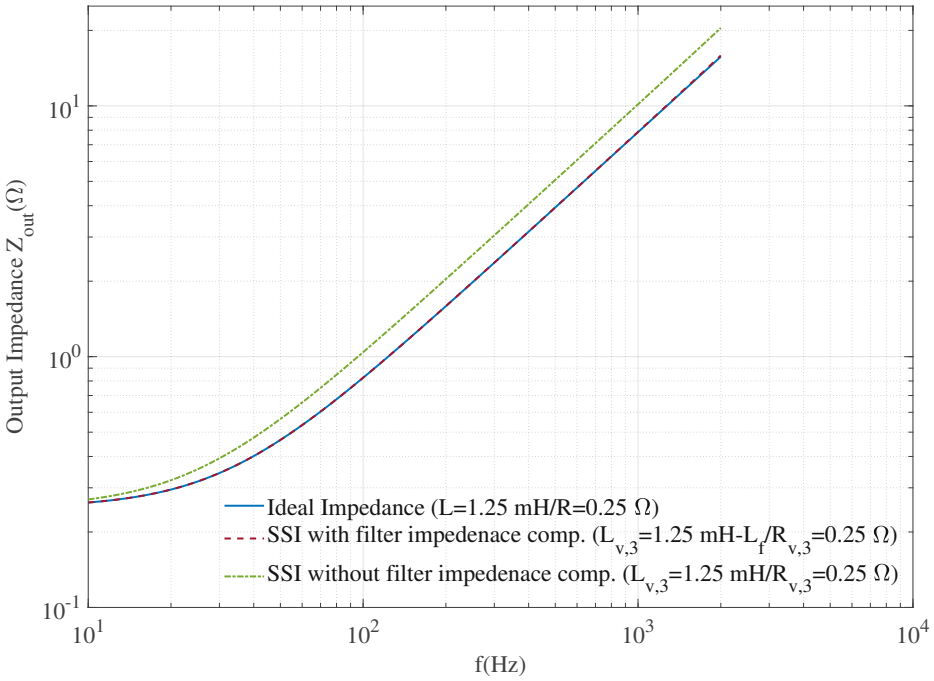
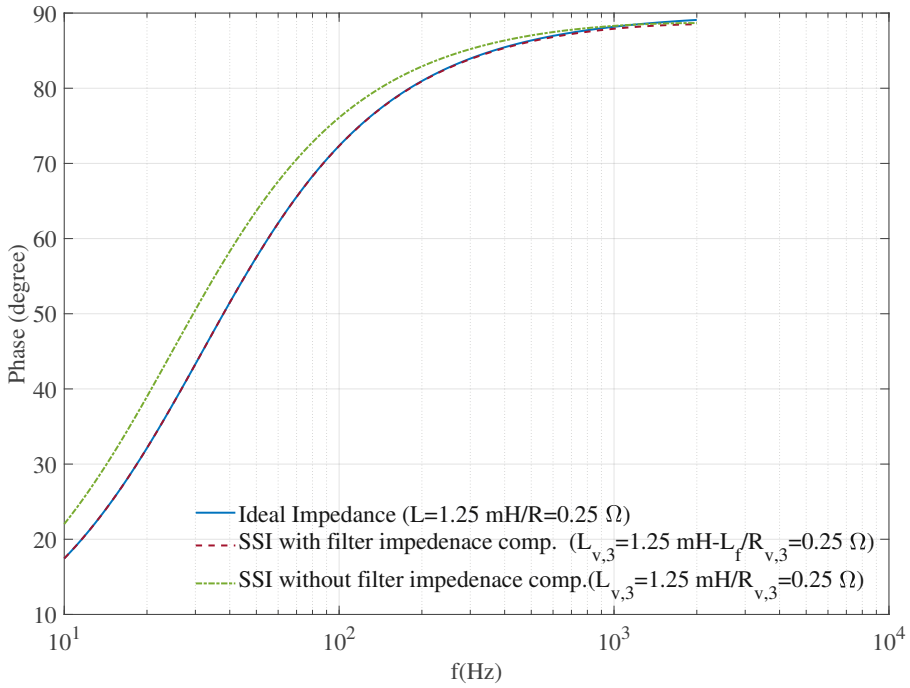


Figure 4.6: Measurement setup of the small-signal inverter - AC-sweep analysis

Fig. 4.7 shows the results of the AC-sweep analysis of the small-signal inverter compared with a reference model. As described before, the reference model is based on a resistive-inductive series element (Ideal impedance - blue curve) offline simulation. The measurement results are based on the setup according to Fig. 4.6. The simulation results (Ideal Impedance - blue curve) and the measurement results of the laboratory prototype with filter impedance compensation (SSI filter impedenace comp. - red curve) coincide very well. In the range of 10 Hz to 100 Hz the magnitude of the impedance shows almost resistive behaviour and for frequencies above 200 Hz the inductive part of the impedance dominates the characteristic. The measurement results of the laboratory prototype without filter impedance compensation (SSI - green curve) are showing deviations of the magnitude and the phase, compared to the simulation results (Ideal Impedance - blue curve). Consequently, in order to guarantee accurate impedance emulation, the results are showing that the output impedances of each component of the CAACS has to be analysed and compensated if necessary. Therefore, also the output impedance of the large-signal inverter and of the transformer has to be analysed.



(a)



(b)

Figure 4.7: Bode plot of the output impedance of the small signal inverter (a) Magnitude (Ω) (b) Phase (degree)

4.2 Output Impedance Compensation

The CAACS, depicted in Fig. 4.8, basically consists of three parts, the large-signal inverter, the small-signal inverter and a coupling transformer.

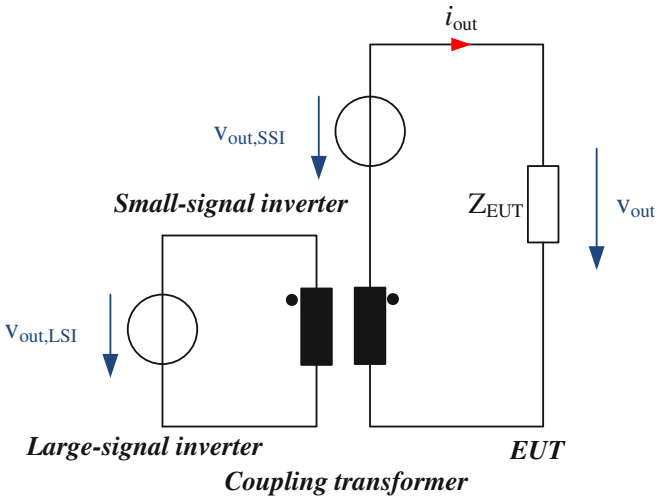


Figure 4.8: Equivalent circuit of a single phase CAACS consisting of a large-signal inverter, coupling transformer and a small signal inverter.

The proposed system uses a Regatron ACS as large-signal inverter and a laboratory prototype as small-signal inverter. For the operation of such a system, the output impedance of each component must be taken into account and compensated, if necessary in order to receive accurate impedance emulation. The presented results in Sec. 4.1.2 are showing small deviations compared to the reference system, which are mainly caused by the simple compensation algorithm which is based on an resistive-inductive model. This approach is already sufficient for the compensation of passive resistive-inductive parasitics (e.g. filter inductors, coupling transformer). However, the information of the frequency dependent output impedance of the large-signal inverter must be available for proper compensation of these parasitics. Therefore the measured transfer function of the output impedance characteristic of a Regatron ACS is implemented into the small signal inverter control scheme, which compensates the error in addition to the emulation of the virtual impedance.

In particular, the emulation of low impedance values require an accurate compensation of the passive parasitics and the output impedance $Z_{\mathrm{out,LSI}}$ of the large signal inverter. The passive parasitics are dominated by the transformer resistance $R_{\mathrm{cu,T}} = 280\ m\Omega$ and the equivalent stray inductance $L_{\sigma,\mathrm{T}} = 850\ \mu H$ of the used YY0-transformer. This is compensated by considering in the impedance emulation according to

$$R_{\mathrm{v}} = R_{\mathrm{v}}^{*} - R_{\mathrm{cu,T}} \tag{4.6}$$

$$L_{\mathrm{v}} = L_{\mathrm{v}}^{*} - L_{\sigma,\mathrm{T}} \tag{4.7}$$

while the output impedance of the Regatron TC.ACS.50 is measured[1] and ana-

[1]Measurement data was provided by Regatron AG

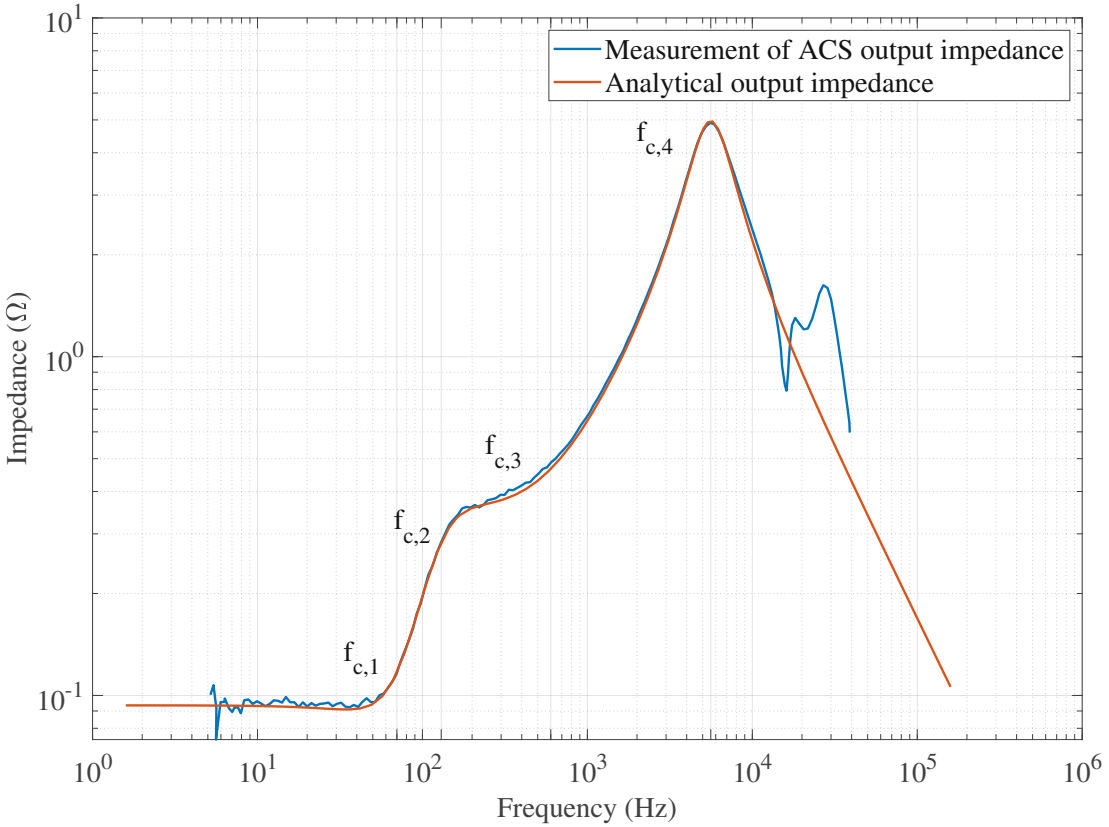


Figure 4.9: Bode plot of the measured and analytical approximation of the output impedance $Z_{\text{out,LSI}}$ of the large signal inverter (Regatron TC.ACS.50) [10].

lytically described according to Fig. 4.9. The bode plot of the measured output impedance indicates a two-stage LC filter and as can be seen the magnitude of the output impedance $Z_{\text{out,LSI}}$ is dominated by inductive behaviour for frequencies below $f_{\text{c,4}} = 5600$ Hz. Since the magnitude of the output impedance $Z_{\text{out,LSI}}$ decreases for frequencies beyond $f_{\text{c,4}}$ the output filter capacitors are dominating the characteristics. For low frequencies in the range of 0 - $f_{\text{c,1}}$ the output impedance shows no frequency dependency, which corresponds to resistive behaviour with a value of $Z_{\text{out,LSI}}(f_{\text{c,1}}) = 90$ mΩ. For the further analysis the cut-off frequencies has to be determined and also the damping ratio for the second-order transfer functions. The obtained parameters are listed in Tab. 4.6.

Based on these parameters for the cut-off frequencies and damping ratios an analytical approximation of the transfer function of the output impedance can be derived by

$$Z_{\text{out,LSI}}(s) = \frac{V_{\text{out,LSI}}(s)}{I_{\text{out,LSI}}(s)} = Z_{12} \cdot Z_3 \cdot Z_4. \tag{4.8}$$

Therefore the individual components of the output impedance can be approximated by

Table 4.6: Parameters and cut-off frequencies of the output impedance transfer function of the large signal inverter (Regatron TC.ACS.50) [10]

Parameter	Value
Gain V	0.0935 Ω
Damping ratio θ_1	1.15
Damping ratio θ_2	1.1
Damping ratio θ_4	0.65
Cut-off frequency $f_{c,1}$	70 Hz
Cut-off frequency $f_{c,2}$	130 Hz
Cut-off frequency $f_{c,3}$	600 Hz
Cut-off frequency $f_{c,4}$	5600 Hz

$$Z_{12}(s) = V \cdot \frac{\frac{s^2}{\omega_{c,1}^2} + \frac{s\theta_1}{\omega_{c,1}} + 1}{\frac{s^2}{\omega_{c,2}^2} + \frac{s\theta_2}{\omega_{c,2}} + 1} \tag{4.9}$$

$$Z_3(s) = \frac{s}{\omega_{c,3}} + 1 \tag{4.10}$$

$$Z_4(s) = \frac{1}{\frac{s^2}{\omega_{c,4}^2} + \frac{s\theta_4}{\omega_{c,4}} + 1}. \tag{4.11}$$

The analytical approximation of the transfer function can be used now for the implementation if the compensation algorithm into the the control scheme of the small-signal inverter. Therefore the discrete transfer function of the output impedance is calculated by

$$Z_{\text{out,LSI}}(z) = V \cdot \frac{5.388z^3 - 16.053z^2 + 15.936z - 5.274}{z^4 - 3.864z^3 + 5.623z^2 - 3.653z + 0.8942} \tag{4.12}$$

applying the zero-order hold (ZOH) transformation method and a sample rate of $T_s = 5\ \mu s$.

The single-phase control scheme of the cascaded advanced AC-simulator including an output impedance compensation algorithm of large-signal inverter is depicted in Fig. 4.10.

The control scheme is based on a PI-type voltage controller according to section 3.2.4. In addition the virtual output impedance is realized by measuring the output current signal, which is processed by a P-element and a DT1-element in parallel for the emulation of the resistive-inductive grid impedance. For damping the critical resonance frequency of the LC filter RL passive damping circuit is implemented. The ACS impedance element contains the discrete transfer function of the large-signal inverter output impedance, which is used for the compensation algorithm.

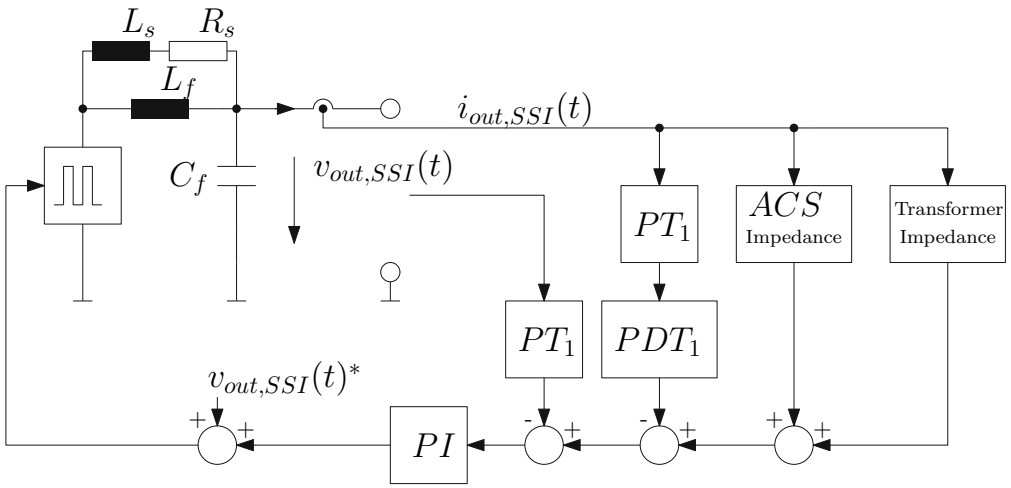


Figure 4.10: Single-phase control scheme of the SSI with passive damped LC filter, virtual resistive-inductive impedance and output impedance compensation.

In section 4.1 the operation with resistive load and different virtual impedance values has been presented. Since the frequency domain analysis were made with a relativly large impedance value ($Z_{\mathrm{v},3}$), the impact of the large-signal output impedance could be neglected. Fig. 4.11 shows the output impedance $Z_{\mathrm{out,LSI}}$ and the virtual impedance values ($Z_{\mathrm{v},1} \ldots Z_{\mathrm{v},4}$).

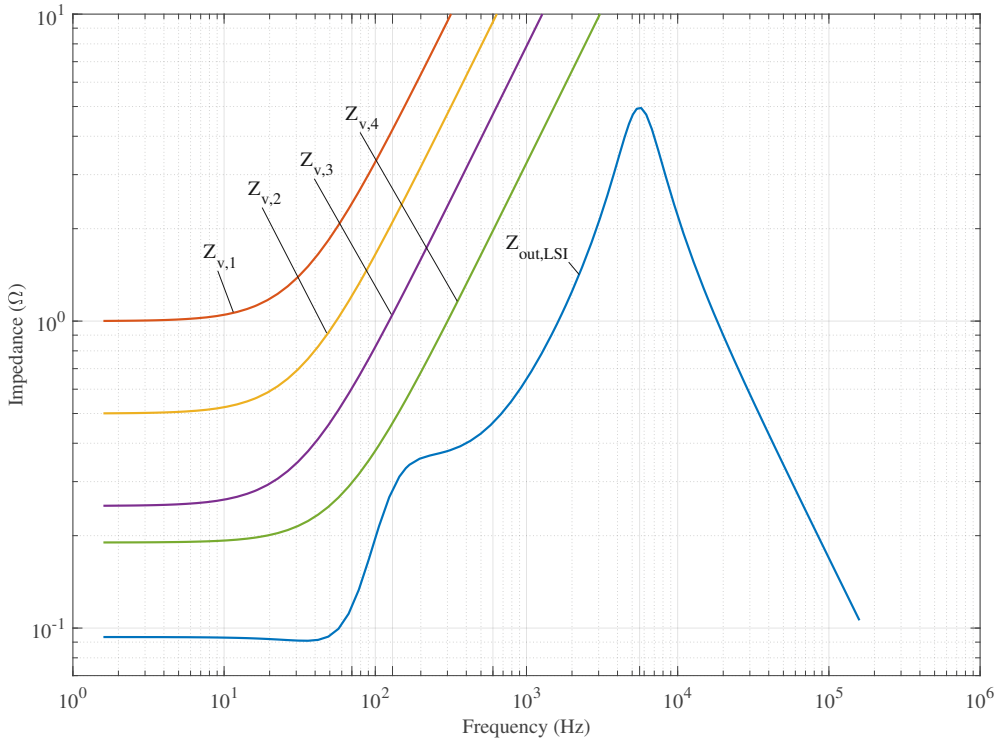


Figure 4.11: Bode plot of the of the large-signal inverter output impedance $Z_{\mathrm{out,LSI}}$ and the virtual impedance values ($Z_{\mathrm{v},1} \ldots Z_{\mathrm{v},4}$).

However, if small grid impedance values are emulated the compensation algorithm has to be validated. Therefore the control structure was implemented according to Fig. 4.10 and the measurement results are evaluated in time domain and frequency domain:

- Time domain: Three phase cascaded AC simulator system with resistive load (i) enabled and (ii) disabled compensation algorithm
- Frequency domain: Single phase cascaded AC simulator system (i) enabled and (ii) disabled compensation algorithm

4.2.1 Time Domain Analysis

The setup for validation of the compensation algorithm in the time domain is equal to Fig. 3.12. Analysing the output of the large-signal inverter (Fig. 4.9) the output impedance of the large-signal inverter (Regatron ACS) is relatively low ($Z_{\text{out,LSI}}(f_{\text{c,1}}) = 190$ mΩ) for frequency values in the vicinity of $f_{\text{nom}} = 50$ Hz. In order to demonstrate the impact of the output impedance and the corresponding compensation algorithm, the frequency of the large-signal inverter was set to $f = 500$ Hz. The value of the laboratory power resistor was set to $R_{\text{EUT}} = 21\ \Omega$ and is used as EUT. The parameters for the time domain tests are listed in Tab. 4.7.

Table 4.7: Parameters for the time domain analysis of the cascaded advanced AC-simulator with output impedance compensation algorithm

Parameter	Value
Virtual resistor	$R_{\text{v,1}} = R_{\text{v,2}} = 190$ mΩ
Virtual inductor	$L_{\text{v,1}} = 520\ \mu H, L_{\text{v,2}} = 50\ \mu$H
Large signal voltage (Mains voltage)	$V_{\text{out,LN}} = 230\ \text{V}_{\text{rms}}$
Large signal frequency	$f = 500$ Hz
Load resistor	$R_{\text{EUT}} = 21\ \Omega$

As stated before, two test scenarios have been made and are depicted in Fig. 4.12 for a virtual impedance value of $R_{\text{v,1}} = 190$ mΩ and $L_{\text{v,1}} = 520\ \mu$H and in Fig. 4.13 or a virtual impedance value of $R_{\text{v,2}} = 190$ mΩ and $L_{\text{v,2}} = 50\ \mu$H. Both test scenarios were carried out with (scenario 1) and without compensation (scenario 2) of the large-signal output impedance. Also a reference signal has been measured for both test scenarios, where no virtual impedance was applied. As the virtual impedance value, in Fig. 4.12, is significantly higher than the large-signal output impedance, only a small deviation between the compensated $v_{\text{out,abc,comp}}(Z_{\text{v1}})$ and the uncompensated signal $v_{\text{out,abc}}(Z_{\text{v1}})$ can be observed. Due to this high virtual impedance value a phase displacement angle of $\varphi \approx 2.1°$ can be measured between the reference signal $v_{\text{out,abc}}(Z = 0)$ and the $v_{\text{out,abc}}(Z_{\text{v1}})$.

The compensation shows a more significant impact for the emulation of low virtual impedance values. A test was performed with low virtual impedance values $R_{\text{v,2}} = 190$ mΩ and $L_{\text{v,2}} = 50\ \mu$H. Fig. 4.13 shows the measurement re-

sults of compensated and uncompensated large-signal inverter output impedance. This results are showing a significant deviation between the peak value of the uncompensated voltage $\hat{v}_{\text{out,abc}}(Z_{\text{v2}}) = 318,5$ V and the compensated voltage $\hat{v}_{\text{out,abc,comp}}(Z_{\text{v2}}) = 322,5$ V.

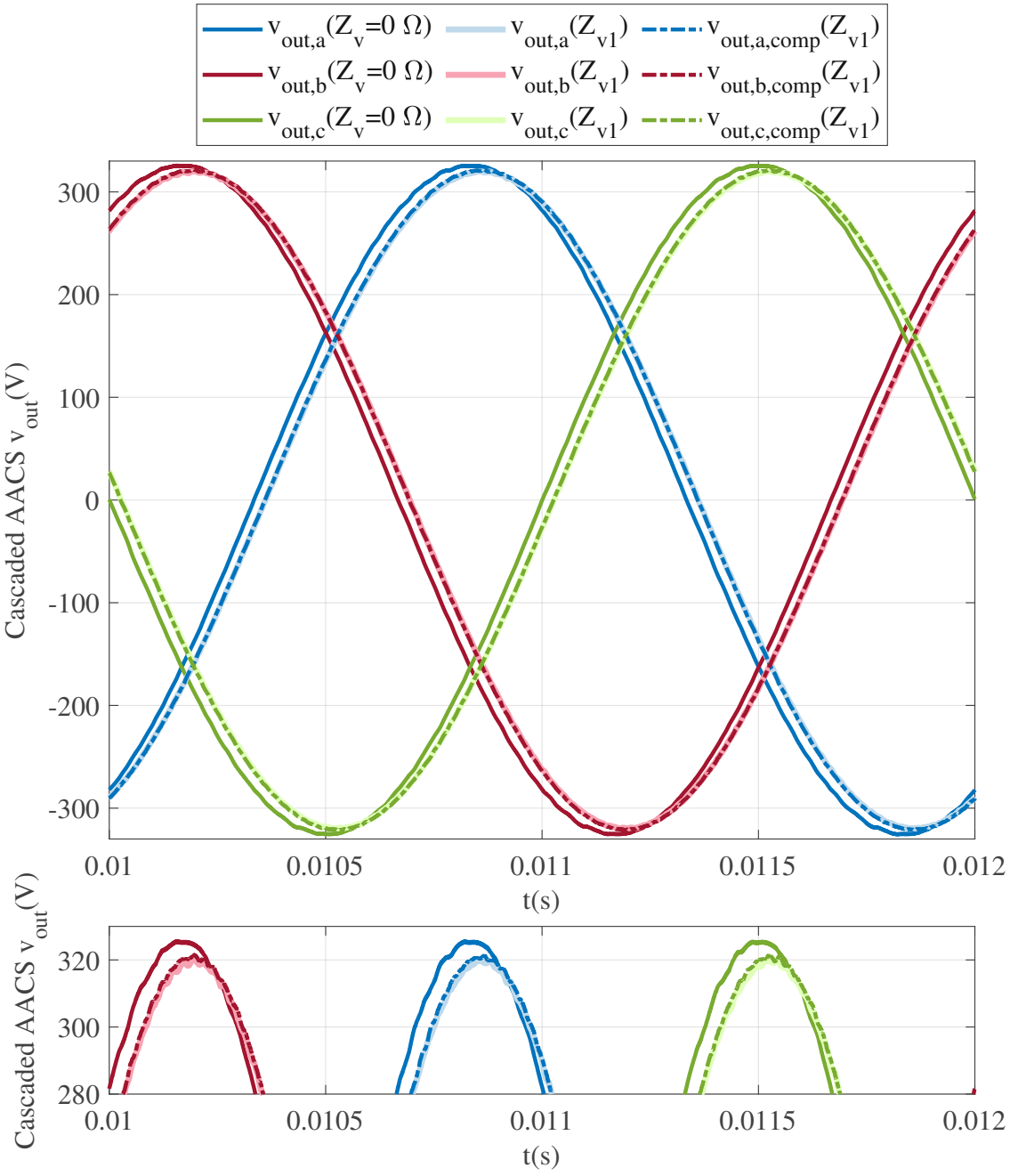


Figure 4.12: Comparison of compensated and uncompensated time domain measurement signals of three-phase cascaded advanced AC-simulator system with virtual impedance $R_{\text{v,1}} = 190$ mΩ, $L_{\text{v,1}} = 520$ μH (large signal voltage $V_{\text{out,ls,RMS}} = 230$ V, $f = 500$ Hz) [10].

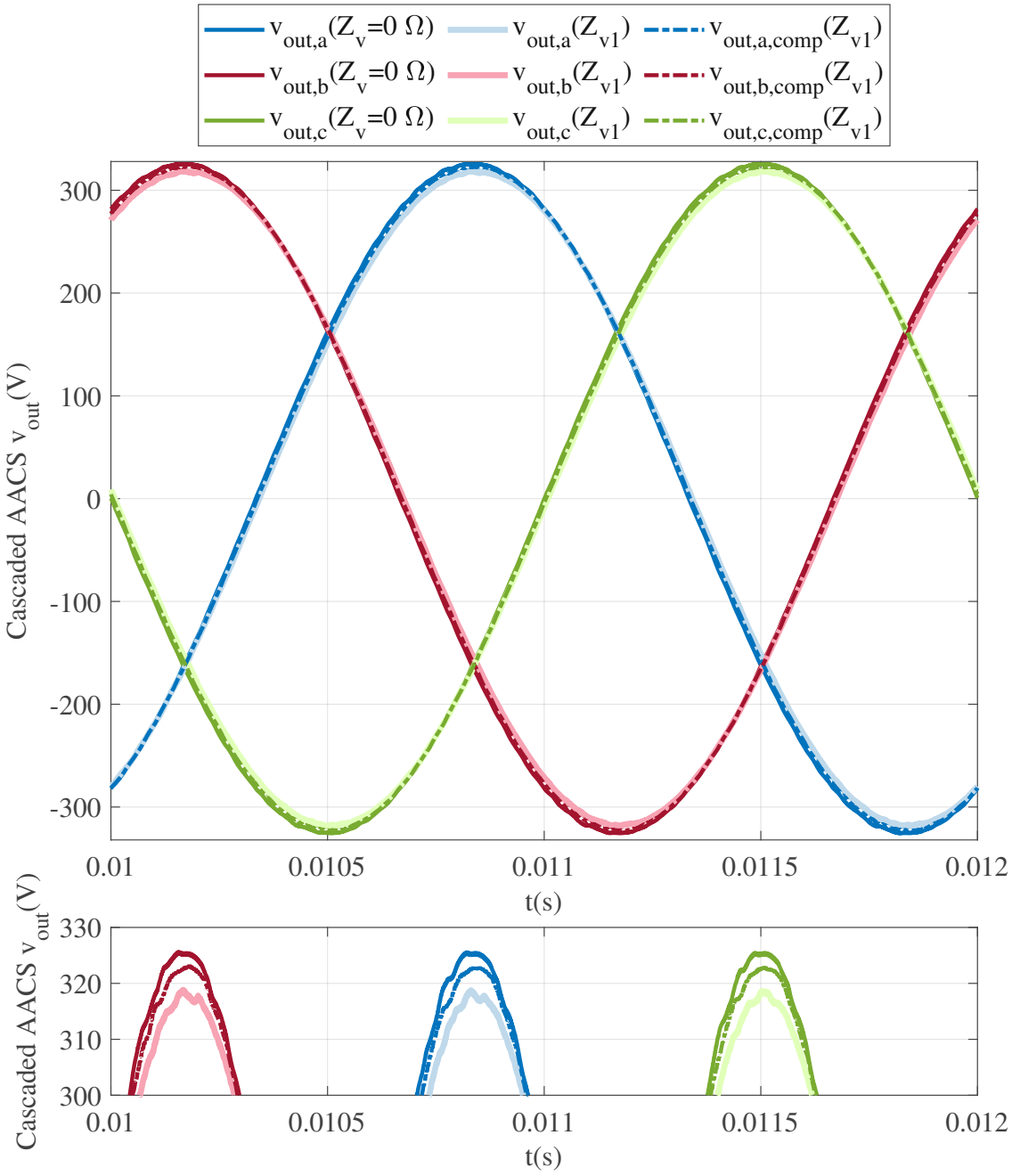


Figure 4.13: Comparison of compensated and uncompensated time domain measurement signals of three-phase cascaded advanced AC-simulator system with virtual impedance $R_{\mathrm{v},1} = 190\ \mathrm{m\Omega}$, $L_{\mathrm{v},1} = 50\ \mu\mathrm{H}$ (large signal voltage $V_{\mathrm{out,ls,RMS}} = 230\ \mathrm{V}$, $f = 500\ \mathrm{Hz}$) [10].

4.2.2 Frequency Domain Analysis

In section 4.1.2 the frequency domain analysis was done for the small-signal inverter, in order to determine the output impedance. In this section the frequency domain analysis for the cascaded advanced AC-simulator including the large-signal generator is presented. Measurements with and without compensation algorithm are compared to an ideal resistive-inductive reference impedance. The frequency domain analysis is done for a single phase setup. The implemented test bench is depicted in Fig. 4.14. Since the Regatron ACS is used as large-signal inverter, the linear power amplifier Spitzenberger & Spieß PAS10000 is used as small-signal perturbation for AC-sweep analysis. Based on the measured output voltage $v_{\mathrm{out,a}}$ and the corresponding output current $i_{\mathrm{out,a}}$ a FFT is performed and the resulting output impedance is calculated according to Eq. 4.4.

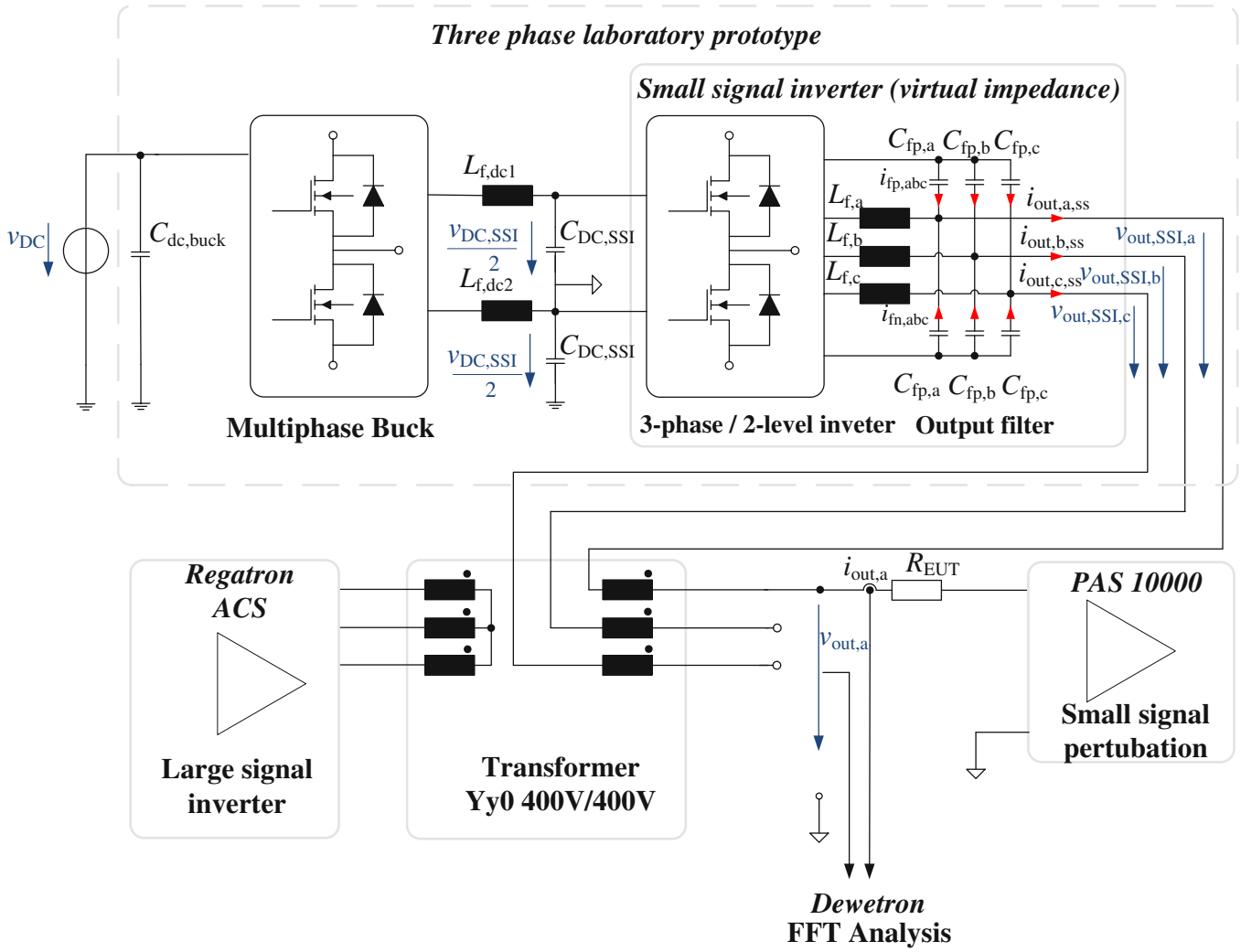


Figure 4.14: AC sweep setup for the cascaded advanced AC-Simulator with Regatron ACS (large signal inverter), proposed laboratory prototype (small signal inverter) and PAS 10000 linear power amplifier for small signal pertubation [10]

In Tab. 4.8 the parameters of the frequency domain analysis of the cascaded advanced AC-simulator with output impedance compensation algorithm are sum-

marized.

Table 4.8: Parameters of the frequency domain analysis of the cascaded advanced AC-simulator with output impedance compensation algorithm.

Parameter	Value
Virtual resistor	$R_{\mathrm{v},1} = R_{\mathrm{v},2} = 190$ mΩ
Virtual inductor	$L_{\mathrm{v},1} = 520$ μH, $L_{\mathrm{v},2} = 50$ μH
Small-signal pertubation	$\hat{v}_{pertubation} = 20$ V
Frequency range	$f = 10$ Hz $-$ 2 kHz
Power resistor	$R_{\mathrm{EUT}} = 43$ Ω

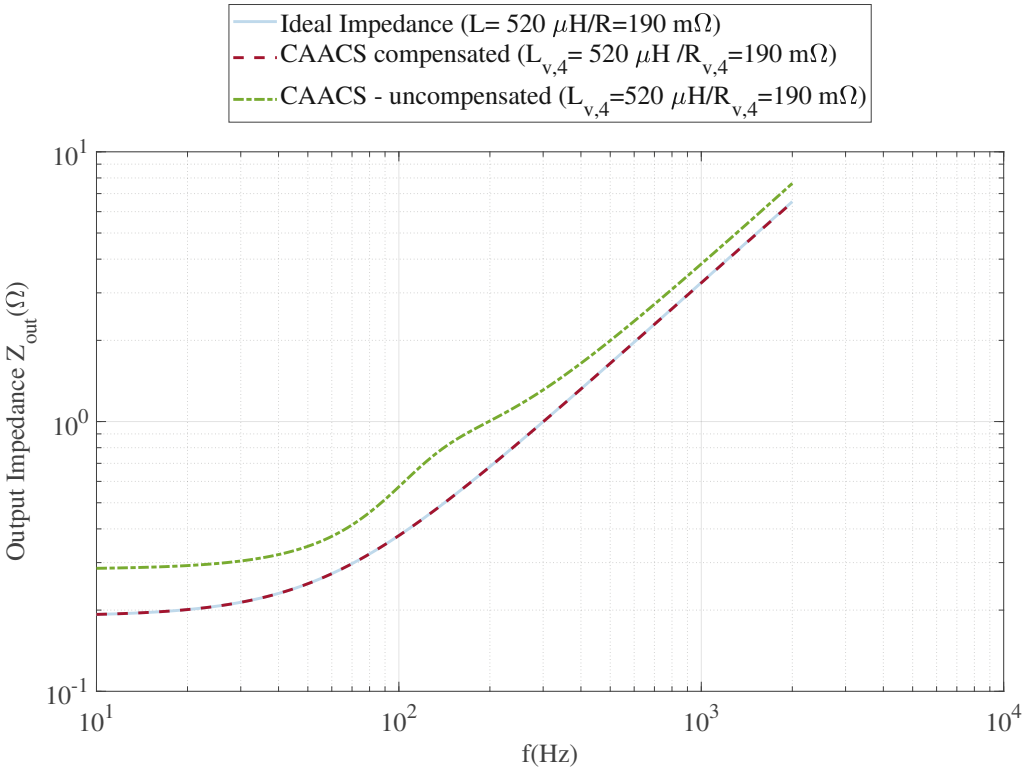
In Fig.4.15 the bode plot of measured compensated and uncompensated output impedance characteristics with virtual impedance of $R_{\mathrm{v},1} = 190$ mΩ, $L_{\mathrm{v},1} = 520$ μH are shown. In addition an ideal reference curve is also depicted in the diagram (blue curve). For frequencies above 100 Hz the inductive part of the impedance dominates. The uncompensated measurement curve (green curve) shows a slight deviation compared to the ideal reference and the compensated impedance characteristic (red curve).

The bode plot of measured compensated and uncompensated output impedance characteristics with virtual impedance of $R_{\mathrm{v},1} = 190$ mΩ, $L_{\mathrm{v},1} = 50$ μH is depicted in Fig. 4.16. As already with the time domain analysis, the active compensation algorithm shows a major impact on the measurement results. While the deviation between the ideal reference impedance characteristic (blue curve) and the compensated impedance characteristic (red curve) is negligible, the deviation between the uncompensated impedance characteristic (green curve) compared to ideal reference impedance characteristic (red curve) is relatively high.

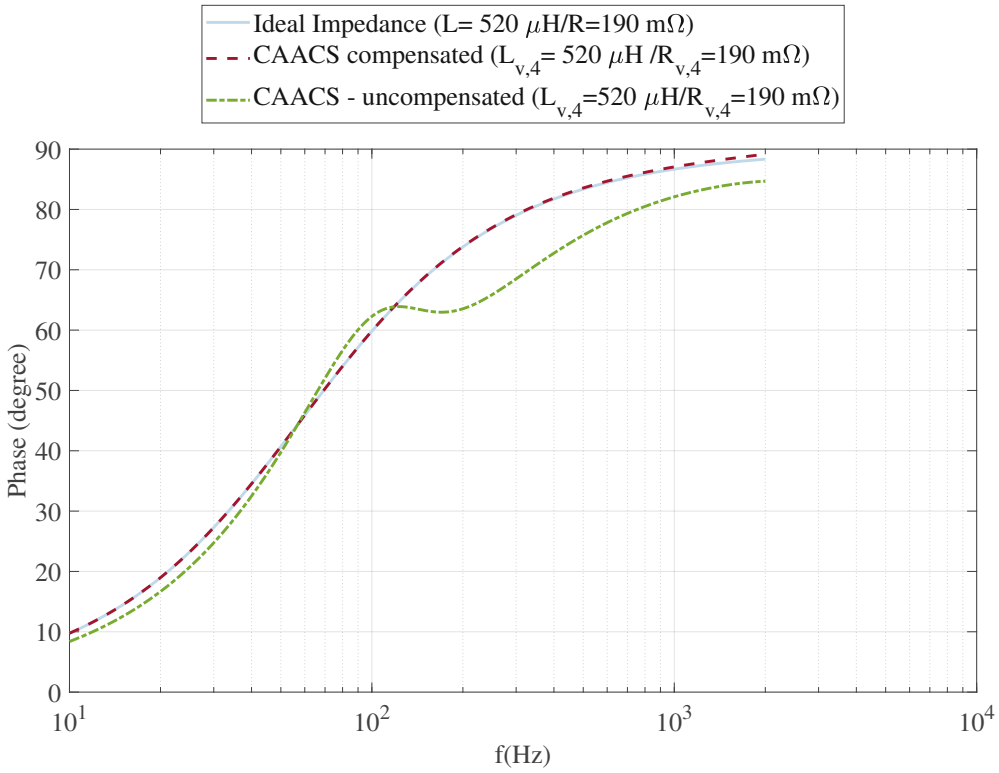
However, since the transformer impedance is affected by the temperature, the operating point of the CAACS has to be considered for an accurate transformer impedance compensation.

Fig. 4.17 shows the relative error of the measured compensated and uncompensated output impedance characteristics in relation to the ideal reference system for virtual impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 520$ μH. The maximum relative error of 60.78 % of the uncompensated virtual impedance appears at $f = 130$ Hz, whereas for the compensated impedance very small deviations can be observed around the frequency of 2 kHz.

The relative error for impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 50$ μH is depicted in Fig. 4.18. For such small virtual impedance values the relative error for the uncompensated measurements increases significantly to a maximum value of 174.4 % at $f = 224$ Hz.

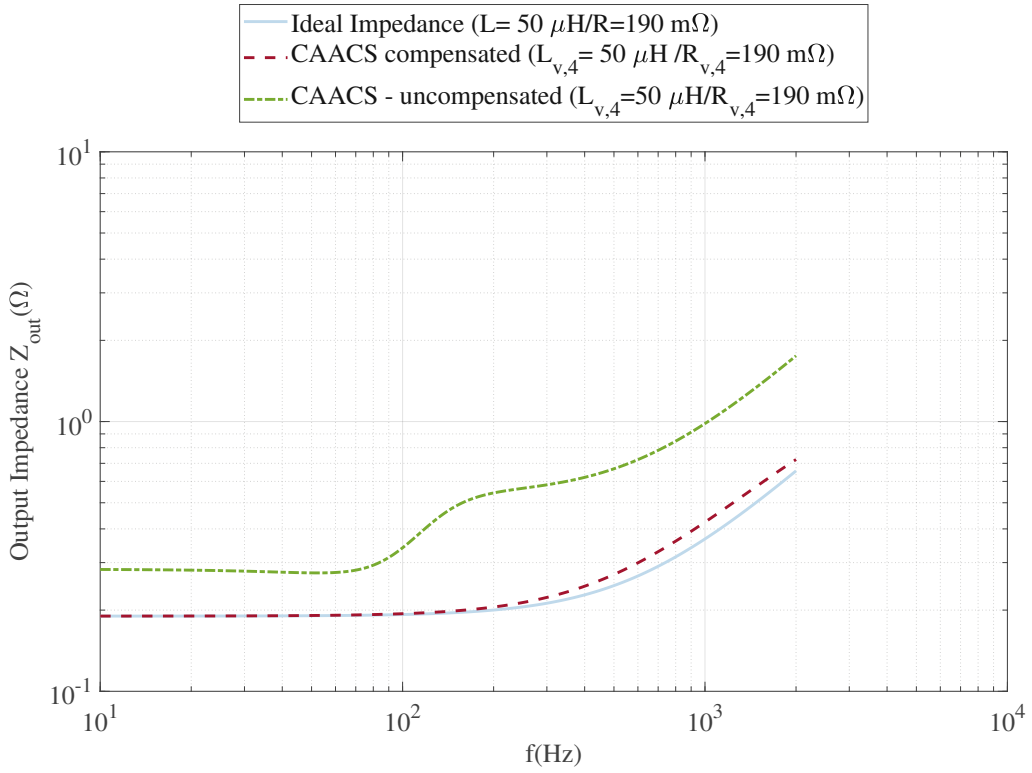


(a)

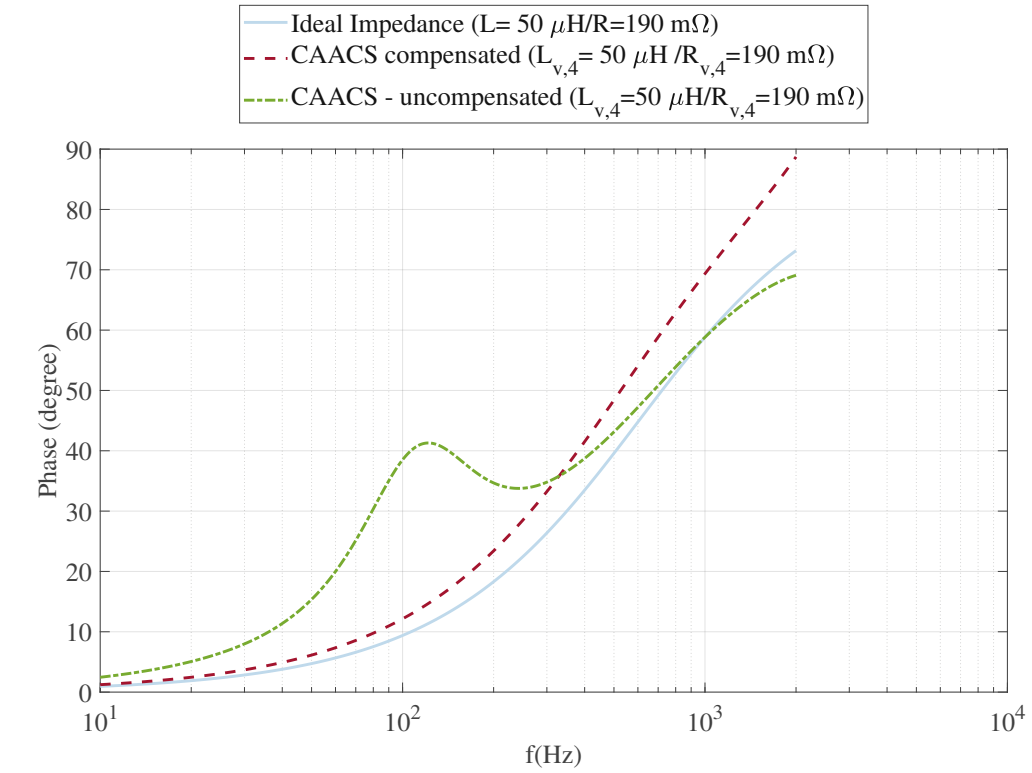


(b)

Figure 4.15: Bode plot of measured compensated and uncompensated output impedance characteristics of three-phase cascaded advanced AC-simulator system with virtual impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 520$ μH (a) Magnitude (Ω) (b) Phase (degree)



(a)



(b)

Figure 4.16: Bode plot of measured compensated and uncompensated output impedance characteristics of three-phase cascaded advanced AC-simulator system with virtual impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 50$ μH (a) Magnitude (Ω) (b) Phase (degree)

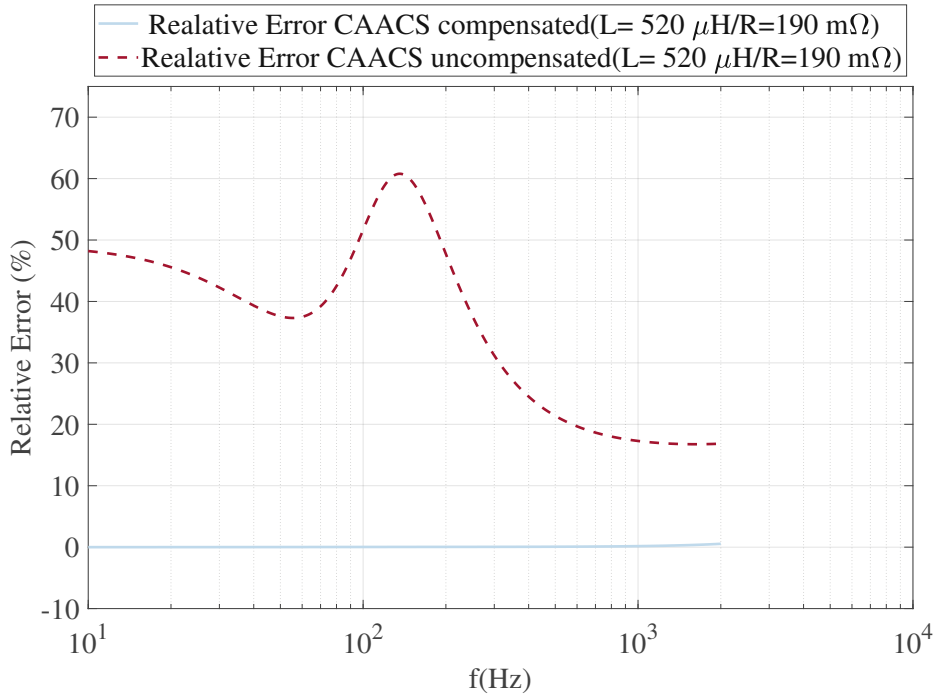


Figure 4.17: Relative error of the measured compensated and uncompensated output impedance characteristics of three-phase cascaded advanced AC-simulator system with virtual impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 520$ μH.

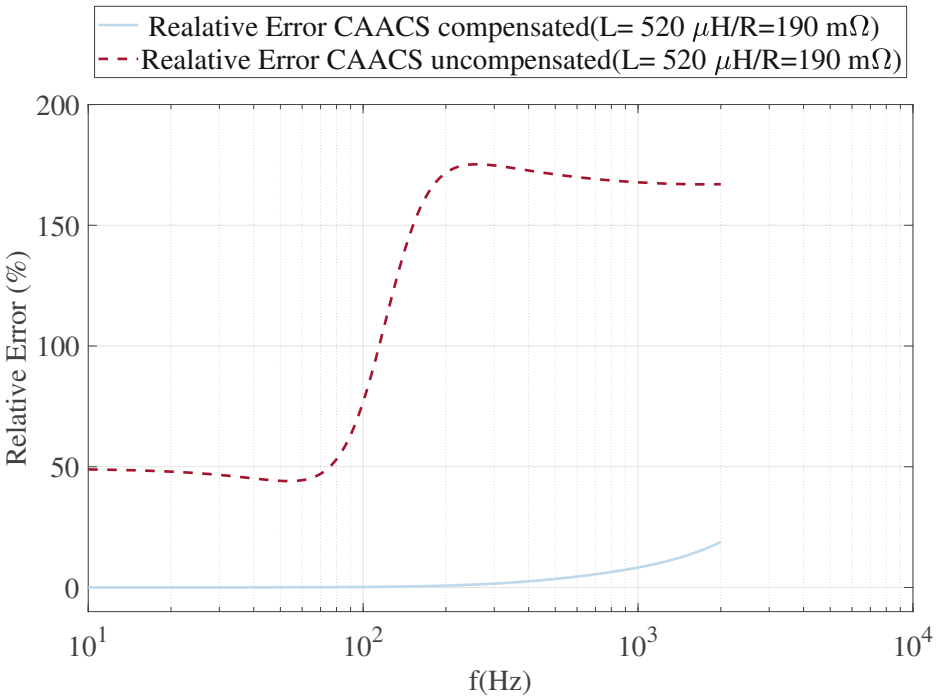


Figure 4.18: Relative error of the measured compensated and uncompensated output impedance characteristics of three-phase cascaded advanced AC-simulator system with virtual impedance values of $R_{v,1} = 190$ mΩ, $L_{v,1} = 50$ μH.

4.3 Non Linear Load Operation

4.3.1 Inverter Current Slew Rate

For an extended validation of the CAACS, the operation mode with non-linear loads is analysed. Non-linear loads are generating harmonic distortions in the spectrum of the output current, which has to be handled by the CAACS. According to section 1.2, requirements of the relevant standards have to be fulfilled. Especially the EN 61000-3-3 electromagnetic compatibility requires the measurement of higher order harmonic currents (up the 40^{th} harmonics), which results in the specification of the small-signal bandwidth $f_{\mathrm{bw}} = 2$ kHz. Therefore, the spectrum up to 2 kHz of the output current of the CAACS is analysed with non-linear loads. The dynamic response of the total system assembly is limited by the characteristics of the LC output filters and therefore the maximum current slew rates has to be determined. The current slew rate of a voltage source inverter can be approximated by

$$\frac{di_{out}(t)}{dt} \cong \frac{1}{L_f}\frac{V_{\mathrm{DC,SSI}}}{2}(1 - \underbrace{m(t)}_{\frac{v_{\mathrm{out,SSI}}(t)}{\frac{V_{\mathrm{DC,SSI}}}{2}}}). \tag{4.13}$$

It must be noted, that only the limitations of the inverter topology are considered and the control method is not taken into account. For the determination of the maximum current slew rate of the small-signal inverter a filter inductance of $L_{\mathrm{f,ss}} = 180\ \mu$H, a DC-link voltage of $V_{\mathrm{DC,SSI}} = 100$ V and a minimum modulation index $m_{\mathrm{min}} = \frac{1}{2} - \frac{\hat{V}_{\mathrm{out,LN,max}}}{V_{\mathrm{DC,SSI}}} = 0.1$ are assumed and thus results in

$$\frac{di_{\mathrm{out,max,SSI}}}{dt} = \frac{1}{L_{\mathrm{f,SSI}}}\frac{V_{\mathrm{DC,SSI}}}{2}0.9 = 0.25\ \mathrm{A}/\mu\mathrm{s} \tag{4.14}$$

The same approximation can be applied for the large-signal inverter, whereby an inductor value of $L_{\mathrm{f,ls}} = 360\ \mu$H (derived from ACS Regetron analysis) and a DC-link voltage of $V_{\mathrm{DC,LSI}} = 800$ V is used and therefore results in

$$\frac{di_{\mathrm{out,max,ls}}}{dt} = 0.5\ \mathrm{A}/\mu\mathrm{s}. \tag{4.15}$$

According to the above approximations and due to the fact that the small-signal inverter is directly connected to the EUT (see Fig. 3.12), the maximum small-signal inverter slew rate determines ($\frac{di}{dt}$) the dynamic response of the total system. The following two topologies are now compared with respect to their grid-side input current slew rate:

- Passive single-phase bridge rectifier uncontrolled (B2) with output capacitor
- Passive three-phase full-wave bridge rectifier (B6) uncontrolled with output capacitor and DC-side output inductor

4.3.2 Passive Single-Phase Rectifier

Fig. 4.19 shows the topology of a passive single-phase rectifier, with a resistive-inductive grid impedance R_N and L_N. The diode rectifier is followed by an output capacitor C_{DC} in order to reduce the output voltage ripple. However, for the

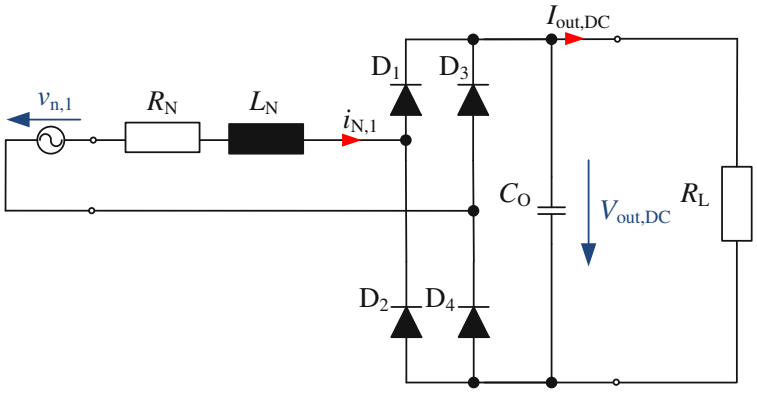


Figure 4.19: Passive single-phase rectifier with output capacitor (B2).

determination of the input current slew rate, the grid-side input current $i_{N,B2}$ has to be analysed. Therefore the topology of a passive single-phase rectifier is simulated and evaluated. However, since with low grid impedance values the current slew rate increases, the values according to Tab. 4.9 has been chosen for the determination of the maximum current slew rate.

Table 4.9: Parameters for the determination of the maximum current slew rate of single-phase rectifier.

Parameter	Value
Grid resistance	$R_N = 190$ mΩ
Grid inductance	$L_N = 50$ μH
Peak grid voltage	$\hat{V}_n = 325$ V
Initial capacitor voltage	$V_{out,dc} = 320$ V
Nominal frequency	$f_n = 50$ Hz
Output capacitor	$C_{DC} = 4700$ μF
Load Resistor	$R_L = 29.96$ Ω

Fig. 4.20 illustrates the simulation results of the single-phase rectifier.

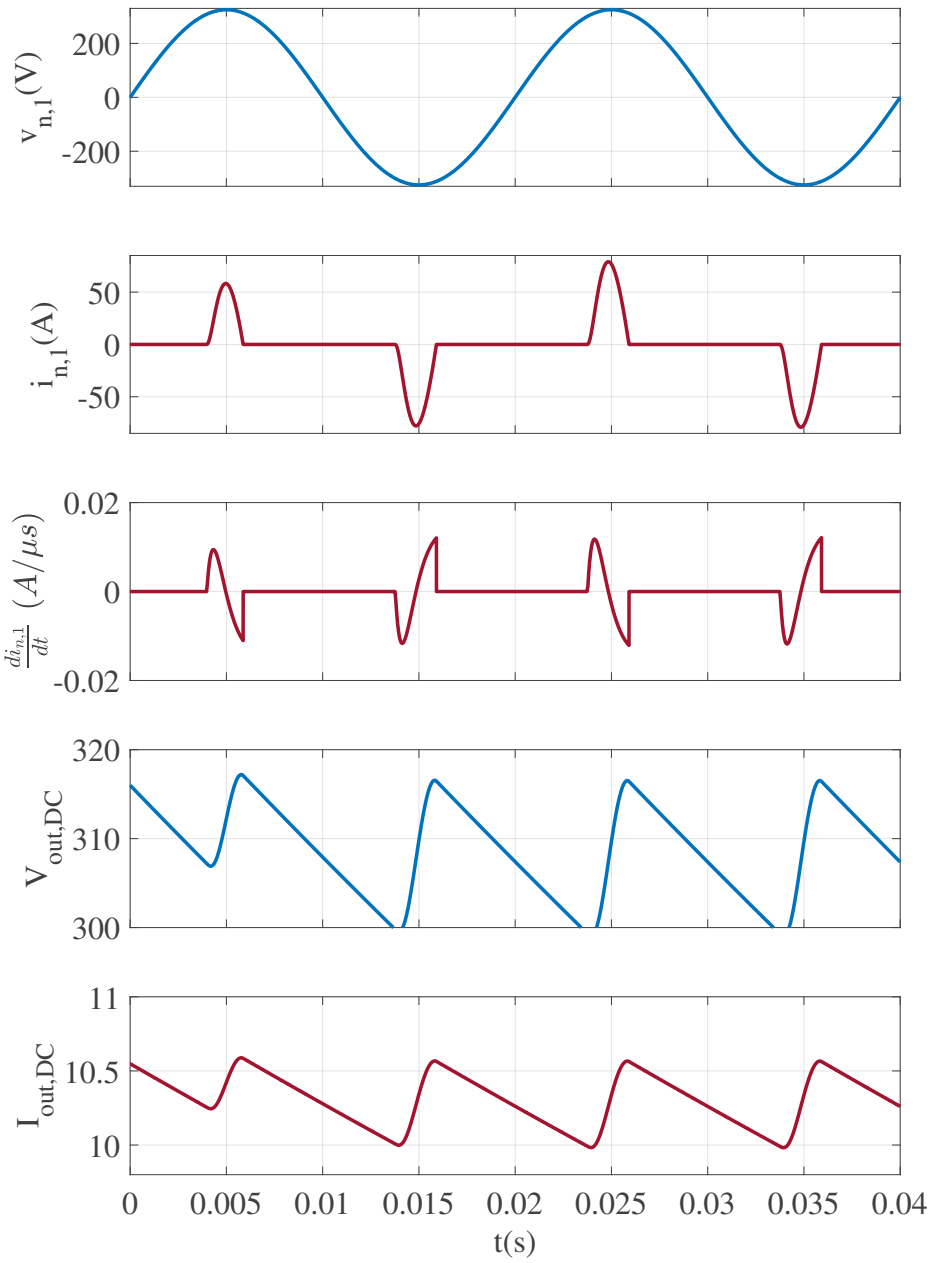


Figure 4.20: Simulation results of the single-phase rectifier (Input voltage $v_{\mathrm{n,1}}$, input current $i_{\mathrm{n,1}}$, input current slew rate $\frac{i_{\mathrm{n,1}}}{dt}$, output voltage $V_{\mathrm{out,DC}}$, output current $i_{\mathrm{out,DC}}$).

According to Fig. 4.20 maximum current slew rate of the passive single-phase rectifier results in

$$\frac{di_{\mathrm{B2,max}}}{dt} = 0.121 \text{ A}/\mu\text{s}. \tag{4.16}$$

4.3.3 Passive Three-Phase Rectifier

The passive three-phase rectifier is a widely used topology in industry due to its simplicity, low voltage ripple and high power-handling capability [55]. In Fig. 4.21 the passive three-phase rectifier with DC-side inductor and output capacitor is depicted. The simple topology and robustness are major advantages of the passive three-phase rectifier, however the poor input current quality compared to active rectifiers with power factor correction (PFC) and the corresponding grid perturbation is a serious drawback.

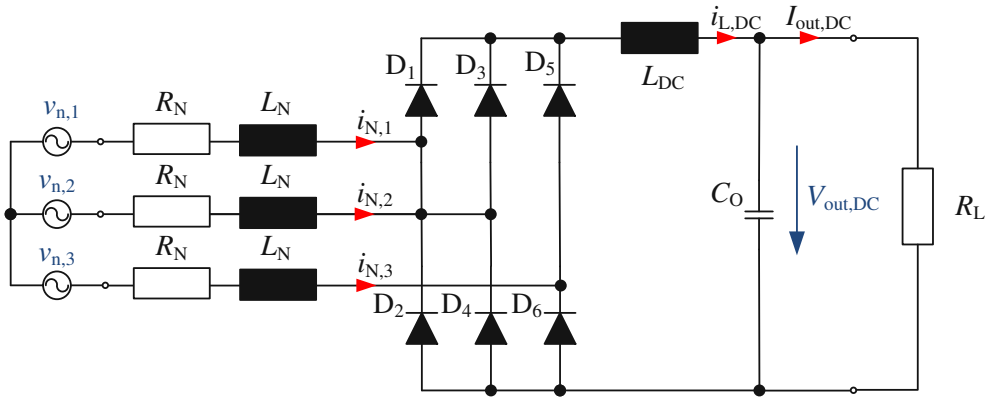


Figure 4.21: Passive three-phase rectifier with DC-side smoothing inductance and output capacitor (B6).

Table 4.10: Parameters for the design of the passive components L_{DC}, C_O and for the determination of the maximum current slew rate of a passive three-phase rectifier.

Parameter	Value
Grid resistance	$R_N = 190$ mΩ
Grid inductance	$L_N = 50$ μH
Peak grid voltage	$\hat{V}_{n,ln} = 325$ V
Output power	$P_o = 10$ kW
Nominal frequency	$f_n = 50$ Hz
Output voltage ripple	$\Delta V_{o,pkpk} = 3.6$ V
Total harmonic distortion	$THD_i = 0.42$
Load Resistor	$R_L = 27.85$ Ω

According to [56] the DC-side smoothing inductor L_{DC} can be calculated by

$$L_{\mathrm{DC}} = \frac{\hat{V}_{\mathrm{n}}^2}{\omega_{\mathrm{n}} P_{\mathrm{o}}} \frac{3}{\pi} \sqrt{\frac{\frac{9}{2} - \left(\frac{54}{35\pi}\right)^2 \left(1 + \mathrm{THD}_i^2\right)}{1 + \mathrm{THD}_i^2 - \left(\frac{\pi}{3}\right)^2}} \left[\sqrt{\left(\frac{\pi}{3}\right)^2 - 1} - \arccos\left(\frac{3}{\pi}\right)\right] \tag{4.17}$$

and the output capacitor C_{O} results in

$$C_{\mathrm{O}} = -\frac{3\sqrt{3}\hat{V}_{\mathrm{n}}}{\pi \omega_{\mathrm{n}}^2 L_{\mathrm{DC}} \Delta V_{\mathrm{o,pkpk}}} \left(\frac{1}{27}\pi^2 + \frac{2}{\sqrt{3}}\pi - 4\right). \tag{4.18}$$

with the dedicated values shown in Tab. 4.10 the passive components for the B6 rectifier are given by $L_{\mathrm{DC}} = 2.2$ mH and $C_{\mathrm{O}} = 4700$ μF.

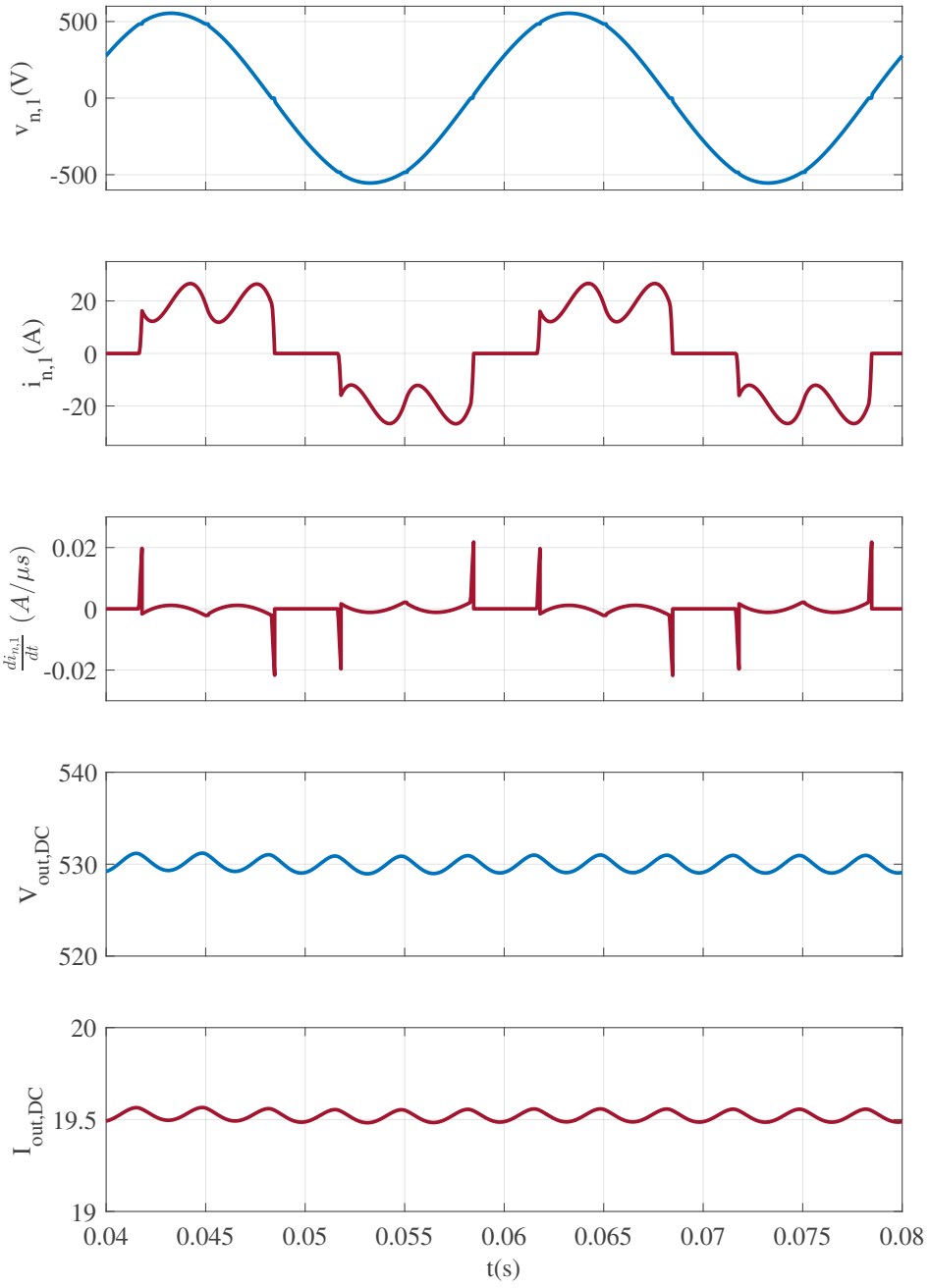


Figure 4.22: Simulation results of the passive three-phase rectifier (Input voltage $v_{\mathrm{n},1}$, input current $i_{\mathrm{n},1}$, input current slew rate $\frac{i_{\mathrm{n},1}}{dt}$, output voltage $V_{\mathrm{out,DC}}$, output current $i_{\mathrm{out,DC}}$).

According to the simulation results depicted in Fig. 4.22 the maximum current slew rate of a passive three-phase rectifier in continuous conduction mode can be assessed to

$$\frac{di_{\mathrm{r,max}}}{dt} = 0.218 \text{ A}/\mu\text{s} \tag{4.19}$$

with the parameters listed in Tab. 4.10

The passive three-phase rectifier is used for further tests due to the higher

current slew rate requirements compared to a passive single-phase rectifier. The laboratory prototype of the passive three-phase rectifier shown in Fig. 4.23, basically consists of an uncontrolled B6 rectifier, a DC-side smoothing inductor, an output capacitor and a discharging resistor.

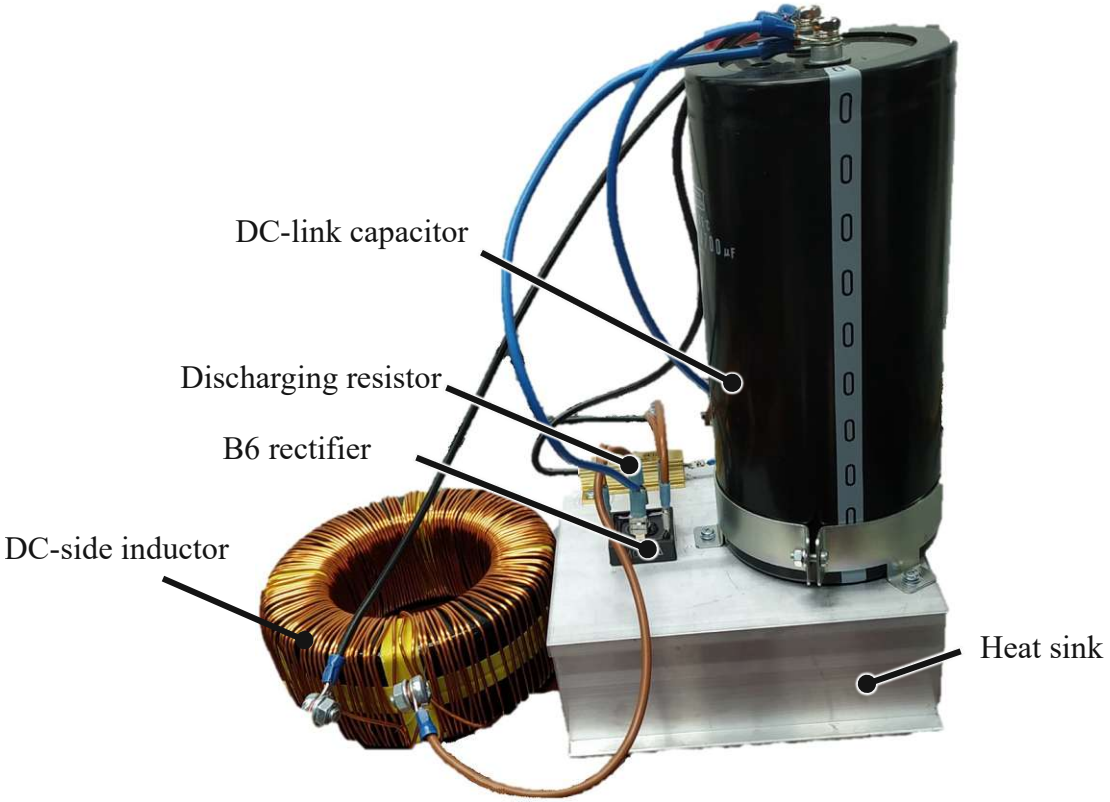


Figure 4.23: Laboratory prototype of the passive three-phase rectifier (B6) for the non-linear load operation of the cascaded advanced AC-simulator.

4.3.4 Time Domain Analysis

Fig. 4.24 shows the test setup for the time domain analysis and the frequency domain analysis, where a passive three-phase rectifier (B6) with a power resistor is used as non-linear load for the cascaded advanced AC-simulator system. The rectifier is operated in continuous conduction mode and with a nominal input voltage of $V_{\mathrm{n,LL}} = 400$ V. In Tab. 4.11 the parameters of the test setup for

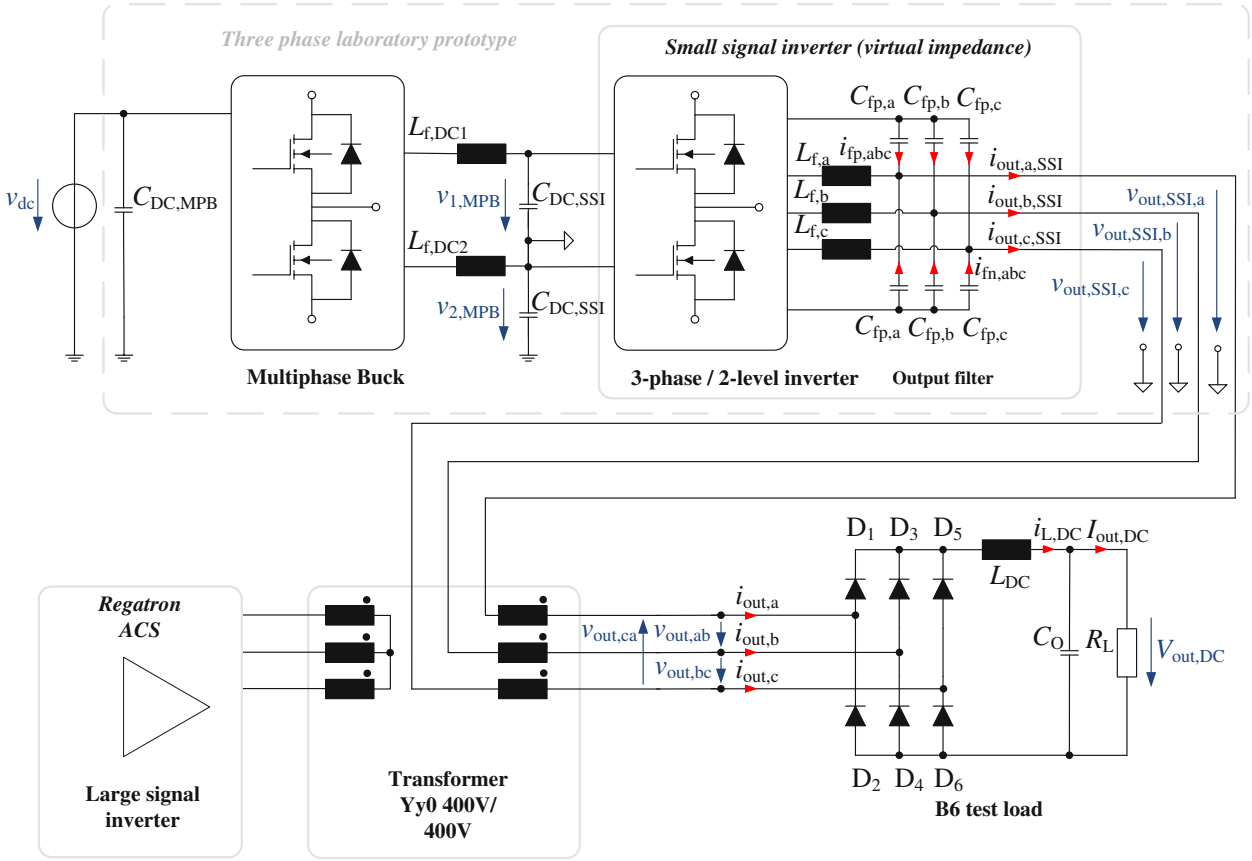


Figure 4.24: Cascaded advanced AC-Simulator system with Regatron ACS (large signal inverter), laboratory small signal prototype and non-linear load (B6) [11].

the cascaded advanced AC-simulator with non-linear load is summarized. Two different virtual grid impedance values are used, to illustrate the impact of the compensation algorithm.

The measurement results of the three-phase output voltage and current of the CAACS with emulated grid impedance values of $R_{\mathrm{N}} = 190$ mΩ and $L_{\mathrm{N}} = 520$ μH including compensation of the large-signal output impedance are shown in Fig. 4.25. The resulting mains current shows the characteristic of the passive three-phase rectifier in continuous inductor current mode with an output current value of $I_{\mathrm{out,a,comp}}(Z_1) = 6.14$ A_{rms}.

For the validation of the total system at non-linear loads, a single phase output current is compared with the current characteristic of an ideal offline simulation, see Fig. 4.26. The measurement is done with enabled compensation of the parasitic inductance of the coupling transformer L_σ and the output impedance of the large-signal inverter. As can be seen, the voltage ($u_{out,ab,comp}(Z_1)$) and current ($i_{out,a,comp}(Z_1)$) characteristic of the measurement coincides with the reference

Table 4.11: Parameters and component values of the experimental setup for the time domain analysis and the frequency domain analysis of the CAACS with non-linear load.

Parameter	Value
Virtual Resistor	$R_{\mathrm{v},1} = R_{\mathrm{v},2} = 190\ \mathrm{m\Omega}$
Virtual Inductor	$L_{\mathrm{v},1} = 520\ \mu\mathrm{H}, L_{\mathrm{v},2} = 50\ \mu\mathrm{H}$
Output capacitor	$C_{\mathrm{DC}} = 4700\ \mu\mathrm{F}$
Output inductor	$L_{\mathrm{DC}} = 2.2\ \mathrm{mH}$
Load Resistor	$R_{\mathrm{L}} = 82\ \Omega$
Output power	$P_{\mathrm{L}} = 3560\ \mathrm{W}$

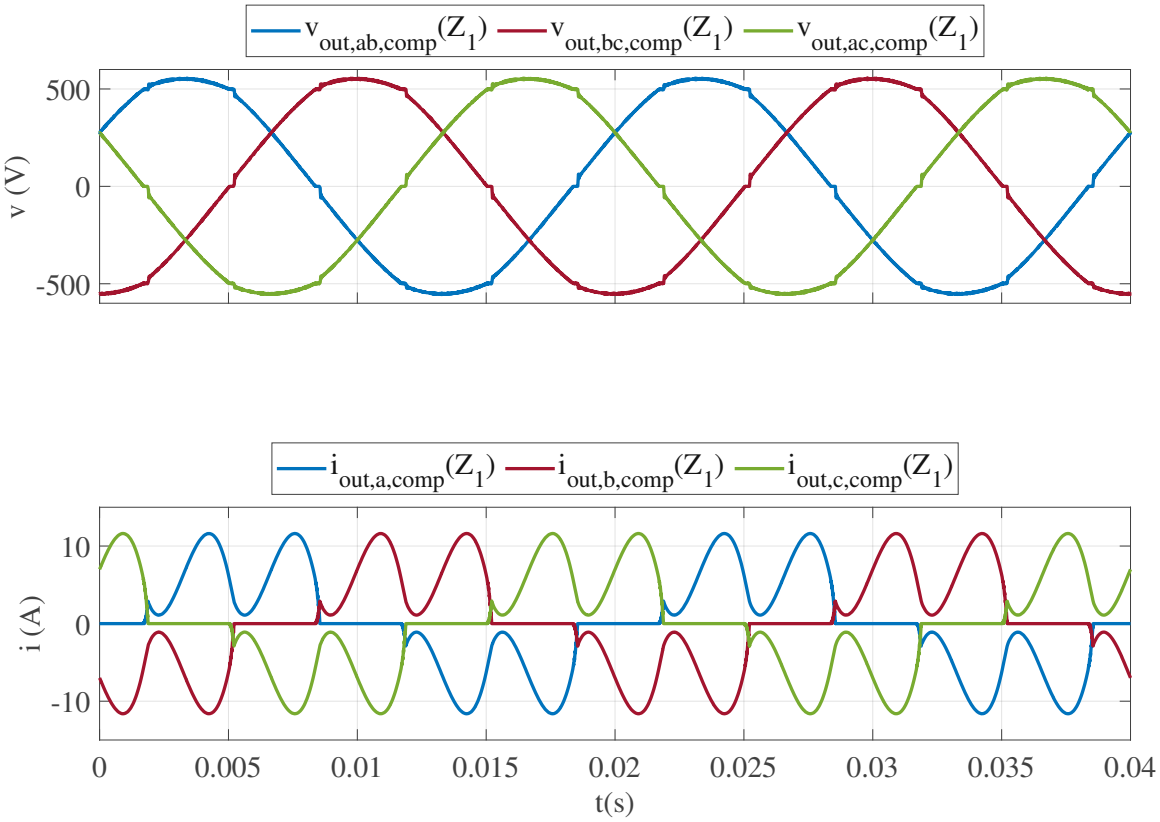


Figure 4.25: Measurement of the three-phase output voltage and three-phase output current of the cascaded advanced AC-Simulator with compensated output impedance, virtual grid impedance ($R_{\mathrm{N}} = 190\ \mathrm{m\Omega}$; $L_{\mathrm{N}} = 520\ \mu\mathrm{H}$) and a passive three-phase rectifier as non-linear load [11].

characteristics ($v_{\mathrm{out,ab,ref}}(Z_1); i_{\mathrm{out,a,ref}}(Z_1)$) of the ideal offline simulation. Fig. 4.27 shows the measurement with disabled compensation of the the output impedance of the large-signal inverter, major deviations can be observed.

The measurement results with emulated grid impedance values of $R_{\mathrm{N}} = 190\ \mathrm{m\Omega}$ and $L_{\mathrm{N}} = 50\ \mu\mathrm{H}$ including compensation of the large-signal output impedance are depicted in Fig. 4.28. Only the voltage measurement shows minor deviations compared to the ideal offline simulation. With disabled compensation of the output impedance of the large-signal inverter, larger deviations between measurement and

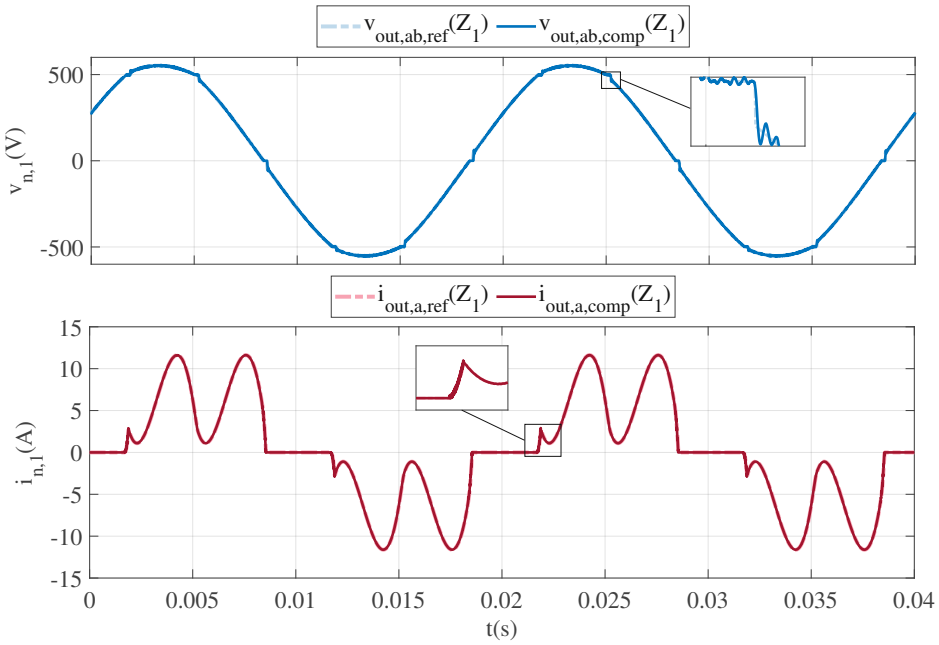


Figure 4.26: Measurement of a single phase output voltage and output current of the cascaded advanced AC-Simulator with compensated output impedance and virtual grid impedance ($R_N = 190$ mΩ; $L_N = 520$ μH) compared with an ideal offline simulation.

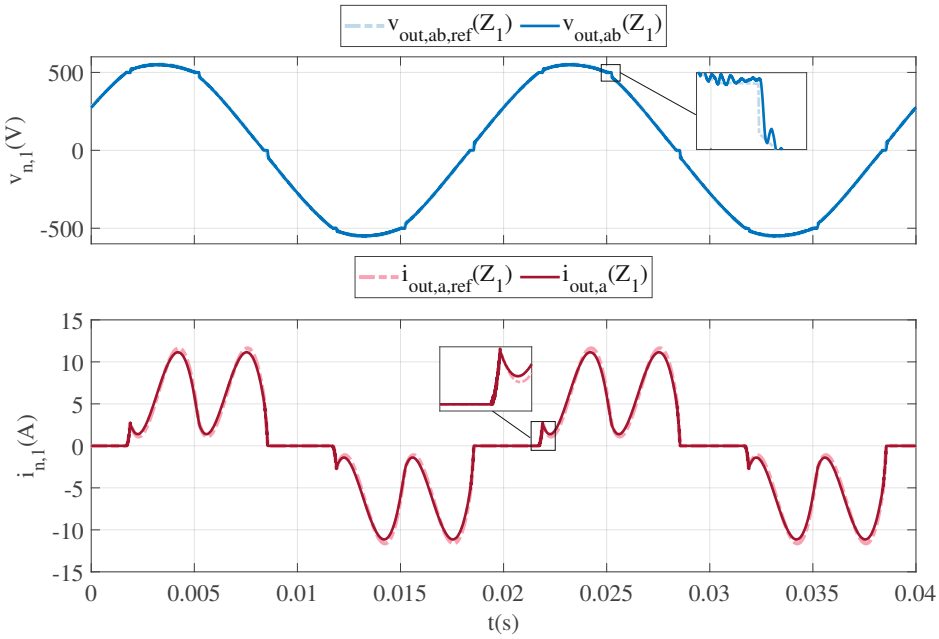


Figure 4.27: Measurement of a single phase output voltage and output current of the cascaded advanced AC-Simulator without compensated output impedance and virtual grid impedance ($R_N = 190$ mΩ; $L_N = 520$ μH) compared with an ideal offline simulation.

ideal simulation occur again illustrated in Fig. 4.29.

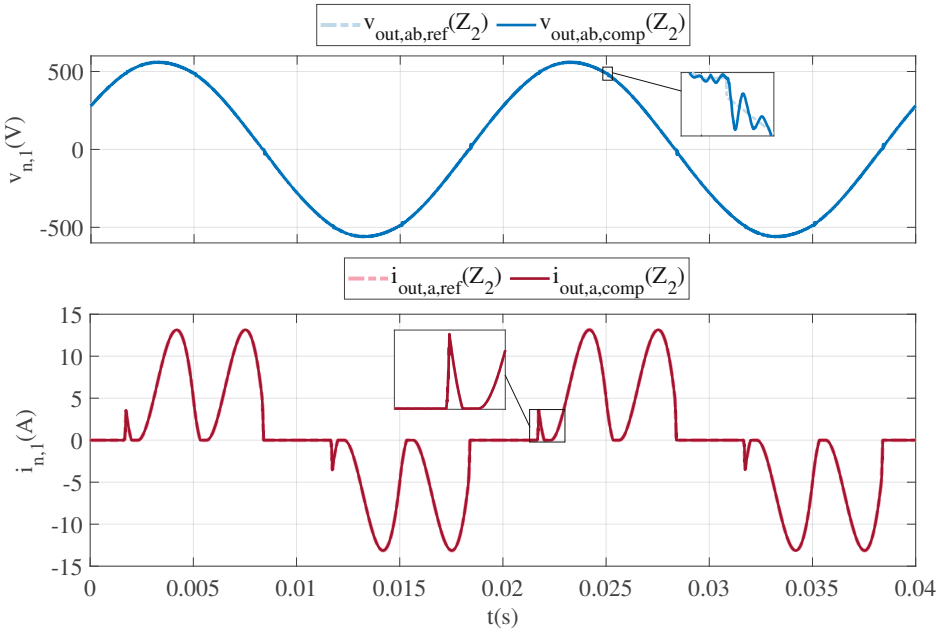


Figure 4.28: Measurement of a single phase output voltage and output current of the cascaded advanced AC-Simulator with compensated output impedance and virtual grid impedance (R_N = 190 mΩ; L_N = 50 μH) compared with an ideal offline simulation.

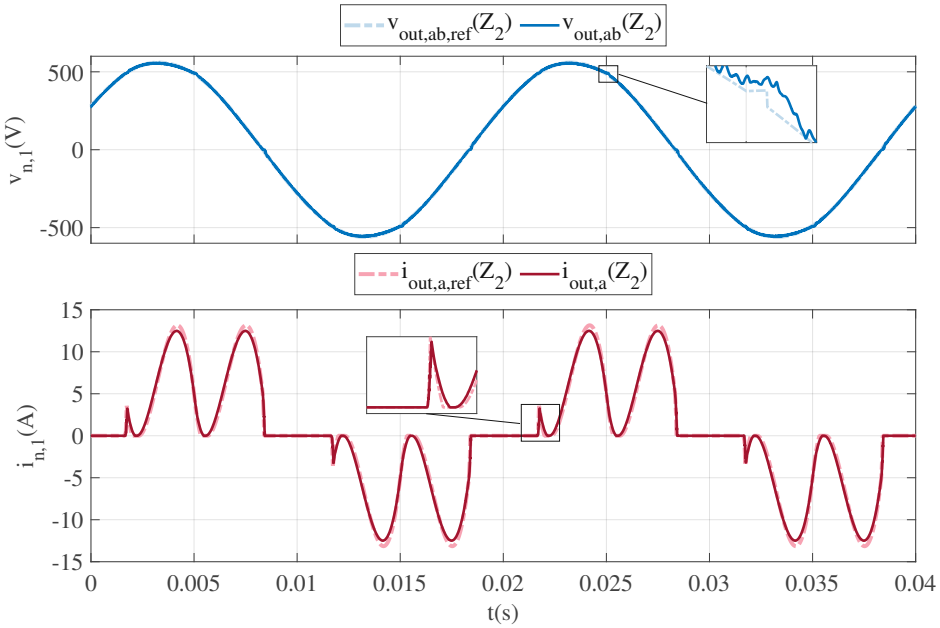


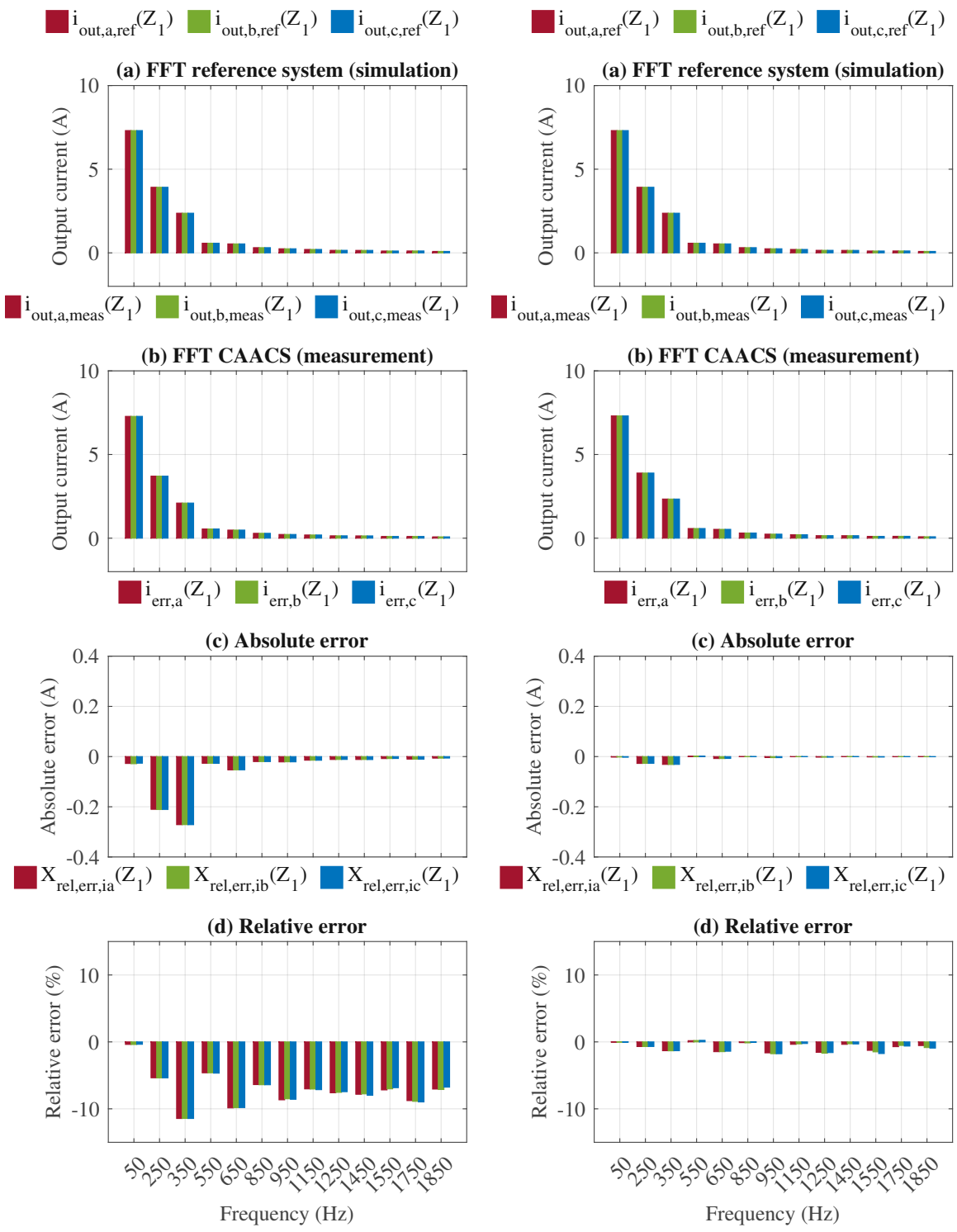
Figure 4.29: Measurement of a single phase output voltage and output current of the cascaded advanced AC-Simulator without compensated output impedance and virtual grid impedance (R_N = 190 mΩ; L_N = 50 μH) compared with an ideal offline simulation.

4.3.5 Frequency Domain Analysis

For the frequency domain analysis the measured current and the simulated current are processed with a Fast Fourier Transformation (FFT) and evaluated at relevant harmonic frequencies. Furthermore, the relative error is calculated for each harmonic frequency in order to determine the deviation between the ideal system and the measured results of the cascaded advanced AC-simulator. The relative error is given by

$$X_{\mathrm{rel,err},I} = \frac{I_{n,\mathrm{ref}} - I_{n,\mathrm{meas}}}{I_{n,\mathrm{ref}}} \tag{4.20}$$

where $I_{n,\mathrm{ref}}$ denotes the simulated reference current and $I_{n,\mathrm{meas}}$ denotes the measured current of the cascaded advanced AC-simulator. Fig. 4.30 illustrates the comparison between the current of a simulated ideal AC-source with grid impedance and the measurement results of the cascaded advanced AC-simulator with emulated grid impedance with the dedicated values $R_{\mathrm{N}} = 190$ mΩ and $L_{\mathrm{N}} = 520$ μH. As can be seen in Fig. 4.30(a), the maximum relative error is $-11,45$ % at $f_{\mathrm{h7}} = 350$ Hz with disabled compensation algorithm. The relative error is showing almost negative values, which corresponds to a higher output impedance compared to the ideal AC-source. These deviations are mainly caused by the output impedance of the large signal inverter. It has to be noted, that the amplitude of the fundamental frequency and the fifth and the seventh harmonic are showing significant current values.



(a) Disabled compensation algorithm (b) Enabled compensation algorithm

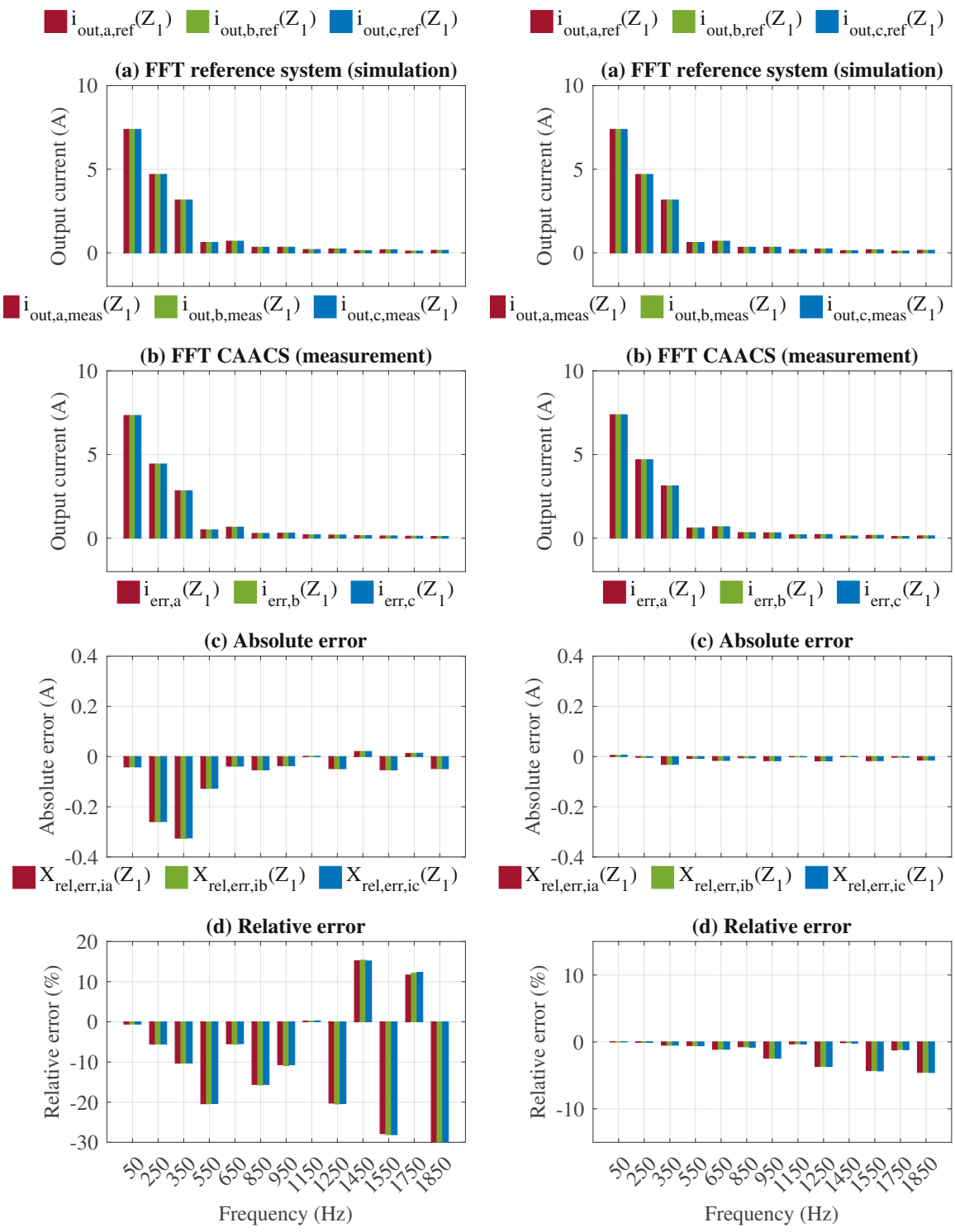
Figure 4.30: FFT analysis of output current (R_N = 190 mΩ; L_N = 520 μH) (a) Ideal three-phase system with grid impedance (offline simulation) (b) Cascaded advanced AC-Simulator output with virtual grid impedance (c) Absolute error of ideal system and advanced AC-simulator system (d) Relative error of ideal system and advanced AC-simulator system.

As shown in 4.30 (b), these deviations/errors can be significantly reduced with enabled output impedance compensation for the large signal inverter, whereby the small-signal inverter now also compensates the output impedance of the large-signal inverter (Regatron ACS) and the coupling transformer by feed-forward control. The maximum relative error can be reduced to -1.34 % for the seventh order harmonic compared to $-11,45$ % without compensation (see Tab. 4.12). Thus it can be observed that an enabled compensation algorithm of critical parasitics within the large signal device comes with significant improvements over the whole current spectrum especially for the fifth order harmonic and the seventh order harmonic.

Table 4.12: Comparison of the relative output current error ($R_{\mathrm{N}} = 190$ mΩ; $L_{\mathrm{N}} = 520$ μH) with enabled and disabled compensation algorithm.

Frequency	$X_{\mathrm{rel,err,ia}}$	$X_{\mathrm{rel,err,ib}}$	$X_{\mathrm{rel,err,ic}}$	$X_{\mathrm{rel,err,ia,comp}}$	$X_{\mathrm{rel,err,ib,comp}}$	$X_{\mathrm{rel,err,ic,comp}}$
50 Hz	-0.38 %	-0.39 %	-0.36 %	-0.03 %	-0.03 %	-0.04 %
250 Hz	-5.36 %	-5.38 %	-5.37 %	-0.7 %	-0.7 %	-0.69 %
350 Hz	-11.45 %	-11.44 %	-11.45 %	-1.32 %	-1.34 %	-1.32 %
550 Hz	-4.62 %	-4.62 %	-4.67 %	0.19 %	0.21 %	0.24 %
650 Hz	-9.86 %	-9.82 %	-9.82 %	-1.46 %	-1.46 %	-1.39 %
850 Hz	-6.38 %	-6.4 %	-6.41 %	-0.11 %	-0.14 %	-0.06 %
950 Hz	-8.66 %	-8.5 %	-8.58 %	-1.64 %	-1.77 %	-1.77 %
1150 Hz	-7.03 %	-7.05 %	-7.14 %	-0.37 %	-0.29 %	-0.24 %
1250 Hz	-7.6 %	-7.54 %	-7.44 %	-1.56 %	-1.69 %	-1.6 %
1450 Hz	-7.82 %	-7.77 %	-7.98 %	-0.37 %	-0.28 %	-0.31 %
1550 Hz	-7.18 %	-7.02 %	-6.84 %	-1.27 %	-1.49 %	-1.74 %
1750 Hz	-8.78 %	-8.89 %	-8.97 %	-0.72 %	-0.53 %	-0.62 %
1850 Hz	-7.05 %	-7.12 %	-6.76 %	-0.55 %	-0.85 %	-0.93 %

The output impedance of the large-signal inverter and coupling transformer affect the emulation of small virtual grid impedance values much more than for large grid impedance values. Therefore the virtual inductor value now is reduced to $L_{\mathrm{N}} = 50$ μH, in order to validate the concept. Fig. 4.31 (a) shows the comparison between the FFT of the output current of a simulated ideal reference system and the cascaded advanced AC-simulator with reduced inductance and without output impedance compensation. The maximum relative error occurs at $f_{\mathrm{h37}} = 1850$ Hz with -31.5 %!



(a) Disabled compensation algorithm

(b) Enabled compensation algorithm

Figure 4.31: FFT analysis of the output current ($R_N = 190$ mΩ; $L_N = 50$ μH) (a) Ideal three-phase system with grid impedance (offline simulation) (b) Cascaded advanced AC-Simulator output with virtual grid impedance (c) Absolute error of ideal system and advanced AC-simulator system (d) Relative error of ideal system and advanced AC-simulator system.

As can be seen the relative error is increased significantly for this test case with the small grid impedance value. The result can be considerably improved with enabled compensation algorithm (see Fig. 4.31 (b)). According to Tab. 4.13 the maximum relative error is improved to a maximum value of 5 % with enabled output impedance compensation.

Table 4.13: Comparison of the relative output current error ($R_N = 190$ mΩ; $L_N = 50$ μH) with enabled and disabled compensation algorithm.

Frequency	$X_{rel,err,ia}$	$X_{rel,err,ib}$	$X_{rel,err,ic}$	$X_{rel,err,ia,comp}$	$X_{rel,err,ib,comp}$	$X_{rel,err,ic,comp}$
50 Hz	$-0,55$ %	$-0,56$ %	$-0,36$ %	$0,03$ %	$0,03$ %	$0,04$ %
250 Hz	$-5,53$ %	$-5,52$ %	$-5,37$ %	$-0,03$ %	$-0,04$ %	$-0,03$ %
350 Hz	$-10,31$ %	$-10,25$ %	$-11,45$ %	$-0,5$ %	$-0,5$ %	$-0,49$ %
550 Hz	$-20,4$ %	$-20,35$ %	$-4,67$ %	$-0,55$ %	$-0,57$ %	$-0,57$ %
650 Hz	$-5,55$ %	$-5,44$ %	$-9,82$ %	$-1,11$ %	$-1,08$ %	$-1,1$ %
850 Hz	$-15,72$ %	$-15,58$ %	$-6,41$ %	$-0,73$ %	$-0,75$ %	$-0,8$ %
950 Hz	$-10,94$ %	$-10,69$ %	$-8,58$ %	$-2,42$ %	$-2,42$ %	$-2,43$ %
1150 Hz	$0,17$ %	$0,25$ %	$-7,14$ %	$-0,3$ %	$-0,27$ %	$-0,33$ %
1250 Hz	$-20,46$ %	$-20,36$ %	$-7,44$ %	$-3,67$ %	$-3,64$ %	$-3,67$ %
1450 Hz	$15,35$ %	$15,15$ %	$-7,98$ %	$-0,12$ %	$-0,1$ %	$-0,19$ %
1550 Hz	$-28,09$ %	$-28,09$ %	$-6,84$ %	$-4,29$ %	$-4,3$ %	$-4,33$ %
1750 Hz	$12,17$ %	$12,32$ %	$-8,97$ %	$-1,21$ %	$-1,13$ %	$-1,17$ %
1850 Hz	$-31,37$ %	$-31,27$ %	$-6,76$ %	$-4,56$ %	$-4,54$ %	$-4,57$ %

Chapter 5

Summary - Outlook

In this thesis, the analysis and verification of an advanced AC-Simulator (AACS) with virtual output impedance emulation has been addressed. A main application for AC/grid simulating power sources with defined output impedances is the test of grid-connected converters like solar inverters, active rectifiers, static VAr compensators etc. Conventional AC-simulator setups with output/grid impedance emulation usually are based on active power sources (amplifiers) with passive (R/L) impedance components. Such systems are simple and robust, but they suffer from higher investment cost, additional electrical losses during operation and limited flexibility.

The implementation of a virtual impedance emulated by the control system of the power amplifier in contrast avoids the disadvantages mentioned before. Such an impedance "emulation" in principle could be performed by a single-stage power converter topology, i.e., impedance emulation by the main power amplifier. Advantageously, however, a cascaded circuit topology (Cascaded Advanced AC Simulator ... CAACS) resulting in higher dynamic performance is proposed, analytically described and implemented as a laboratory hardware prototype setup in this thesis.

The CAACS basically consist of a large-signal switch-mode power inverter (LSI) providing the fundamental AC output voltage signal and an additional small-signal inverter (SSI) arranged in series to the LSI using a coupling power transformer. The SSI is dedicated mainly to the emulation of the virtual grid impedance. The proposed CAACS has turned out to be a promising approach, because it shows improved measurement accuracy and bandwidth compared to a single-stage topology. However, to achieve accurate measurement results, the output impedance of the LSI as well as the coupling transformer impedance has to be compensated by the SSI, which could be successfully verified and validated within this thesis.

Besides the operation behaviour at standard (ohmic) load, the CAACS prototype, furthermore also the feeding of non-linear load is addressed. For this the characteristics of different diode bridge rectifiers (single-phase B2 and three-phase B6 bridge rectifier) are discussed. The limitations of the bandwidth of the proposed CAACS are also analyzed and verified on the laboratory test setup using a three-phase B6 bridge rectifier. For the validation a FFT of the measured current signal is compared to an idealized reference system under different operation/load conditions. The results demonstrate a significant improvement of the precision of the measurement current harmonics (being relevant to meet the required EMI

regulations of the DUT, e.g., a rectifier or a solar inverter), if the control of the SSI includes also a compensation of the output impedance of the LSI including also the impedance of the coupling transformer. This especially is true for emulating lower virtual impedance values (e.g. 190 mΩ/50 μH). For such rates, by activating the proposed active impedance compensation (LSI output + transformer) the precision of the measured current harmonics in the relevant frequency region up to 2 kHz can be kept < 5 % for most of the harmonics < 1 %...2 %. Without compensation much higher error rates (up to 20 % and even more) would appear, which clearly demonstrates the proper operation of the proposed concept.

For future developments and analyses in especial following points would be of interest: At present the implemented virtual impedance is focused to a resistive-inductive characteristic. It would therefore be of interest to implement other grid impedance topologies. Especially for the emulation of power grids based on power cables the corresponding cabling capacitances have to be considered for the virtual impedance characteristic to be implemented. As the intersection of such a grid impedance and a specific inverter output impedance characteristic might lead to unstable network configurations. The analysis of such grid impedance scenarios (RLC networks) and the extension of virtual impedance characteristic are relevant for future research tasks.

Concerning the power level of research and simulation laboratories, e.g. the AIT SMARTEST is rated up to 850 kVA, a corresponding increase in output power of the CAACS is mandatory. In order to obtain a flexible and expandable system, the operation of multiple CAACS devices arranged in parallel would be a promising approach. However, for the impedance emulation with parallel operated CAACS advanced control strategies might be required and should be analyzed. At the same time the up-scaled System has to fulfill the specifications, especially the required small-signal bandwidth of $f_{\mathrm{bw}} = 2$ kHz.

Pertaining to the compensation of the large-signal inverter output impedance, an extension for different types of large-signal generators should be implemented. Therefore two different approaches can be applied. On one hand the approach based on the existing off-line output impedance measurement can be used and further be developed in order to facilitate the implementation of new impedance characteristics. On the other hand the small-signal inverter can be used to determine the output impedance of the large-signal inverter, including also parasitics of, e.g., the coupling transformer by applying an "on-line" AC-sweep analysis. Such a measurement could be used directly for the impedance compensation.

Finally, the analysis and prototypical implementation of the cascaded advanced AC-simulator based on an isolated dual-active bridge (DAB) may be another promising approach. For such a system no coupling transformer would be needed which may improve also the bandwidth of the large-signal inverter. Therefore, the development of a high-power DAB substituting the buck converters would be mandatory in order to avoid the presently required line-frequency isolation transformer.

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