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Investigation of charge up effects on silicon test structures

Ausgeführt am
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Abstract

The CMS-experiment is one of the large LHC experiments at CERN. As it is continuously running, the detector degrades with time because of the radiation damage of the colliding particles. So the detector has to be renewed around 2023 in the so-called phase II upgrade. For this upgrade, new sensors have to be developed with new technology or materials that exhibit higher radiation hardness, because after the upgrade the luminosity of the LHC shall be increased. The scope of this diploma thesis is the comparison of the process quality of the sensors of different vendors based on the characterisation of test structures. Special emphasis was laid on charge up effects that were examined and also tried to provoke on MOS structures in particular.

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1 CMS-Experiment

The CMS-experiment is one of the four big experiments at the *Large Hardron Collider* (LHC) at CERN[1]. The LHC is a circular particle accelerator with a circumference of 26.7 km, located about 100 m below the earth's surface. It was built to accelerate two proton beams in opposite direction, each with an energy of 7 TeV. When brought to collision, this results in a center-of-mass energy of 14 TeV, which is released and thus available for the creation of (new) particles [2].

The four big experiments[2] at the LHC are ALICE, LHCb, ATLAS and CMS. ALICE is designed to investigate heavy ion collisions (i.e. Pb-nuclei) to search for quark-gluon plasma, a special state of matter that is believed to have dominated the universe in the first fractions of seconds after the Big Bang. It only exists at very high densities, because else quarks and gluons only occur in bound states due to the so-called quark confinement. The LHCb experiment is intended to study the CP-violation[3] observing the decay modes of $B-$mesons (i.e. the $B^0 - \bar{B}^0-$system consisting of $d\bar{b}$ and $\bar{d}b$ quarks, respectively) and to precisely measure the elements of the quark mixing matrix, which describes the mixing angles between the down-type (d, s, b) and up-type (u, c, t) quarks and is also referred to as CKM-matrix[4] [3].

The two experiments ATLAS and CMS have the same goals, but are designed differently and completely independent of each other, so that they can confirm the results of each other and, thus, rule out systematic errors [4]. They are built as general purpose detectors to investigate a wide field of physics, e.g. supersymmetry[5] [2]. A major task of these two experiments was fulfilled on 4 July 2012, when ATLAS and CMS announced that they had each observed a new particle in the mass region around 126 GeV that is consistent with the Higgs boson predicted by the Standard Model[6] [1].

The acronym CMS stands for *Compact Muon Solenoid*, as it lays emphasis on the detection of muons created by the proton-proton-interactions, since they reveal much information about the decay modes. The term *compact* has to be understood in comparison to other detectors of similar weight[7], as it still has a length of 21 m and a diameter of 15 m. The solenoid is superconducting, induces a magnetic field of 4 Tesla and, thus, makes possible the compact design. The functional principle of CMS is the

[1] CERN is the European Organisation for Nuclear Research, located near Geneva, Switzerland. The acronym stands for the former French name *Conseil Européen pour la Recherche Nucléaire* [1].

[2] There are also two smaller experiments called TOTEM and LHCf that shall measure the cross-section of the proton and the number and energies of π^0-mesons produced in the collisions [3].

[3] CP-violation is the violation of the so-called CP-symmetry, a theory, according to which the laws of physics should be the same when a particle is interchanged with its antiparticle (charge conjugation) and its spatial coordinates are inverted (parity).

[4] The three letters are standing for the discoverers Cabibbo, Kobayashi and Maskawa.

[5] Supersymmetry (SUSY) is a theory that postulates a supersymmetric bosonic partner to each fermion and vice versa. Though, these supersymmetric particles are so heavy that they haven't been found yet.

[6] The Higgs boson was proposed by Robert Brout, François Englert and Peter Higgs in 1964, the latter two were awarded with the Nobel prize in physics in 2013 [1].

[7] CMS weights around 12,000 t, while ATLAS, for example, only weights about half of it, but has almost eight times the volume of CMS [2, 3].

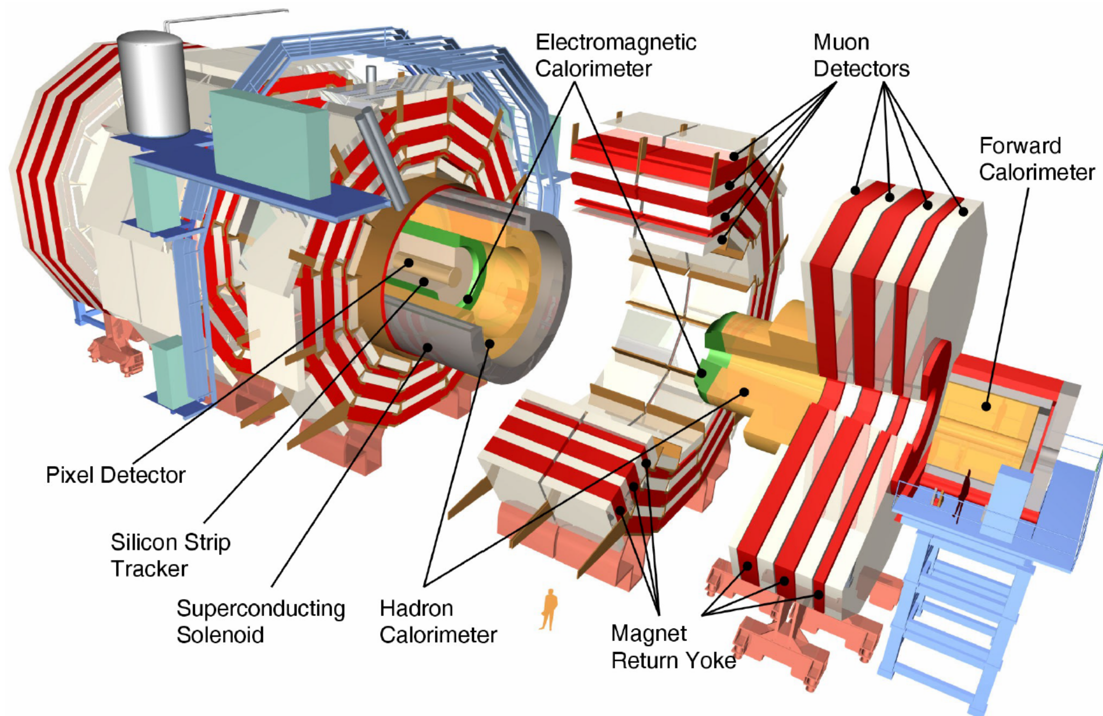


Figure 1: A schematic view of the CMS detector, for comparison the size of a person is shown in front. [2]

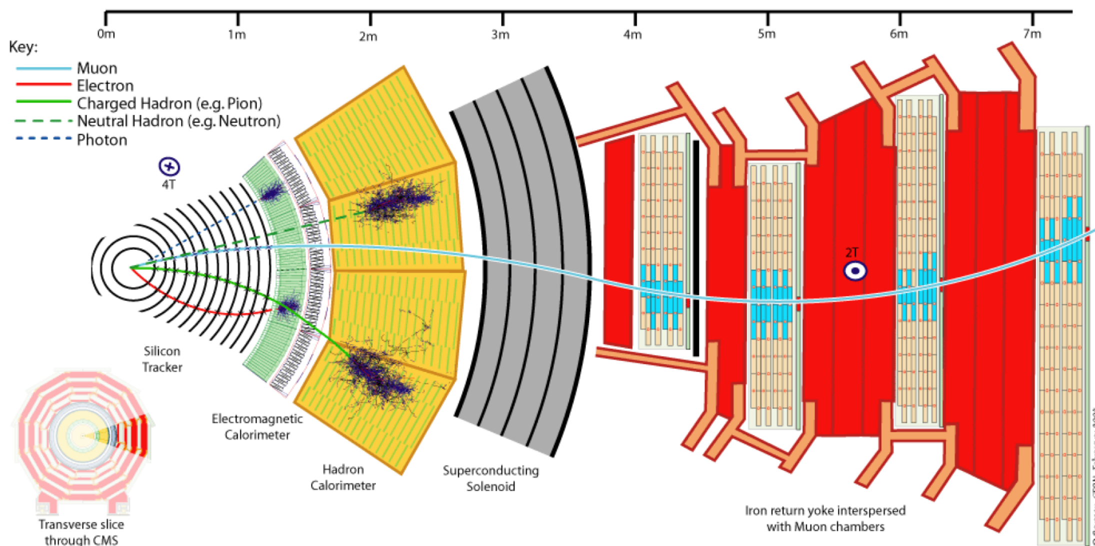


Figure 2: A slice of the CMS detector with the trajectories of different traversing particles and the sections where they are detected. [4]

following: In the magnetic field of the solenoid, charged particles follow spiraling paths and the curvature of this paths reveals the momenta of the particles. The energy of the particles is measured in the calorimeters. The electrons and photons are absorbed by the so-called *electromagnetic calorimeter* (ECAL), as they interact electromagnetically, while hadrons, which are interacting by the strong force, are measured in the *hadronic calorimeter* (HCAL). The muons are detected in the *muon chambers* and only weakly interacting particles, as the neutrinos, are escaping all detectors. Nevertheless, they can be determined by adding up the momenta of all the detected particles and evaluate the missing momentum [5].

The CMS detector is composed of different layers that are arranged onion-like around the interaction point. The innermost part is the so-called *tracker* that utilises silicon pixel (two-dimensional) and silicon strip (one-dimensional) sensors to reconstruct the trajectories of the particles and their interaction point, and thus locate secondary vertices[8]. The next layers are filled with the calorimeters described above, first the ECAL, then the HCAL. Thereafter the solenoid is situated, and outside of it, the muon chambers are located, since muons are likely to traverse the whole detector. In figure 1 a schematic view of the whole CMS detector is displayed. Figure 2 shows a slice of the detector with different traversing particles and in which part of it they are detected [3].

In the LHC, every 25 ns two bunches of protons collide. This corresponds to an interaction frequency of $f = 40\,\text{MHz}$ and results in a luminosity of $10^{34}\,\text{cm}^{-2}\text{s}^{-1}$. The luminosity $\mathcal{L}$ describes the probability of an interaction of two colliding particle bunches

[8]Secondary vertices occur when very short-lived particles decay into other (lighter) particles before they reach the detector.

and can be calculated by

$$\mathcal{L} = f \frac{n^2}{4\pi\sigma_x\sigma_y} \tag{1}$$

where n is the number of particles of each bunch and σ_x and σ_y characterise the beam spreads in horizontal and vertical directions. This value is, beside the center-of-mass energy, the most important parameter characterising a collider and shall be increased by a factor of 5 after the so-called *phase II upgrade* in 2025 [2].

1.1 Phase II upgrade

The increased luminosity of the so-called *high luminosity LHC* (HL-LHC) corresponds to more interactions and leads to a higher track density. This can be measured with the so-called *pile-up*, the number of events produced at one beam crossing. The pile-up shall be increased to 140 interactions per beam crossing after the phase II upgrade.

To deal with this increase, the tracker will grow in granularity. This will be realised by more implemented silicon sensors, shorter strips in the outer tracker and more layers of pixel sensors in the inner tracker.

Another advantage is the reduction of material in the tracker volume, what improves the particle detection.

However, a higher luminosity also means higher radiation, which primary affects the tracker, as this is the innermost detector. Therefore, a more radiation-hard material is needed and so the new tracker shall be built of silicon sensors in p-type bulk and n-type implant [6].

The functional principle of silicon sensors is explained in the following section.

2 Semiconductor detectors

Initially, it was planned to use Micro-Strip Gas Chambers for the CMS tracker, however, silicon detectors are more practical due to their advantages like a higher radiation tolerance, a low mean ionisation energy and a fast signal response [7].

2.1 Semiconductor theory

In a crystal lattice, there are so many atoms that the energy states form almost continuous energy bands. Nevertheless, there are empty energy intervals that can not be occupied by electrons and, thus, are called *energy band gaps* E_g. The uppermost entirely filled energy band is called *valence band* and the lowermost empty or partly filled band is called *conduction band*. Solids can be classified by these energy band gaps into conductors, where conduction and valence band are overlapping and electrons can be exited to higher energy levels with only small amounts of energy, semiconductors, which have a clear but small energy gap (e.g. for silicon it is 1.12 eV) and insulators, where the band gap is large ($E_\mathrm{g} \gtrsim 5\,\mathrm{eV}$), so that it is unlikely that electrons are excited from the valence band to the conduction band (see fig. 3) [4, 2].

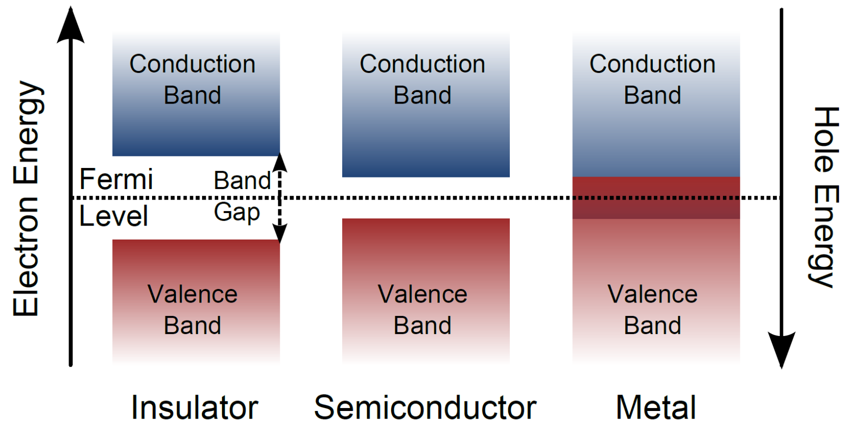


Figure 3: Energy band structure of solids classified by the energy band gap E_g into insulators, semiconductors and conductors (metals) [4].

There are semiconductors like silicon that have an *indirect band gap*, which means that the minimum energy in the conduction band is shifted to the maximum in the valence band by a $\vec{k}-$vector in momentum space (see fig. 4). Thus, to conserve the momentum, an electron needs some source of momentum to fall from the conduction band into the valence band. However, in a semiconductor with *direct band gap* like germanium or gallium arsenide, electrons at the conduction band edge can combine directly with holes at the valence band edge. As the energy from this recombination process will be emitted as light, this is called spontaneous emission [2].

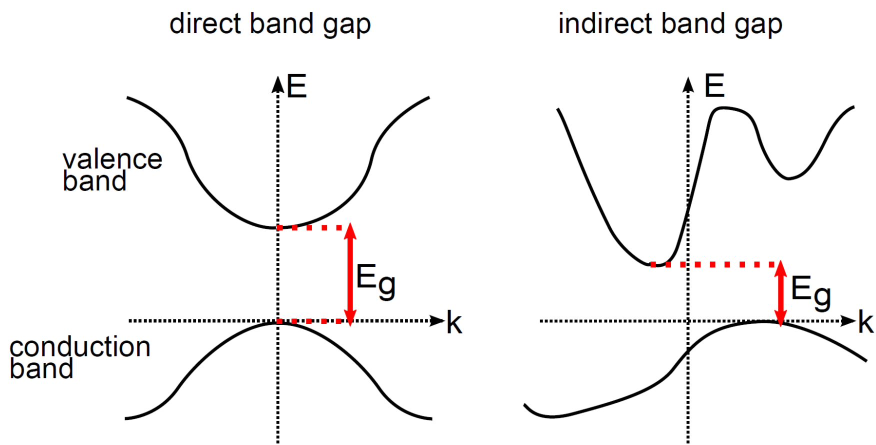


Figure 4: Energy diagram in momentum space for a semiconductor with direct (left) and indirect (right) band gap [4].

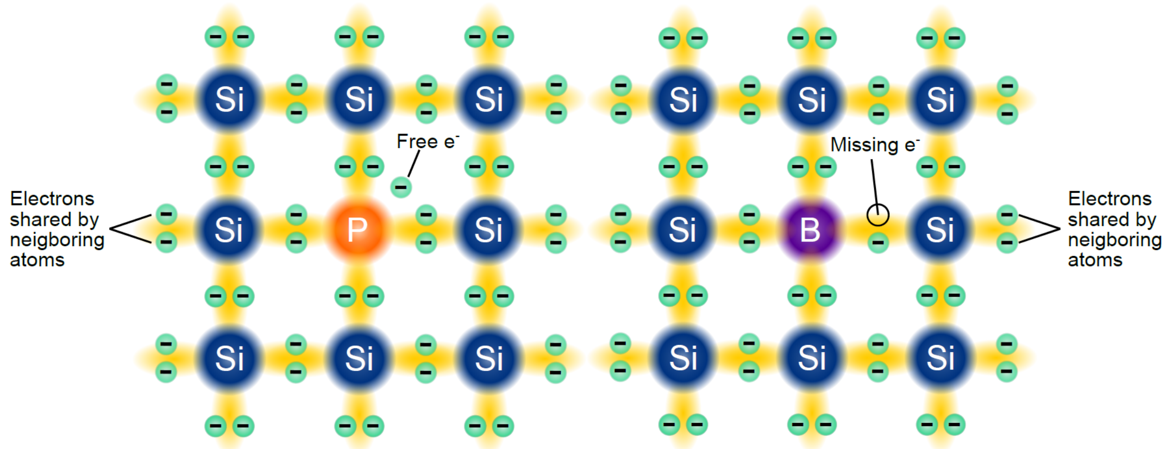


Figure 5: Silicon lattice doped with phosphorus (P) forming an n-type material (left) and with boron (B) forming a p-type material (right side) [4].

By introducing a small amount[9] of impurity atoms into an intrinsic semiconductor, one can modify its energy band configuration and affect its electrical properties. This process is called doping and there are two types, affecting the electrical properties differently, depending on the doping material and its position in the periodic table of the elements. Donors are elements from the fifth main group of the periodic table that add some energy states below, but very close to the conduction band, when incorporated into the crystal lattice of the semiconductor crystal. They provide weakly-bound valence electrons to the material, creating excessive negative charge carriers and, thus, this material is called *n-type*. A typical element used for n-type doping is phosphorus (P), seen on the left side of fig. 5. Acceptors are elements with three valence electrons that introduce energy states closely above the valence band, when incorporated into the crystal lattice. The missing negative electron in the lattice, called *hole*, acts like a positive charge and, thus, this material is called *p-type*. A typical element used for p-type doping is boron (B), seen on the right side of fig. 5. For silicon with boron doping, the energy gap between the introduced energy states and the conduction band edge is reduced to only 0.045 eV [2].

The doping of a semiconductor shifts the Fermi energy E_{F} towards the corresponding band edge, for donors to the conduction band and for acceptors to the valence band (see fig. 6). So, when two differently doped materials are brought into contact with each other (e.g. a *pn-junction*), the energy bands are bending, because the Fermi level must remain constant in a system in thermodynamic equilibrium. This leads to many useful electrical properties, also described in section 3 in more detail (e.g. sec. 3.2, fig. 11) [2].

[9] 1 atom per 10^6 atoms of silicon [4].

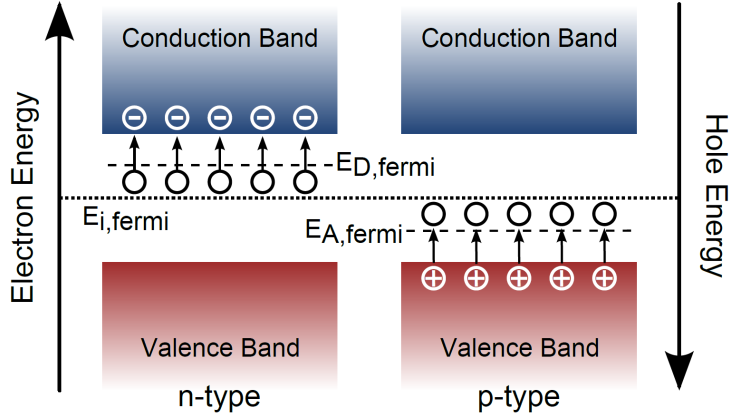


Figure 6: Energy band structure for semiconductors doped with donors (left) and acceptors (right side) and the shift of the corresponding Fermi levels $E_{\mathrm{D,fermi}}$ and $E_{\mathrm{A,fermi}}$ towards the conduction band (n-type) and the valence band (p-type), respectively [4].

2.2 Silicon sensors as particle detectors

For a silicon sensor, as it is used in the current tracker of the CMS experiment, a very lowly doped silicon n-bulk is used as substrate. A thin, highly doped p^+-region (p^+-implant) on this n-substrate forms a large-area pn-junction. (This holds for so-called *p-in-n* sensors, though, in the phase II upgrade of the tracker, there shall be used p-substrate and n^+-implant. However, this is more complex since it needs additional implantations[10] and goes beyond the scope of this thesis, as it is not yet fully developed.) A detector is utilised like a diode operated in reverse direction. Therefore, a reverse bias voltage is applied between the p^+-implant and the back side of the substrate which is highly doped n^+ to ensure good ohmic contact to the aluminium backplane. This bias voltage depletes the bulk from free charge carriers and a so-called *space charge region* (SCR) forms, starting from the p^+-implant. When a particle is traversing the sensor now, it creates electron-hole-pairs along its track, similar to the ionisation of gas, while loosing energy. Due to the applied voltage, the electron-hole-pairs are separated, the electrons move to the p^+-implant and the holes to the n^+-backplane. This drift is detected as electrical signal.

2.2.1 Silicon strip sensors

To achieve a spatial resolution, the p^+-implant is segmented into strips or pixels. So by differentiating the implant-segment where a signal is detected, one obtains a one- (strips) or two-dimensional (pixels) spatial resolution of the particles track. In figure 7 a schematic cross section of an n-bulk silicon strip detector is shown. Here one can also see that the readout of the signal is coupled capacitively from the implant-strips via a

[10] So-called *p-stop* implantations or *p-spray* to ensure strip separation.

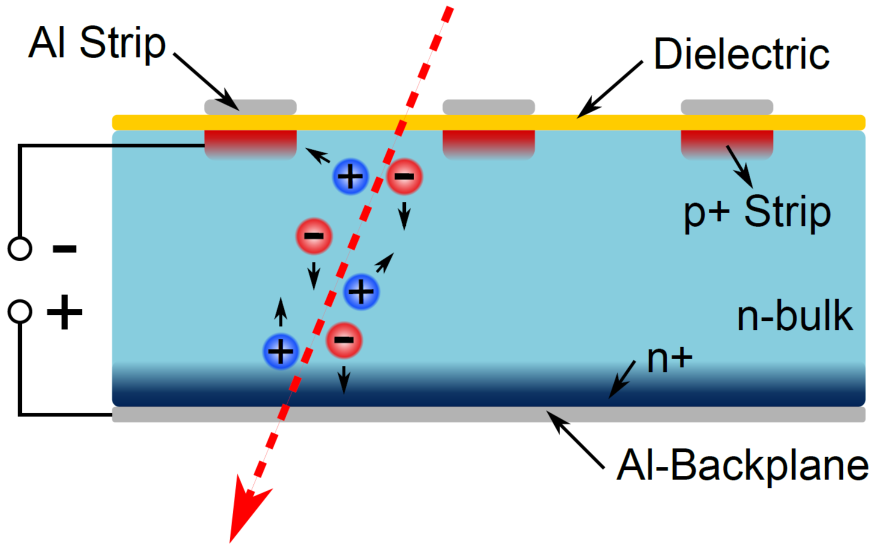


Figure 7: Schematic cross section of an n-bulk silicon strip detector with a traversing particle (red dashed arrow) producing electron-hole-pairs [4].

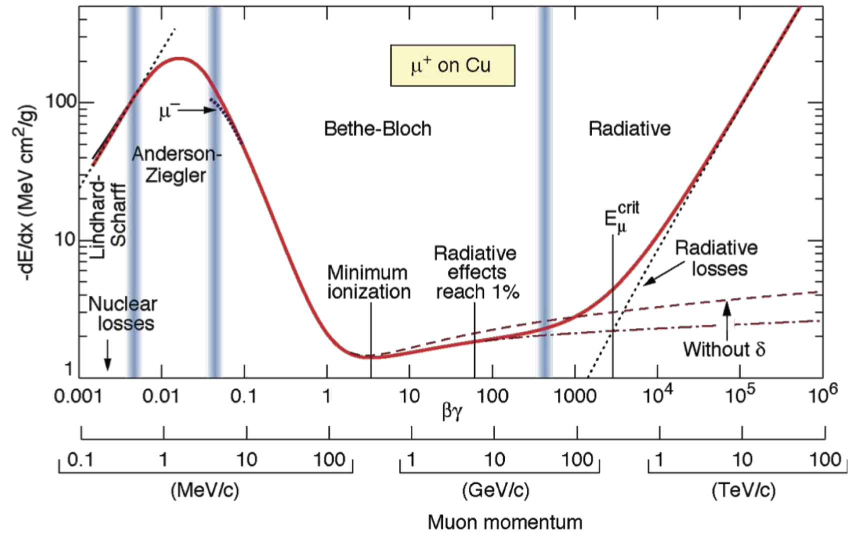
dielectric to the aluminium readout strips to prevent the readout electronics from the leakage current of the detector.

2.2.2 Signal generation

The number of created electron-hole-pairs per particle n is given as the quotient of the total energy loss E_{loss} and the energy required for the creation of an electron-hole-pair E_{eh}:

$$n = \frac{E_{\text{loss}}}{E_{\text{eh}}}. \tag{2}$$

For silicon $E_{\text{eh}} \approx 3.6\,\text{eV}$. E_{loss} comes from the Bethe-Bloch formula (see fig. 8 top) considering a minimum ionising particle (minimal turning point of the curve). However, corrections are necessary for thin layers ($300\,\mu\text{m}$), due to high energetic δ-electrons (knock-on-electrons). This is known as restricted Bethe-Bloch formula (seen in fig. 8 bottom left) and not only lowers the mean energy deposition $\frac{dE}{dx}$, but also deviates the minimum of the curve. Moreover, the statistical fluctuations of the energy loss in thin layers is described by the *Landau distribution* (seen in fig. 8 bottom right), which is not symmetric but has a long upper tail (also called *Landau tail*) due to the high energetic δ-electrons. Therefore, the mean value of the energy deposition is higher than the most probable value (peak of the Landau distribution) by a factor of 1.22. So the most probable energy loss is $E_{\text{loss}} \approx 80\,\text{keV}$, resulting in a most probable charge of about $n = 22,000$ electron-hole-pairs created by a minimum ionising particle traversing a silicon sensor of $300\,\mu\text{m}$ thickness. (More detailed information to this calculation can be found in [8].)



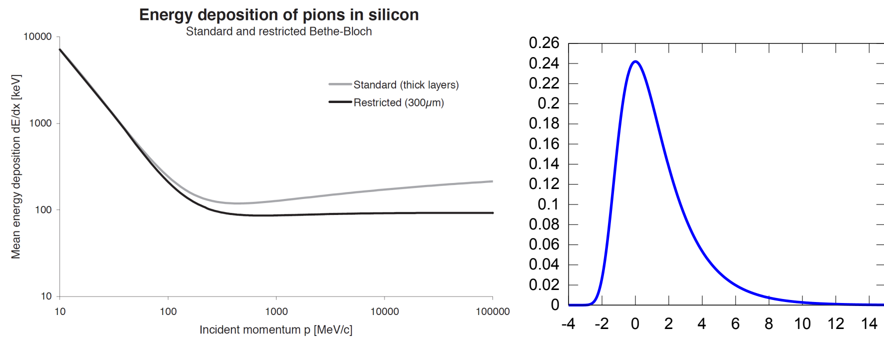


Figure 8: Top: Mean energy deposition $\frac{dE}{dx}$ according to the Bethe-Bloch formula, minimum ionisation at the minimal turning point of the curve. Bottom left: Comparison of standard (thick layers, grey) and restricted Bethe-Bloch formula (300 μm silicon, black). Bottom right: Landau distribution resulting in a ratio of 1.22 between mean value and most probable (peak) value [3, 8].

Compared to the intrinsic charge carrier density of silicon of about $10^{10}\,\mathrm{cm}^{-3}$, this is a relatively small number and, therefore, it is crucial to deplete the sensor of free charge carriers to achieve a suitable signal-to-noise ratio (SNR). Only the depleted region of the detector acts as sensitive area for detection, and so, the detector should be operated with a bias voltage sufficiently high for the space charge region to extend across the whole sensor. This threshold bias voltage is called *full depletion voltage* V_{depl} [3].

As this thesis only deals with test structures (described in sec. 3), more information about silicon sensors can be found in any of the references [9], [10], [11] or [2], a detailed explanation of the manufacturing process of silicon microstrip detectors gives [4].

2.2.3 Radiation damage

The irradiation induces changes in the semiconductor that degrade the performance of the detector and are thus called *radiation damage*. A few examples for this are an effective doping change of the bulk material (including type inversion of n-type silicon to p-type), an increase of resistivity of undepleted bulk material, a change of oxide charge or charge trapping and thus the reduction of the signal [2].

2.2.4 Manufacturers

There are two commercial vendors for the sensor production that are considered in this thesis: The Japanese company *Hamamatsu Photonics K. K.* (HPK) and the Austrian company *Infineon Technologies Austria AG* (Infineon).

3 Test structures

As the mostly rectangular sensors are produced on round wafers, there are free areas in the rim regions of the wafer, where additional devices are placed. These devices are called *test structures* (TS) and allow to extract a lot of electrical properties of a wafer that cannot be measured directly on the sensor (or only with much more difficulties). Also destructive measurements can be performed on test structures. Since they are produced on the same wafer as the sensor, one can assume that the test structures and the sensors perform identical or exhibit the same weaknesses and, therefore, they are also used to monitor the stability of the production process. The test structures are placed on semicircle-shaped wafer fragments and, thus, also called *half-moons* (HM).

A so-called standard half-moon was designed by the tracker collaboration, a test structure with identical layout for all involved vendors, so that they could be compared to each other.

These standard half-moons were also implemented in all subsequent designs to make a comparison possible. In some cases, some improvements were done or some structures were added, but all standard half-moons contain the six standard test structures that are described in the following subsections of this chapter. In figure 9, a photo of a standard half-moon of HPK and Infineon is shown.

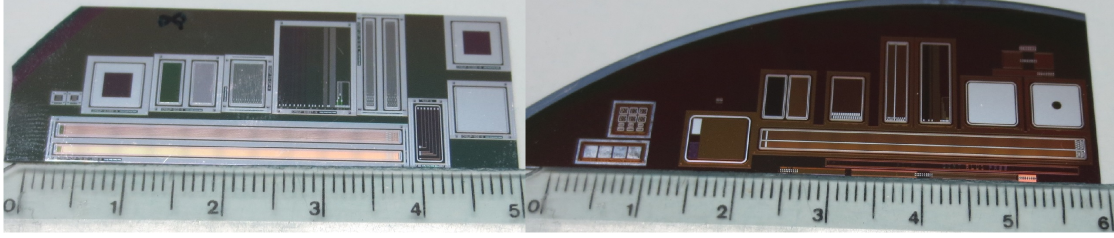


Figure 9: Standard half-moon of HPK (left) and Infineon (right).

3.1 Diode

A diode is a simple *pn*-junction where a *space charge region* (SCR) forms between the implant and the bulk material, where the two different doped semiconductors come into contact with each other. The diode is very similar to the sensor, as a sensor is basically also a simple *pn*-junction just like diode. The main difference is that the implant of the test structure is not segmented. Naturally, it is smaller in size and it also has no poly silicon resistors and bias ring, but is directly connected to the metal pad, where the bias voltage is applied.

So on a diode, the same quantities as on a sensor can be measured and the main parameters characterising the sensor can be extracted.

When a reverse bias voltage (V_{bias}) is applied to the *pn*-junction, the space charge region grows with increasing voltage, until the whole bulk is depleted of free charge carriers. The reverse bias voltage, at which the whole bulk is depleted, is called *full depletion voltage* V_{depl}. The current flowing through the SCR, called *reverse dark current*, is measured for the current versus voltage (IV) characteristic of the diode. A typical IV-curve of an n-type diode is shown in figure 10. The slope is higher for $V_{\mathrm{bias}} < V_{\mathrm{depl}}$ and becomes lower for $V_{\mathrm{bias}} > V_{\mathrm{depl}}$. The measured reverse dark current should be as low as possible to minimize the power needed for biasing the detector and it can also serve as an indicator for defects in the bulk material [13].

When a sufficiently large reverse bias voltage is applied to the diode, the junction breaks down and conducts a very large current. This breakthrough is not inherently destructive, but the maximum current must be limited to avoid an excessive heating [10].

Between the implant and the backside of the diode, the capacitance versus voltage (CV) characteristic can be measured as well. The measured capacitance is dependent on the thickness of the depletion region W, which can be estimated with [2]

$$W \approx \sqrt{2\varepsilon_0\varepsilon_{\mathrm{r}}\mu\rho|V_{\mathrm{bias}}|} \tag{3}$$

where ε_0 is the vacuum permittivity, ε_{r} is the relative permittivity, and ρ and μ are resistivity and the the mobility of the majority charge carriers of the lower doped region, respectively. According to the formula of the parallel-plate capacitor

$$C = \varepsilon_0\varepsilon_{\mathrm{r}}\frac{A}{W} \tag{4}$$

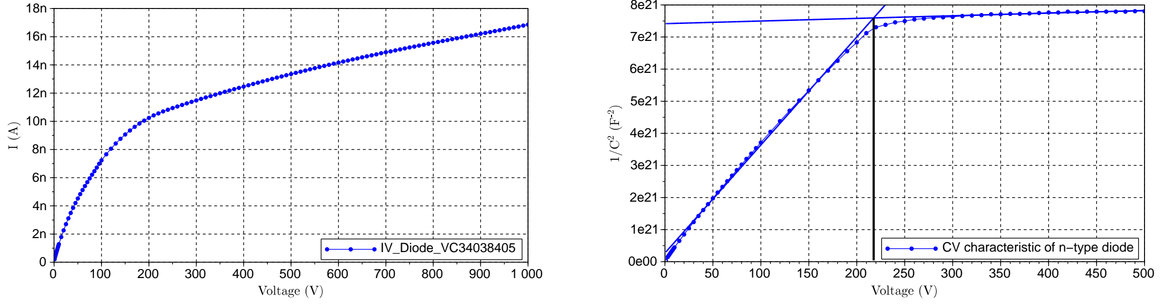


Figure 10: IV-curve of an n-type diode (left) and CV-curve with two linear fits for extracting the full depletion voltage $V_{\mathrm{depl}} = 218\,\mathrm{V}$ (right).

with the active area A of the diode, the capacitance decreases with V_{bias} in accordance with the following dependency:

$$C \approx A\sqrt{\frac{\varepsilon_0\varepsilon_\mathrm{r}}{2\mu\rho|V_{\mathrm{bias}}|}} \;\propto\; |V_{\mathrm{bias}}|^{-\frac{1}{2}}. \tag{5}$$

This formula, of course, is only valid for $V_{\mathrm{bias}} < V_{\mathrm{depl}}$, because at V_{depl} the depletion zone reaches its maximum extension and the capacitance stays constant when V_{bias} exceeds V_{depl}:

$$C = \varepsilon_0\varepsilon_\mathrm{r}\frac{A}{d} \tag{6}$$

with d the thickness of the detector that is an active region for the detection.

Due to the dependency of C on V_{bias} of eq. (5), one usually plots $1/C^2$ vs. V_{bias}, so that one can see ideally an curve that increases linearly until V_{depl} and is constant for all $V_{\mathrm{bias}} > V_{\mathrm{depl}}$. From that curve, V_{depl} can easily be extracted by two linear fits, as shown in figure 10, where a measured CV-curve of an n-type diode is plotted.

At the sensor, however, the implant is segmented into strips and, therefore, the electrical field is not linear and the depletion zone does not grow homogeneously. For that reason, a correction factor between the full depletion voltage of a segmented sensor and a planar diode has to be taken into account [14]:

$$\frac{V_{\mathrm{depl\ sensor}}}{V_{\mathrm{depl\ diode}}} = \left(1 + \frac{2p}{d}f\left(\frac{w}{p}\right)\right). \tag{7}$$

In this equation w is the strip width, p the strip pitch, d the thickness of the device and the function $f\left(\frac{w}{p}\right)$ is a numerical approximation of the Poisson equation for the non-linear field [2]:

$$f(x) = -0.00111x^{-2} + 0.0586x^{-1} + 0.24 - 0.651x + 0.355x^2. \tag{8}$$

A further quantity can be measured with the CV-characteristic: the *total capacitance* C_{tot} of the device, which is those capacitance that is measured for $V_{\mathrm{bias}} > V_{\mathrm{depl}}$

and should ideally be constant. (In practice, the mean value of the horizontal fit over the fitted region is taken for C_{tot}; normally the CV-curve is measured up to twice the expected V_{depl}, so that one has roughly the same number of measured points for the fit of the linearly increasing part of the curve and the fit of the horizontal one.) With C_{tot} one can determine the active thickness d of the device, which is the fully depleted region that is an active region for the detection of the sensor, by using the equation of the parallel plate capacitor of eq. (6):

$$d = \varepsilon_0 \varepsilon_{\text{r}} \frac{A}{C_{\text{tot}}}. \tag{9}$$

With V_{depl} and C_{tot} one can furthermore determine the resistivity of the bulk material ρ_{bulk} with the equation [2]:

$$\rho_{\text{bulk}} = \frac{d^2}{2\varepsilon_0 \varepsilon_{\text{r}} \mu V_{\text{depl}}} \tag{10}$$

respectively with eq. (9) inserted:

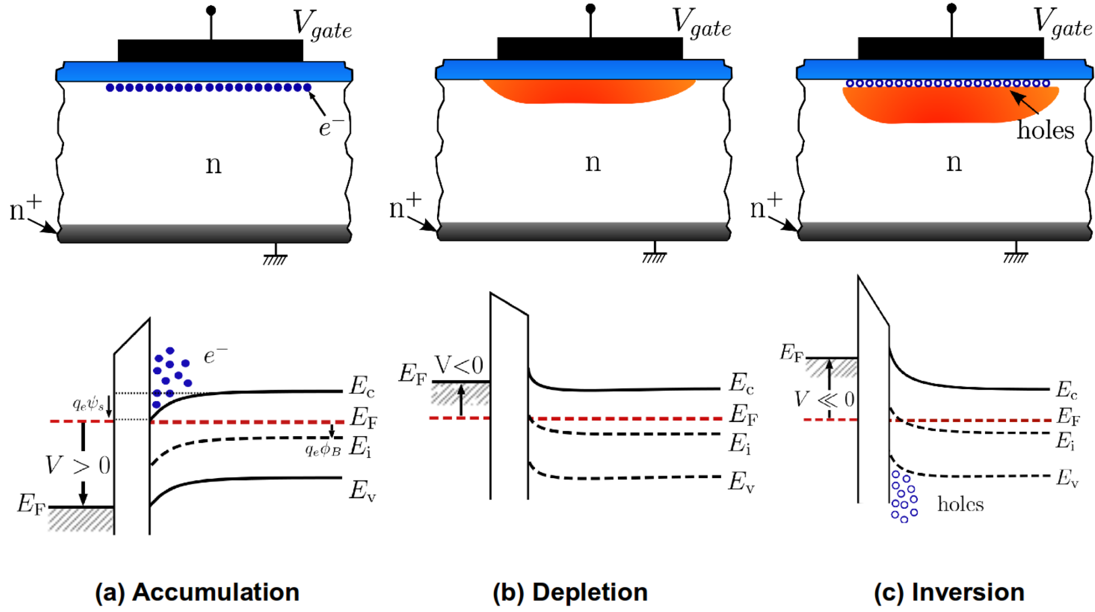
$$\rho_{\text{bulk}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} A^2}{2\mu C_{\text{tot}} V_{\text{depl}}}. \tag{11}$$

At last, a remark to the determination of the active area A, occurring in many formulas in this section: This is the area of the depletion zone forming under the implant, but the depletion zone does not only grow in depth, but also laterally, according to formula (3). So A is not identical with the area of the implant region, but is measured from half the way between the implant and the *edge ring*. The edge ring is encircling every device and shielding it electrically from the other devices on the wafer because it is doped the same way as the backplane and, therefore, practically lies on backplane potential. So we can assume that the potential applied on the metal pad falls to backplane potential to the guard ring.

3.2 MOS

A *Metal Oxide Semiconductor* (MOS) structure consists, as the name says, of a metal layer, an oxide layer and a semiconductor. More general, this structure is referred to as a *MIS* (*metal-insulator-semiconductor*) structure, but as for silicon devices the common insulator is SiO_2, the more commonly used expression is MOS.

The metal layer of the MOS is called *gate*, here the *gate voltage* V_{gate} is applied to vary the band structure of the energy band diagram beneath the semiconductor-oxide interface. When no voltage is applied, the semiconductor bands bend down to the dielectric layer for n-doped silicon (and up for p-doped silicon) to accommodate the work function difference between the metal and the semiconductor, because at thermal equilibrium the Fermi level must be constant. The work function $q\Phi$ is the energy necessary to move an electron from the Fermi level to the vacuum level. To achieve the so-called *flat-band* condition, when all bands are flat, the work function difference



(a) Accumulation **(b) Depletion** **(c) Inversion**

Figure 11: A schematic cross section (top) and the energy band diagram (bottom) of an n-type MOS in (a) accumulation, (b) depletion and (c) inversion. In the energy band diagrams one can see from left to right the metal with the Fermi level E_{F}, the oxide and the semiconductor with the conduction band E_{c}, the quasi Fermi level E_{F}, the intrinsic Fermi level E_{i} and the valence band E_{v} [15, 16].

between the metal and the semiconductor $q\Phi_{\text{m}} - q\Phi_{\text{s}}$ has to be compensated by applying an external voltage, the so-called *flat-band voltage* V_{fb}[11]:

$$V_{\text{fb}} = \Phi_{\text{m}} - \Phi_{\text{s}}. \tag{12}$$

This equation is, however, only valid in the ideal case of the absence of oxide charges. Hence, the value of V_{fb} can be used as an indicator of the oxide charges, as we will see later. But first, we discuss further states an external gate voltage V_{gate} can induce (In figure 11 the schematic cross section (top) and the energy band diagram (bottom) of an n-type MOS is shown, and so we will discuss the following cases for an n-type semiconductor):

Accumulation: When $V_{\text{gate}} > V_{\text{fb}}$, the energy bands bend downwards in the boundary region and the Fermi level gets closer to the conduction band edge and so free electrons are accumulated at the semiconductor-oxide interface (fig. 11 (a)).

[11] Theoretically V_{fb} should be close to zero, because the work function difference $\Phi_{\text{m}} - \Phi_{\text{s}} := \Phi_{\text{ms}}$ is very small and typically lies in a range of -0.1 V and -1 V, but it is dependent on the doping concentration and the temperature [15].

Depletion: For $V_{\text{gate}} \leq V_{\text{fb}}$, the energy bands bend upwards at the semiconductor-oxide interface and the electrons are repelled from the interface region and a depletion layer forms beneath the interface (fig. 11 (b)).

Inversion: If the voltage is further decreased ($V_{\text{gate}} \ll V_{\text{fb}}$), the intrinsic Fermi level (E_{i}) at the interface will reach and cross the quasi Fermi level (E_{F}) and the concentration of holes will increase, so that a layer filled with minority charge carriers forms, called *inversion layer* (fig. 11 (c)). When the Fermi level and the intrinsic level at the interface coincide, the concentrations of electrons and holes are the same (and equal to the intrinsic carrier concentration) and the inversion layer starts to form. This happens, when the surface potential Ψ_{s} equals the potential difference of the Fermi level and the intrinsic level ϕ_{B} (both drawn in fig. 11 (a)). When $\phi_{\text{B}} < |\Psi_{\text{s}}| < 2\phi_{\text{B}}$, the concentration of holes at the interface is higher than that of the electrons, but lower than the doping concentration, what is referred to as *weak inversion*. For $|\Psi_{\text{s}}| \geq 2\phi_{\text{B}}$, the concentration of minority charge carriers at the interface exceeds the doping concentration of the silicon bulk, and that state is called *strong inversion* [15, 11].

Although the behaviour above was described for n-type MOS, for p-type it is very analogue, only all polarities have to be reversed, the bands bend up instead of down and vice versa and, instead of electrons, the holes are the majority charge carriers and the electrons the minority charge carriers.

Now to the practical purpose of a MOS as a test structure: For a real MOS structure, the flat-band voltage does not only depend on the work function difference $\Phi_{\text{m}} - \Phi_{\text{s}} := \Phi_{\text{ms}}$, but also on charges present in the oxide or at the oxide-semiconductor interface. There are oxide trapped charges, mobile ionic charges, fixed oxide charges (near the interface) and interface trapped charges. The flat-band voltage change doesn't only depend on the amount of charge, but also on the distribution inside the oxide (in particular on the distance x from the metal gate). Thus, the flat-band voltage, with the combined effect of a surface charge density σ at the interface (with a distance from the metal gate of d_{ox}, the oxide thickness) and a volume charge density $\rho(x)$ inside the oxide, can be written as [11]:

$$V_{\text{fb}} = \Phi_{\text{ms}} - \frac{\sigma d_{\text{ox}}}{\varepsilon_{\text{ox}}\varepsilon_0} - \frac{1}{\varepsilon_{\text{ox}}\varepsilon_0}\int_0^{d_{\text{ox}}} \rho(x)x dx. \tag{13}$$

From a MOS device, the capacitance is measured and plotted over the gate voltage, since this curve shows a typical characteristic for the regions of accumulation, depletion and inversion explained above. In the case of accumulation, one measures the constant capacitance of the oxide layer C_{ox}. When V_{gate} reaches the region of depletion, the capacitance drops down rapidly as the depletion layer grows (because $C \propto \frac{1}{d}$, see eq. (6)). The measured capacitance is the series of the oxide capacitance C_{ox} and the capacitance of the depletion layer forming in the semiconductor C_{s}: $C = \frac{C_{\text{ox}}C_{\text{s}}}{C_{\text{ox}}+C_{\text{s}}}$. The capacitance measured in inversion depends on the frequency of the AC signal applied to the MOS for measuring the capacitance. If the AC signal is of a sufficiently low frequency for the minority charge carriers to be able to respond to the signal, they can move into

the depletion layer and short the capacitance and the low-frequency (lf) MOS-curve is obtained, where one measures the oxide capacitance C_{ox} only. If the AC signal frequency is too high for the minority charge carriers to be able to respond to the signal, the more commonly measured high-frequency (hf) MOS-curve is obtained, where one measures the series of the oxide capacitance and the capacitance of the depletion layer at its maximum extent, and so this capacitance stays constant. However, when the DC sweep rate is too high, so that no inversion charge can form during the sweep, the capacitance doesn't stay constant, but drops further down and one obtains the deep-depletion curve [9, 15].

To obtain the true hf-curve, one has to ensure that the time between setting the gate voltage and measuring the capacitance is long enough for the device to come to equilibrium, because otherwise, at a sweep direction from accumulation to inversion, the CV-curve tends to go into partial deep depletion and the resulting curve will be below the true one, and, for a sweep direction from inversion to accumulation, inversion charge can be injected into the substrate and the measured curve will be above the true curve in the inversion region [9].

With the oxide capacitance C_{ox} measured in the accumulation region, one can easily compute the thickness of the oxide d_{ox} by inserting it in equation (9) with the area of the metal gate for A.

The main interest in this measurement, however, is the change of the CV-curve due to oxide charges and interface traps. While the oxide trapped charges, the mobile ionic charges and the fixed oxide charges cause a parallel shift of the CV-curve, the shift due to large amounts of interface trapped charges varies with the surface potential and, therefore, this contribution doesn't only shift but also distort the CV-curve [10].

To measure the shift of the CV-curve, one can lay three linear fits into the hf-curve of the MOS, one in each region of accumulation, depletion and inversion, as seen in figure 12, and extract V_{fb} as the voltage where the capacitance dropped to half the value between accumulation and inversion, to compare it to the ideal value of $V_{\text{fb}} \approx 0$ or a reference sample. C_{ox} is taken as the mean value of the accumulation fit over the fitted region.

3.3 Gate Controlled Diode

A *gate controlled diode* (GCD) is a combination of a diode and a MOS structure. It consists of a segmented implant that is comb-shaped and intertwined with a comb-shaped MOS structure, which consists of a gate coupled over a dielectric layer to the bulk between the implant strips[12]. In figure 13, one can see an image detail of the comb-shaped gate of a GCD under the microscope. The gate can be made not only out of metal (e.g. aluminium), but also out of polysilicon and it should overlap the implant region slightly to prevent potential barriers [9].

Similar to a MOS device, a GCD is operated in three different states: Accumulation, depletion and inversion. However, from a GCD, the current that flows between the implant and the backplane is measured as a function of the gate voltage V_{gate}, keeping

[12]There are also produced round GCDs with a circular implant that is encircled by one or more gate rings.

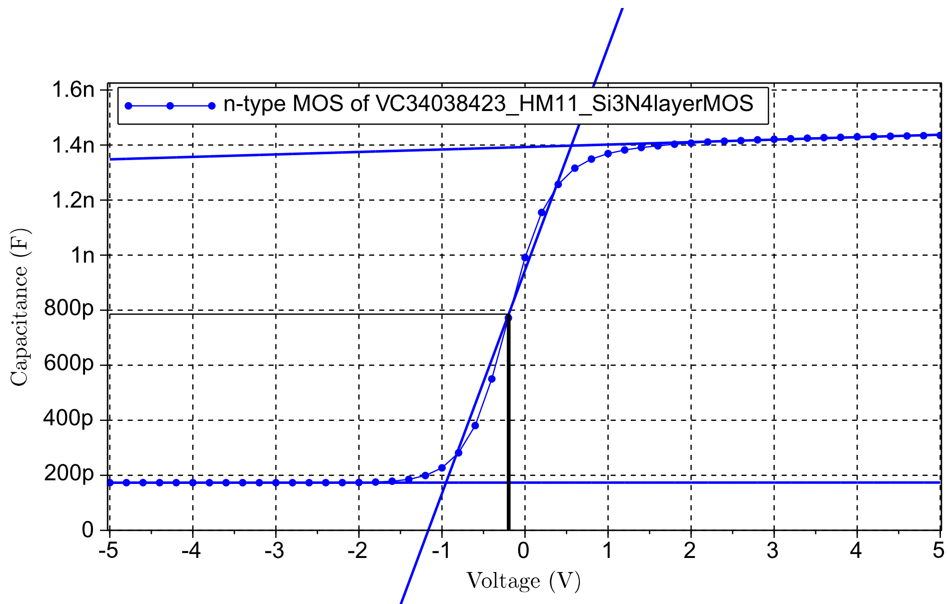


Figure 12: Example for a fit of a hf-MOS-curve with a resulting $V_{\text{fb}} = -0.2\,\text{V}$ and $C_{\text{ox}} = 1.42\,\text{nF}$.

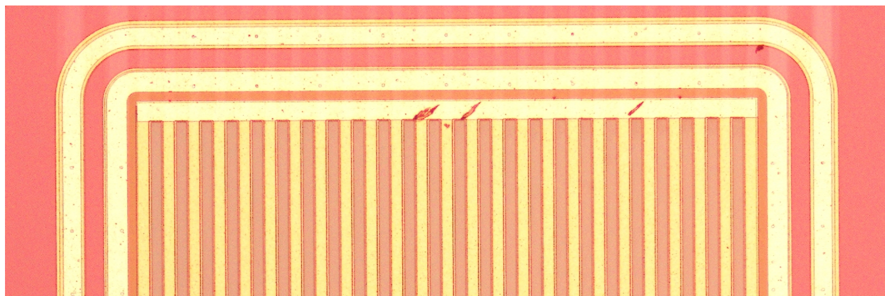


Figure 13: A picture detail of a GCD under the microscope of the comb-shaped gate (yellowish) and the implant stripes in between (reddish).

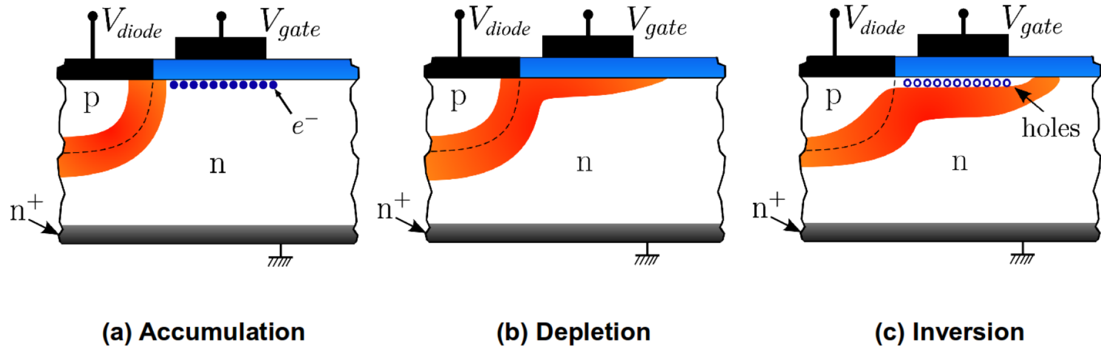


Figure 14: A schematic cross section of an n-type GCD in (a) accumulation, (b) depletion and (c) inversion [16].

the bias voltage V_{bias} constant. Figure 14 shows a schematic cross section and the working principle of an n-type GCD and figure 15 an ideal IV (current vs. gate voltage) curve with all current contributions in the different regions that are explained below:

Accumulation: When $V_{\text{gate}} > V_{\text{fb}}$, electrons accumulate beneath the oxide layer under the gate and separate the implant strips (see fig. 14 (a)). The measured current in this situation is only the diffusion current I_{diff} and the bulk-generation current due to defects in the depleted region of the diode $I_{\text{bulk, diode}}$ (as seen in fig. 15).

Depletion: When V_{gate} reaches V_{fb}, the region under the gate starts to deplete and the current increases rapidly, due to the surface generation current I_{surf} arising from the interface traps (see fig. 14 (b) and fig. 15). The total current measured in depletion is the sum of the surface generation current I_{surf}, the diffusion current I_{diff} and the bulk-generation current due to defects in the depleted region of the diode $I_{\text{bulk, diode}}$ and the MOS $I_{\text{bulk, MOS}}$. The state of depletion holds for $V_{\text{fb}} > V_{\text{gate}} > V_{\text{fb}} + V_{\text{bias}}$ and the depletion zone under the gate widens with increasing V_{gate} and connects the depletion zones from the adjacent implant strips. The current increases slightly, as the bulk-generation current due to defects in the depleted region of the MOS $I_{\text{bulk, MOS}}$ increases with the widening of the depletion zone under the gate (see fig. 15).

Inversion: If the voltage is further decreased, for $V_{\text{gate}} < V_{\text{fb}} + V_{\text{bias}}$, holes accumulate beneath the oxide-semiconductor interface under the gate and shield the interface traps and, thus, suppress the surface current. Therefore, the current rapidly drops at $V_{\text{fb}}+V_{\text{bias}}$ and then stays constant at the level of I_{diff} plus $I_{\text{bulk, diode}}$ plus $I_{\text{bulk, MOS}}$.

The I vs V_{gate} characteristic of a GCD can be easily used to extract the surface current due to the interface traps, as I_{surf} is the height of the step of the depletion region [15].

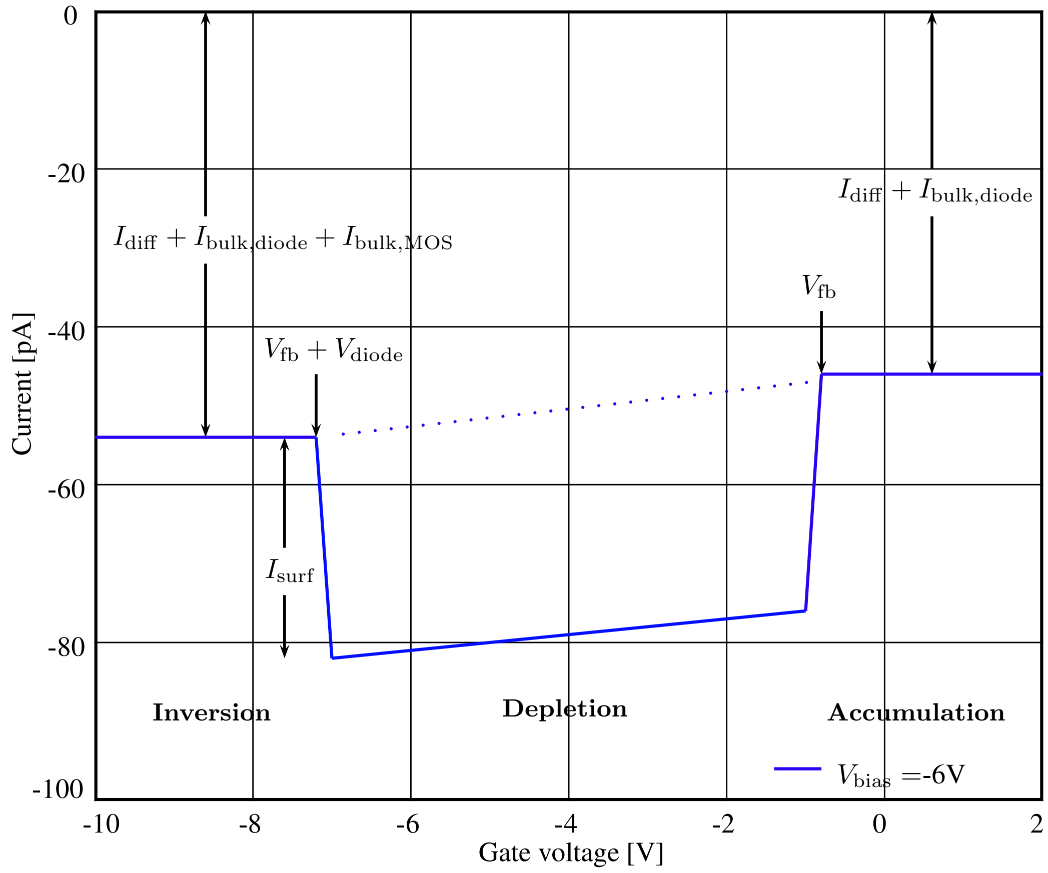


Figure 15: Ideal IV (current vs. gate voltage) curve of a GCD with all current contributions in the different regions at a bias voltage of $-6\,\mathrm{V}$ [15].

3.4 Interstrip capacitance C_{int}

The interstrip capacitance C_{int} is measured on the CAP-TS-AC test structure. This test structure consists of 9 strips that are processed the same way and, naturally, have the same geometry as the sensor. However, the outermost sets of 3 strips on either side are connected among themselves to lie on the same potential and are intended to reproduce the sensor conditions. Between the middlemost strip and its two adjacent strips, the interstrip capacitance is measured, while the structure is biased with different bias voltages over the bias ring.

The so obtained CV characteristic shows variable values within the first voltage steps, when the strips are not perfectly isolated from each other, but stays constant when the area beneath the implant strips is fully depleted [17].

The value of C_{int} is an important parameter for achieving a low signal-to-noise ratio (SNR) of the sensor [13].

3.5 Interstrip resistance R_{int}

The interstrip resistance R_{int} is measured on the CAP-TS-DC test structure, which is very similar to the CAP-TS-AC test structure. Though, the polysilicon resistors are lacking and, thus, the strips are not connected to the bias ring and therewith to each other. This is necessary, because otherwise, essentially the polysilicon resistors would be measured, since they are much smaller than the interstrip resistance. In addition, the implant strips are connected directly to the metal layer above through contact holes and, thus, can be contacted also by the AC pads.

The interstrip resistance is measured between the middlemost strip and its two adjacent strips at different bias voltages. At each bias voltage step (which is applied at the backplane while the bias ring is kept on ground), a small voltage ramp is applied between the middlemost strip and its two grounded adjacent strips and the current flowing between the strips is measured. From the resulting IV curves, the resistance values are obtained by linear fits. This increases the measurement accuracy and suppresses the contribution of a constant leakage current. However, the voltage ramp must be kept small in respect to the bias voltage to avoid a perturbation of the depletion field. Besides, the measured current is expected to be very small, as the interstrip resistance should be high to ensure a good spatial resolution of the sensor [7, 13].

3.6 Sheet resistances

The test structure called *sheet* is designed to measure the resistance values of all conductive layers. These are metal, polysilicon, strip implant, edge implant, and for n-in-p type also p-stop or p-spray. For each material, there are some meander shaped structures with different widths and lengths, where the resistance value is extracted with a linear fit from an IV curve measured on each structure. The measured resistance scales with the length and the inverse of the width. So, for the specific resistivity $\rho/sq.$ in $\Omega/\text{sq.}$ (which is called *sheet resistance*), it is divided by the length and multiplied by the

width, or directly multiplied by the *square number*, as the ratio of width to length w/l is called and which is normally known for each sheet structure.

While for the metal and the polysilicon measurement a depletion zone has no significant influence, for the resistance measurement of the implants, a sufficient bias voltage is essential to ensure that there is no short between the meander of the structure and the resistance over the whole length of the implant is measured.

4 Standard measurements on test structures

All the measurements were performed on the *Process Qualification Center* (PQC) setup in the clean room of HEPHY (fig. 16). This setup consists of a probe table where the device under test can be fixed with a vacuum jig. This table is made of aluminium and connected to a cable, so that the backplane of the device is contacted. Furthermore, there are several needles attached to positioners with micrometer screws to contact the various pads on the surface of the devices. Above the probe table is installed a microscope, which is needed to see the fine structures of the devices and to contact the pads with the needles. All this is set in a light-tight box that is made from aluminium to serve as a Faraday cage and prevent the devices from light-induced currents. Moreover, the environmental conditions in the box (temperature and relative humidity) are monitored and nitrogen gas can be injected to reduce the relative humidity inside the box. In addition, the probe table is equipped with Peltier elements that are joined to a secondary cooling circuit with a liquid coolant, so that the device can be set to a fixed temperature[13].

The measurement devices are located outside the box and connected with the needles and the probe table with plugs through the box. In addition, they are connected via GPIB[14] to a computer where *Labview*[15] programs are controlling all the devices and retrieving the data. For this setup the following measurement instruments were available:

Source measure unit (SMU): Keithley 237: For applying and measuring a voltage or current with high accuracy (pA-range).

Secondary source measure unit (SMU2): Keithley 2410: An additional SMU, required for some of the measurements for applying a gate voltage.

Capacitance meter (LCR): Agilent E4980A: A high-frequency capacitance measure device using frequencies between 20 Hz and 2 MHz. A decoupling box separates the LCR meter from the high bias voltages and thus allows DC voltages beyond the instruments limit of 42 V.

All the standard test structures were measured on an n-type half moon of HPK, a p-type half moon with p-stop implantation and a p-type half moon with p-spray layer,

[13] In the range of −20 to +200 °C [3].

[14] *General Purpose Interface Bus.*

[15] National Instruments, Labview – Graphical Development Environment for Data Acquisition, Analysis, and Presentation (http://www.ni.com/labview/).

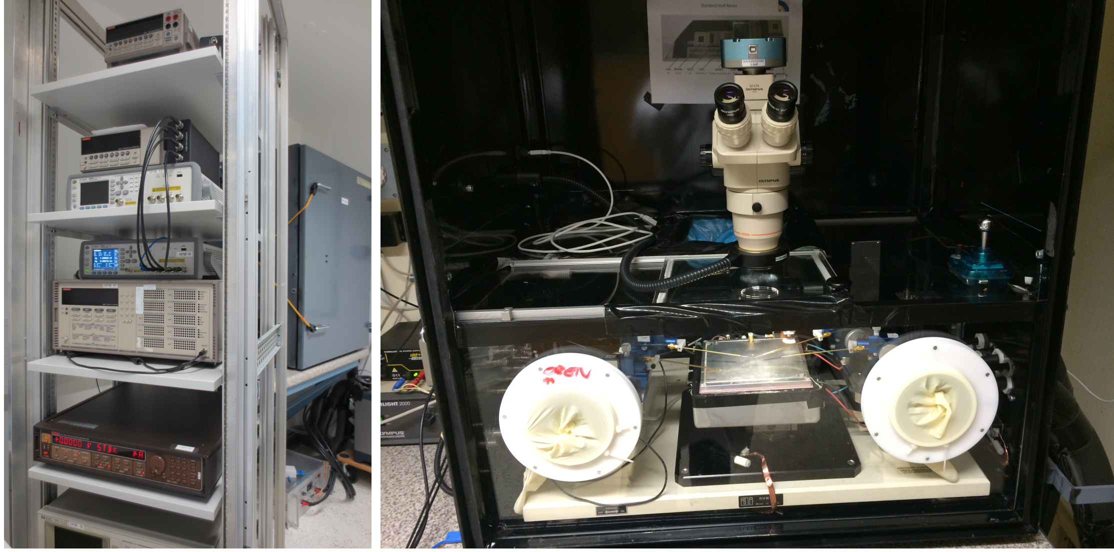


Figure 16: Pictures of the PQC setup.

also from HPK, and for comparison on two half moons of Infineon, one from run 1 and one from run 4, which were, however, only in n-type available. The used wafers are listed in table 1 with their descriptions. The n-type and p-type half moons are identical in design, only the structures CAP-TS-AC, CAP-TS-DC and sheet of the p-type wafer with p-stop have additional p-stop implantations. The wafer with p-spray naturally has a p-spray layer over the whole wafer and, therefore, over all structures. Though, this shouldn't influence the devices, since the doping concentration of the p-spray layer is much less than that of the implant.

[16]Technique used for ingot production; in contrast to Czochralski process which is more often used in chip production but obtains lesser purity [18].

structure	description	producer
FZ320N_W4_TS-2	float-zone[16], 320 nm thickness, n-type, wafer 4, TS 2	HPK
FZ320P_W6_TS-2	float-zone, 320 nm thickness, p-type with p-stop, wafer 6, TS 2	HPK
FZ320Y_W4_TS-2	float-zone, 320 nm thickness, p-type with p-spray, wafer 4, TS 2	HPK
VC14095619_ExtHM	n-type, run 1, wafer 19, extended half moon	Infineon
VC34038405_ExtHM_8	n-type, run 4, wafer 5, extended half moon 8	Infineon

Table 1: Measured structures and their description.

V_{max}	±1000 V
Stepsize	10 V
Compliance	10 μA
Wait	1000 ms

Table 2: Parameters for the IV-measurements of the diodes.

SMU	
V_{max}	±500 V
Stepsize	10 V
Compliance	20 μA
Wait	1000 ms
LCR initialisation	
Voltage level	100 mV
Current level	0
Frequency of AC signal	1 kHz

Table 3: Parameters for the CV-measurement of the diodes.

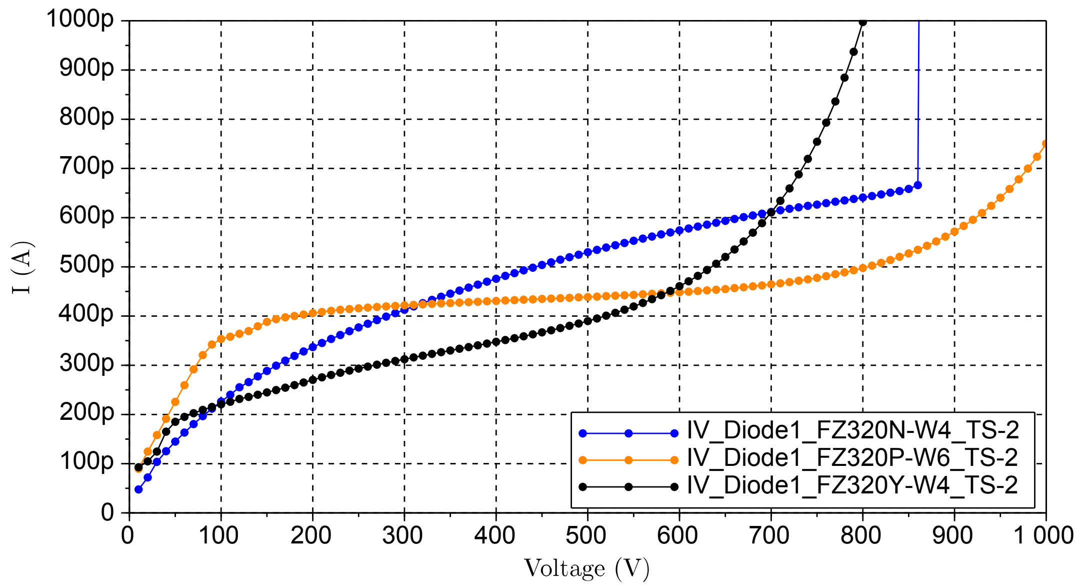
4.1 IV-characteristic of diodes

For the IV-characteristic of a diode, the SMU is connected to the aluminium layer of the diode with its grounded LO-terminal and to the backplane its HI-terminal. Then, the reverse dark current through the diode is measured while the bias voltage is ramped up. The measurement was controlled by the Labview program 'Diode_IV_ntype.vi' for n-type and 'Diode_IV_ptype.vi' for p-type, respectively. The chosen parameters are listed in table 2. For n-type, a positive bias voltage, and for p-type, a negative one has to be applied to operate the diode in reverse direction.

The results of the reverse dark current measurements are plotted in fig. 17, on the abscissa the modulus of the bias voltage is displayed. Only the two diodes from the Infineon wafers are absolutely stable until 1000 V, the n-type diode from HPK exhibited a breakthrough at 860 V, the p-type with p-spray showed a soft breakthrough at about 900 V and the p-type with p-stop was stable until 1000 V, but showed the beginning of a soft breakthrough.

4.2 CV-characteristic of diodes

For the CV-characteristic of a diode, the LCR meter is connected via the decoupling box (DCB) parallel to the SMU, to the backplane with the HI-terminal and to the aluminium pad of the diode with the LO-terminal, as can be seen in the circuit diagram in fig. 18. The capacitance of the depleted area is measured while the bias voltage is ramped up. The measurement was controlled by the Labview programs 'Diode_CV_ntype.vi' and 'Diode_CV_ptype.vi', respectively. All the parameters listed in table 3, the bias voltage is again positive for n-type and negative for p-type.



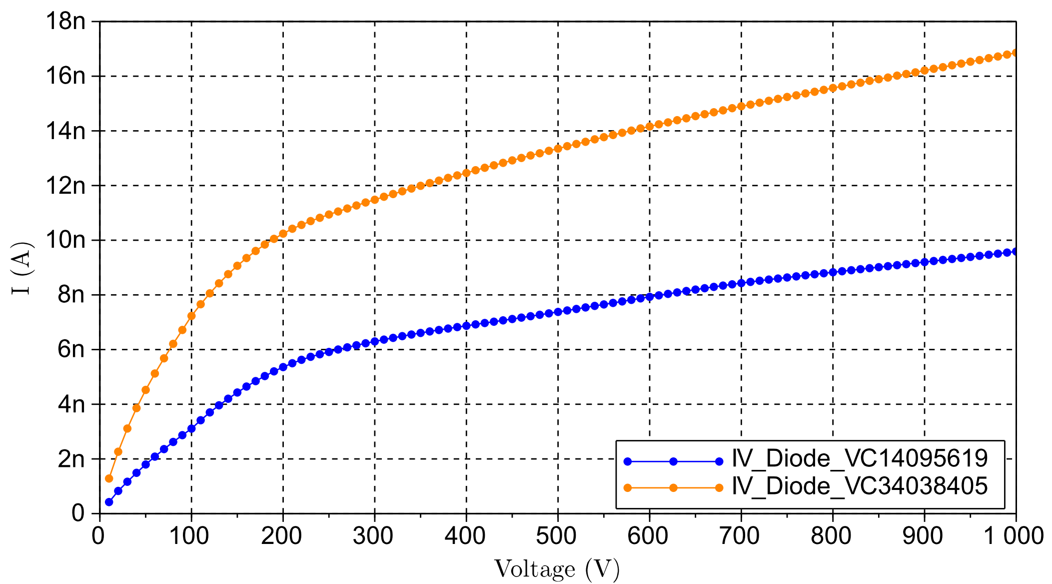


Figure 17: IV curves of the diodes (top: HPK, bottom: Infineon). The bias voltage was ramped up to $\pm 1000\,\mathrm{V}$ in steps of $10\,\mathrm{V}$. On each step the reverse dark current was measured after a delay time of $1\,\mathrm{s}$.

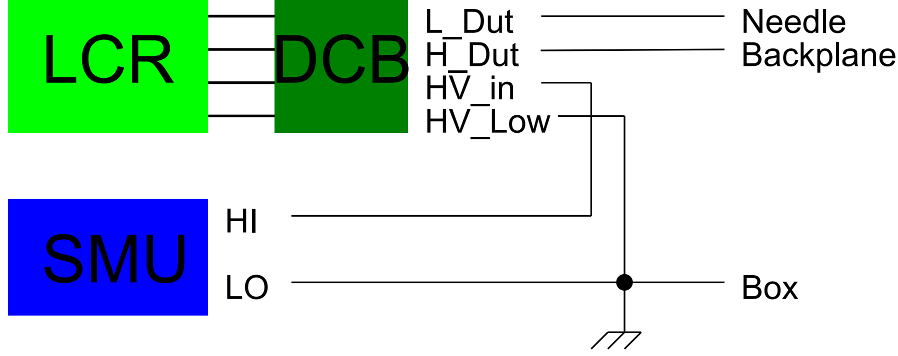


Figure 18: Circuit diagram for the CV-measurements of the diodes and MOS.

structure	V_{depl}	C_{tot}	d
FZ320N_W4_TS-2	188 V	10.3 pF	281 μm
FZ320P_W6_TS-2	−221 V	10.1 pF	286 μm
FZ320Y_W4_TS-2	−218 V	10.4 pF	278 μm
VC14095619_ExtHM	232 V	11.3 pF	309 μm
VC34038405_ExtHM_8	218 V	11.5 pF	304 μm

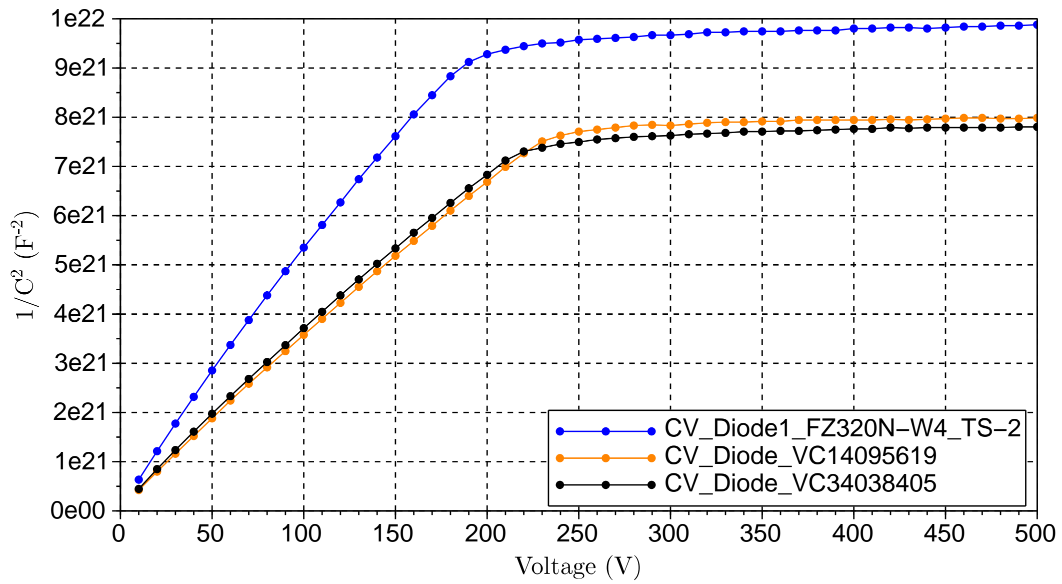
Table 4: Results of the CV-measurements of the diodes for the full depletion voltages V_{depl}, the total capacitances C_{tot} and the active thicknesses d.

The results of the capacitance measurements are plotted in fig. 19. The full depletion voltages V_{depl}, extracted with fits as described in section 3.1, are listed in table 4 together with the total capacitances C_{tot} of the diodes and the active thicknesses d. The latter ones were calculated with equation (9), therefore the active areas A were needed. They were determined as described at the end of section 3.1 and also the rounded corners were considered. In figure 20 the layout file from an Infineon diode is shown with the measured distances. A was then calculated with the formula:

$$A = a^2 - \left(c - \frac{b}{2}\right)^2 \cdot (4 - \pi) \tag{14}$$

with a the side length of the square from half the way between the implant and the edge ring, b the distance from implant to edge ring and c the radius of the rounded corners of the edge ring (see fig. 20). For the Infineon diodes these values are: $a = 5800\,\mu$m, $b = 500\,\mu$m and $c = 750\,\mu$m, and for the HPK diodes: $a = 5267.5\,\mu$m, $b = 374.5\,\mu$m and $c = 453.5\,\mu$m. So one obtains $A_{\text{Infineon}} = 33.4\,\text{mm}^2$ and $A_{\text{HPK}} = 27.7\,\text{mm}^2$ for the active areas.

The results for the active thicknesses d were a bit surprising, as the wafers from HPK are $20\,\mu$m thicker than that from Infineon, actually. Though, HPK made a deeper backside implantation to reduce the active thickness to $300\,\mu$m. Obviously, this reduces d more than $20\,\mu$m, presumably because the implantation gradient is less sharp for deeper



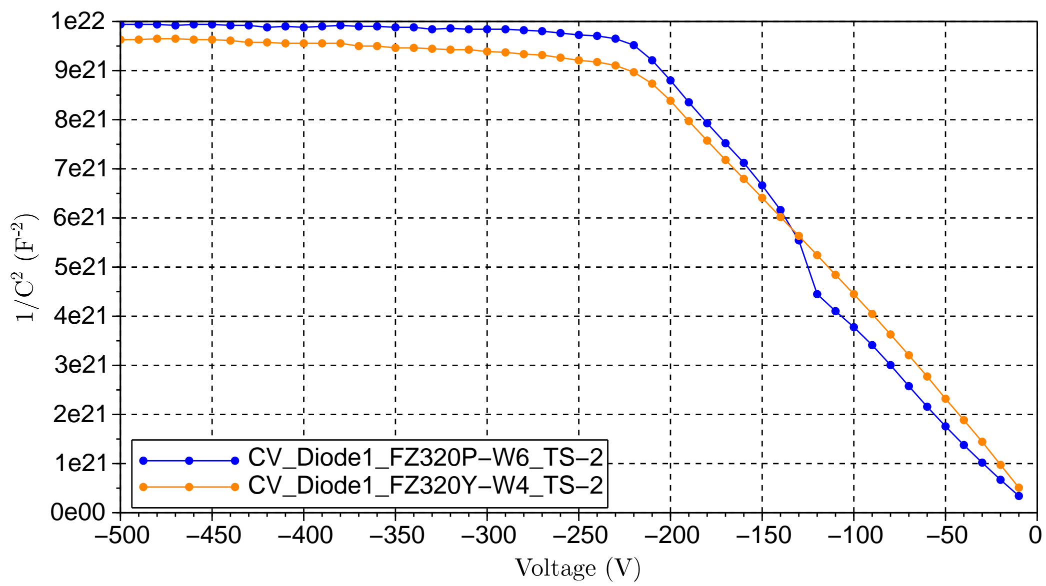


Figure 19: CV curves for n-type (top) and p-type (bottom) diodes. The bias voltage was ramped up to ±500 V in steps of 10 V. On each step the capacitance of the depleted area was measured after a delay time of 1 s.

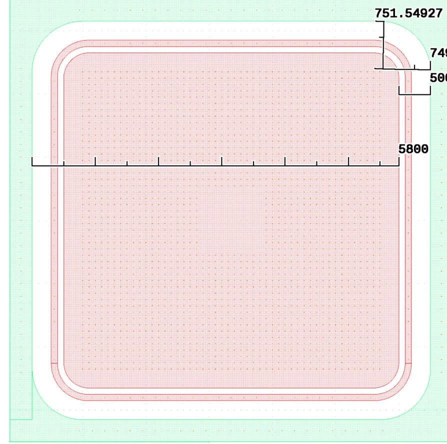


Figure 20: Layout file from an Infineon diode with the implant, the guard ring (not used) and the edge ring (green). The side length from half the way between the implant and the edge ring is $a = 5800\,\mu$m, the distance from implant to edge ring is $b = 500\,\mu$m and the radius of the rounded corners of the edge ring is $c = 750\,\mu$m (for the Infineon diodes).

implantation. The difference in the active thickness also explains the difference of the CV-curves between Infineon and HPK in figure 19 (top).

Furthermore, there was investigated whether one can measure the IV-characteristic and the CV-characteristic in one measurement to achieve more time and work efficiency. In the CV-measurement, the current is also measured and recorded in the file. However, it is measured via the decoupling box and, therefore, depends on the delay time between applying the voltage and measuring the current, as the decoupling box consists of big capacitors that are charged and need some time to discharge.

Hence, capacitance and current versus bias voltage measurements were performed with different delay times and the effect on the IV- and the CV-characteristics was examined. This was done on the structure VC34038405_ExtHM_7, with the same settings as in table 3, but 5 V stepsize and delay times ($Wait$) of 200 ms, 1 s, 2 s, 3 s, 4 s and 5 s, and the curves were measured only up to $V_{\text{max}} = 100$ V, except for the curves with $Wait = 200$ ms, 1 s and 3 s, they were measured up to $V_{\text{max}} = 500$ V.

The resulting IV- and CV-curves can be seen in fig. 21, the IV- on the left side and the CV-curves on the right side. One can see that the current values are some orders of magnitude higher than that in fig. 17 in the previous subsection (4.1) and are decreasing with the delay time exponentially, as plotted in fig. 22 with logarithmic ordinate. Even for a delay time of $Wait = 5$ s, the current is still at approximately 25 nA and, therewith, about one order of magnitude too high. Furthermore, the current is constant over the bias voltage and doesn't show the characteristic shape described in section 3.1. Therefore, the IV-characteristic is measured separately without LCR-meter and decoupling box.

The CV-curve, however, doesn't change with the delay time and the full depletion

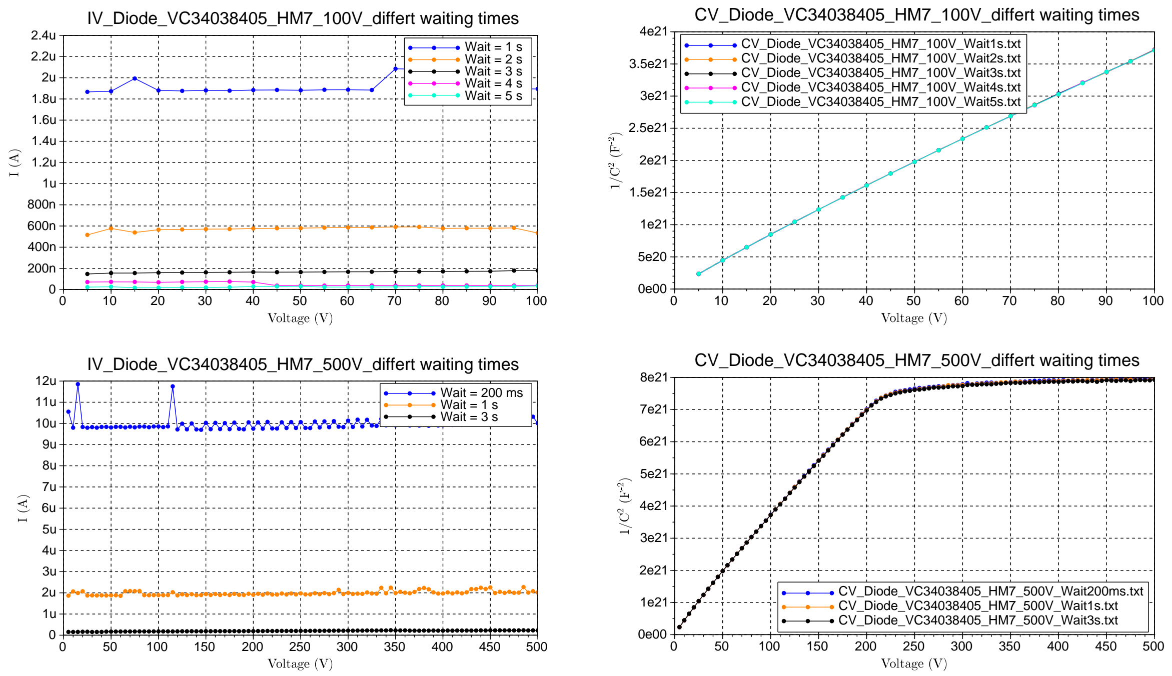


Figure 21: IV-curves (left side) and CV-curves (right side) measured at the same time (both via DCB) and with different waiting times (top: 1, 2, 3, 4 and 5 s; bottom: 0.2, 1 and 3 s).

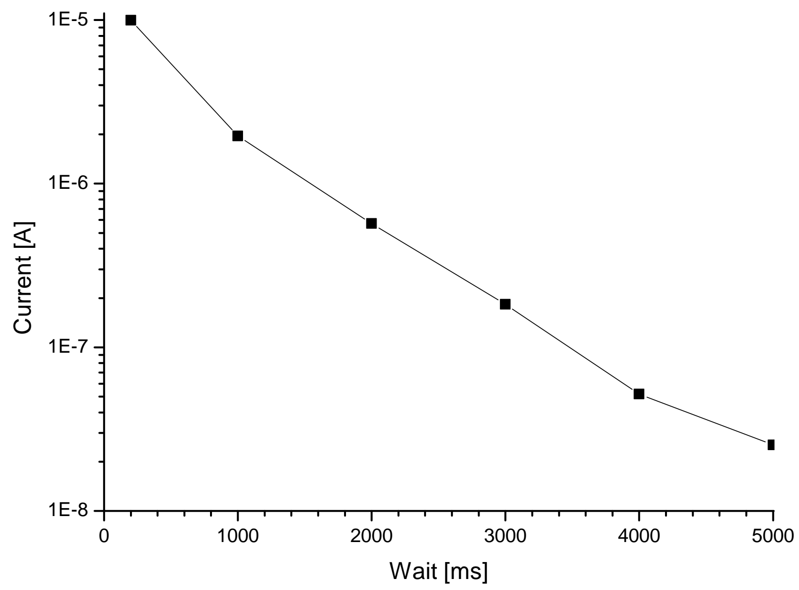


Figure 22: The current measured via LCR-meter and decoupling box is exponentially decreasing with the delay time.

SMU	
V_{min}	$-15\,\text{V}$
V_{max}	$+15\,\text{V}$
Stepsize	1 V
Compliance	$10\,\mu\text{A}$
Wait	1000 ms
LCR initialisation	
Voltage level	5 mV
Current level	0
Frequency of AC signal	1 kHz

Table 5: Parameters for the CV-MOS-measurements of fig. 23.

voltage, that can be fitted from the lower right plot in fig. 21, is also identical for all curves ($V_{\text{depl}} = 216\,\text{V}$). Thus, the CV-characteristic is measured with a delay time of $Wait = 1\,\text{s}$, because this doesn't retard the measurement time too much and with only 200 ms of delay time, one can see in the lower left plot of fig. 21 that the current is more noisy and, with values of $10\,\mu\text{A}$, rather high, as this is normally set for the compliance value.

4.3 CV-characteristic of MOS

For the CV-characteristic of the MOS, the device is connected to the LCR-meter and the SMU the same way as the diode for the CV-measurement (explained in the previous subsection and seen in fig. 18). On the MOS, the capacitance between the gate and the backplane is measured while the voltage applied to the gate is varied between -15 and $+15\,\text{V}$. All measurements were controlled by the program 'MOS_CV_nptype.vi' with the parameters listed in table 5. Here, the gate voltage was varied from minus to plus for all wafer types.

The results of the MOS-measurements are shown in fig. 23. For the n-type MOS, the region of accumulation is on the left side of the plot, where the gate voltage is negative, and the region of inversion where V_{gate} is positive, though, for p-type it is the other way around. Hence, the p-type MOS were measured here in the direction from inversion to accumulation. According to this, the step in the curve of the MOS of the p-type wafer with p-stop (the orange curve in fig. 23) presumably represents the phenomenon described in section 3.2 that inversion charge is injected into the substrate and, thus, the obtained curve is above the true curve in the inversion region.

Therefore, this device was then also measured with twice the delay time and with reversed ramp direction of the gate voltage. Further, the frequency was increased and tested for different values and the stepsize was reduced, which not only yields a better resolution of the curve, but also a smaller current flowing at each step of the voltage ramp.

The so measured curves are shown in fig. 24 and the therefore used parameters are

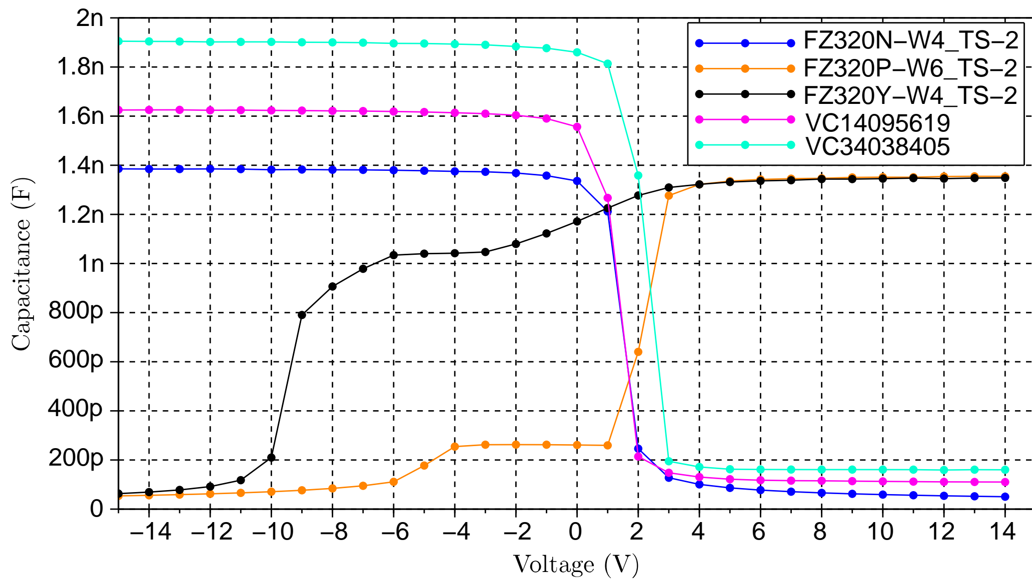


Figure 23: CV-characteristics for the n-type MOS (blue, pink and turquoise) and the p-type MOS with p-stop (yellow) and p-spray (black). Here, the gate voltage was varied from minus to plus for all wafer types.

SMU	
V_{min}	+15 V
V_{max}	−15 V
Stepsize	−0.5 V
Compliance	10 μA
Wait	1000 ms / 2000 ms
LCR initialisation	
Voltage level	5 mV
Current level	0
Frequency of AC signal	10 kHz

Table 6: Parameters for the CV-MOS-measurement of the p-type wafers with reversed ramp direction of the gate voltage.

listed in table 6. One can see, that the grater *Wait*-value only widens the step, but the ramp direction is crucial for the shape of the curve. The true value is somewhere in between the curves of the two ramp directions. However, the capacitance drop of depletion is exactly the same and so, for the flatband voltage or its shift between the different samples, the ramp direction is insignificant.

For the MOS of the p-type wafer with p-spray, the same remeasurements were done as for that with p-stop, and they can be seen in fig. 25. In this case, however, it is not clear whether it is the same effect or some other strange behaviour of the p-spray layer. It may be that the junction of the differently doped p-spray layer and the bulk material causes the second step noticeable in the CV-characteristic (and it is also not clear where to take V_{fb}).

4.4 IV-characteristics of GCDs

The gate controlled diodes have to be connected to two SMUs, the first SMU (K237) provides the constant bias voltage V_{bias}, and the SMU2 (K2410) provides the gate voltage V_{gate} that is varied during the measurement. According to their purpose of use, the SMUs are also called *Bias-SMU* and *Gate-SMU*, respectively. The Bias-SMU also measures the current that flows between the implant and the backplane (BP). For the following measurements, it was connected with its HI-terminal to the implant strips and with its LO-terminal to the backplane, which was grounded. The Gate-SMU was connected with its HI-terminal to the gate strips and with its LO-terminal also to the grounded backplane.

V_{gate} was varied between −15 V and +10 V for n-type and −10 V and +15 V for p-type and the constant V_{bias} was set to −5 V for n-type and +5 V for p-type GCDs, respectively. The measurements were controlled with the program 'GCD_IV_nptype_changed.vi' and all the parameters are listed in table 7.

The results of the IV-characteristics can be seen in fig. 26 and 27. The characteristic of the GCD of the n-type half moon of HPK is in good agreement with the ideal curve

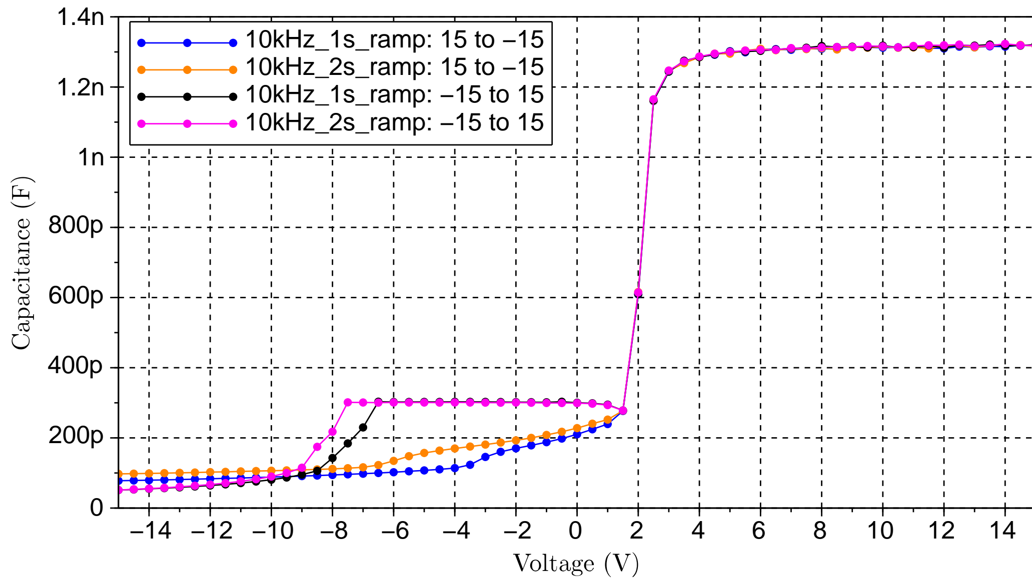


Figure 24: CV-curves of the p-type MOS with p-stop with different ramp directions and waiting times of 1 s and 2 s, respectively.

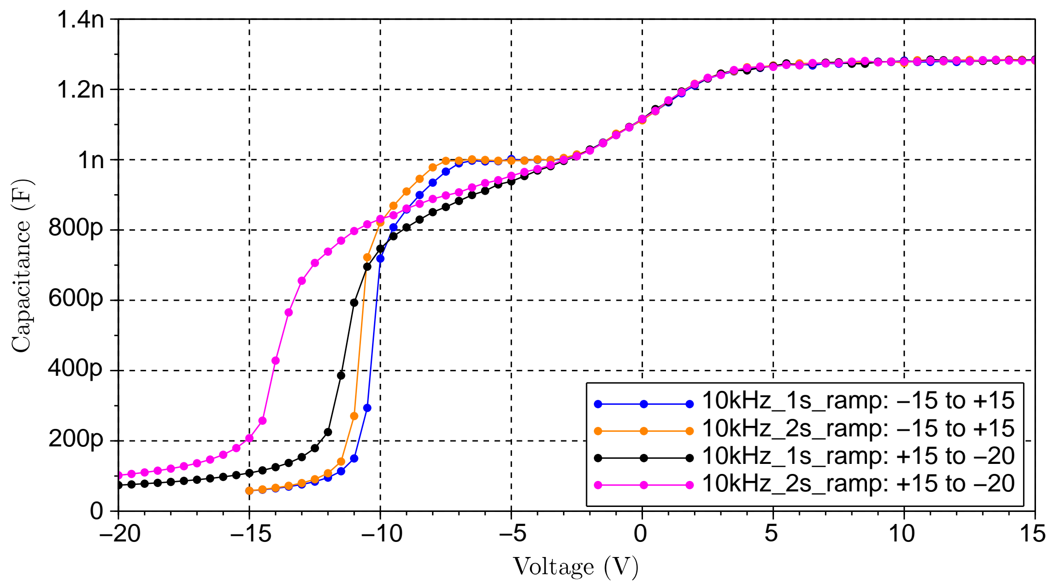


Figure 25: CV-curves of the p-type MOS with p-spray with different ramp directions and waiting times of 1 s and 2 s, respectively.

SMU (K237)	
V_{bias}	± 5 V
Compliance	10 μA
Wait	1000 ms
SMU2 (K2410)	
V_{start}	-15 V / -10 V
V_{max}	$+10$ V / $+15$ V
Stepsize	0.2 V / 0.1 V
Compliance	10 μA

Table 7: Parameters for the IV-GCD-measurement.

of fig. 15 (in sec. 3.3). It shows a distinctive step-shape and a surface current I_{surf} of $\sim$ 80 pA. The characteristic of the GCD of the p-type HM with p-stop is mirrored at both axes, but has the same shape and the absolute value of the surface current is nearly identical with $I_{surf} \approx -70$ pA. The resulting curve of the GCD of the p-type HM with p-spray is similar to that with p-stop and the current levels have the same height ($I_{surf} \approx -60$ pA), however, the width of the step is much broader. This may again be some strange effect of the p-spray layer, because here, also the estimation, that the width of the step should approximately equal the bias voltage, is not valid.

The curves of the GCDs of the Infineon wafers (fig. 27) are rather odd. That of run 1 seems to have a very high bulk-generation current $I_{bulk,\ MOS}$ (compare fig. 15 in sec. 3.3), but even more strange is the fact that the current level on the left side of the step is higher than that on the right. Nevertheless, one can extract a surface current I_{surf} of $\sim$ 45 pA. That of run 4, however, doesn't look like an usual GCD-characteristic. The current levels on either side of the step are very unequal and the curve in the depletion-region is curved in such a way that one can not identify a step on the left side. Moreover, the current is one order of magnitude higher than that of the reference wafers. This also causes a much higher I_{surf}. However, at the right side the step is $\sim$ 300 pA high and at the left the height is at least 1 nA, while at all the other wafers the steps at the left and right side have approximately the same height.

Therefore, more measurements were done, with reversed direction of the gate voltage ramp and with different ramp rates (up to a stepsize of 50 mV and a waiting time of 10 s), but neither of it had any effect on the curve. Also other wafers from that run were measured, but although the curves were slightly different, the shape was the same. A variation of the bias voltage only affected the width of the region of depletion, as expected, but not the shape of the curve. Even a change of the measurement circuit was tried out, but this only shifted the curve, due to changed reference potentials, and didn't change its shape. Thus, more detailed studies will be necessary to explain this curious behaviour.

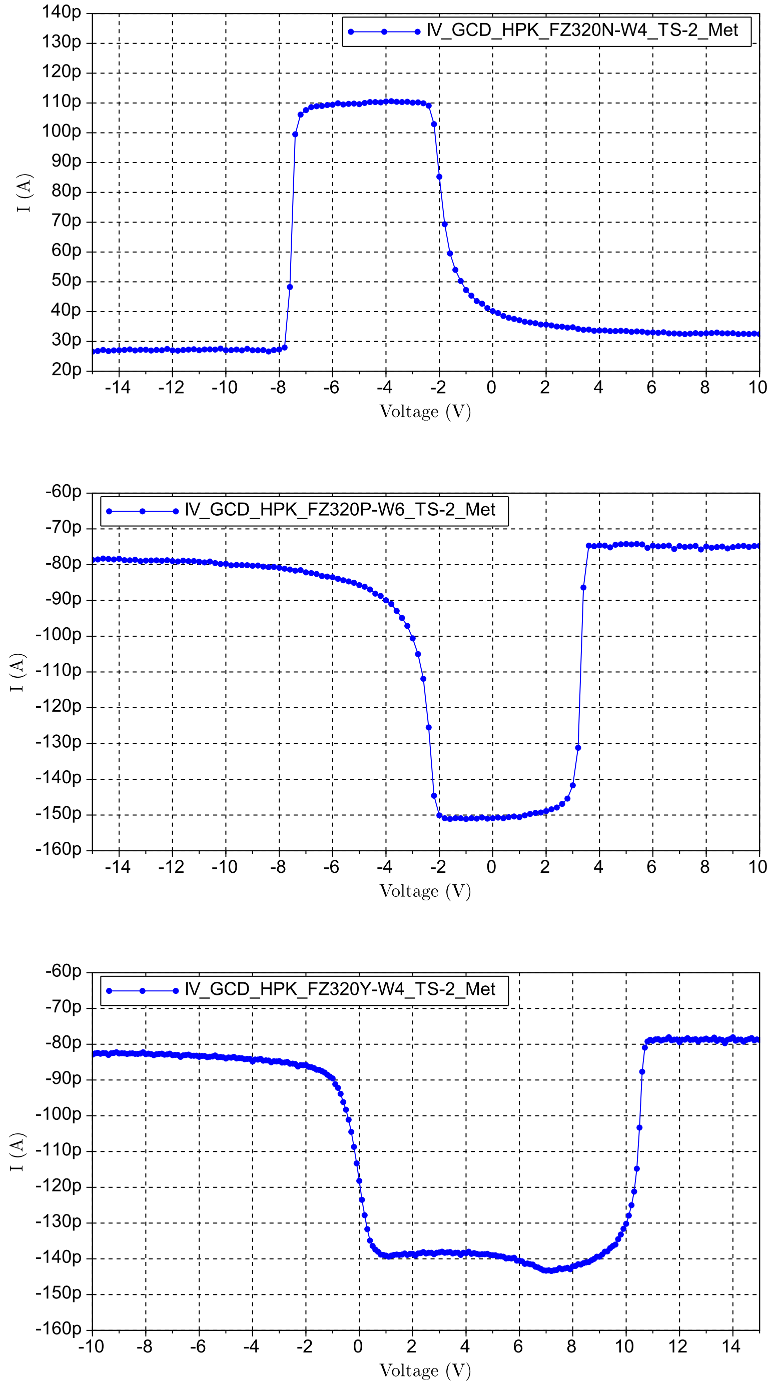
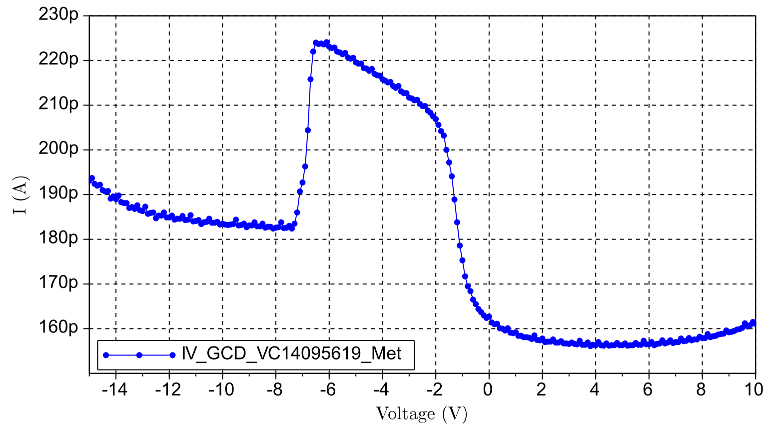


Figure 26: IV-characteristics of GCDs of HPK n-type (top), p-type with p-stop (middle) and p-type with p-spray (bottom) at bias voltages of $V_{\text{bias}} = -5\,\text{V}$ for n-type and $V_{\text{bias}} = +5\,\text{V}$ for p-type.



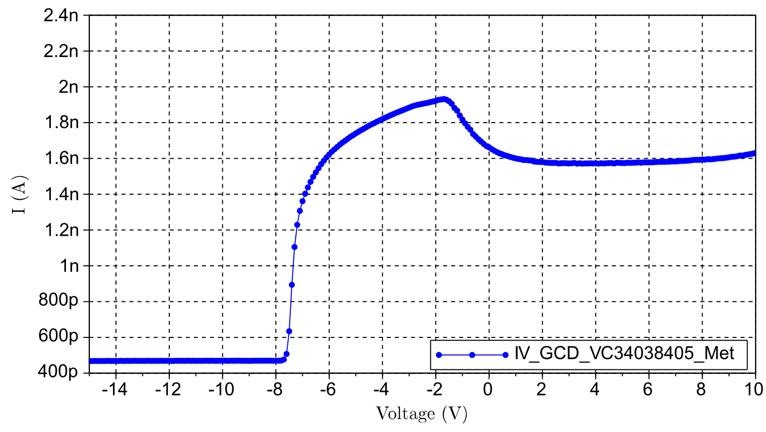


Figure 27: IV-characteristics of GCDs of Infineons run 1 (top) and 4 (bottom) at bias voltages of $V_{\mathrm{bias}} = -5\,\mathrm{V}$.

SMU	
V_{start}	0 V
V_{end}	±100 V
Voltage ramp style	'CEC voltage ramp'
Stepsize	1 V (for 0 – 20 V) and 5 V (for 20 – 100 V) / p-type with p-stop: 0.2 V (for 0 – 5 V)
Compliance	10 μA
Wait	1000 ms
LCR initialisation	
Voltage level	250 mV
Current level	0
Frequency of AC signal	1 MHz

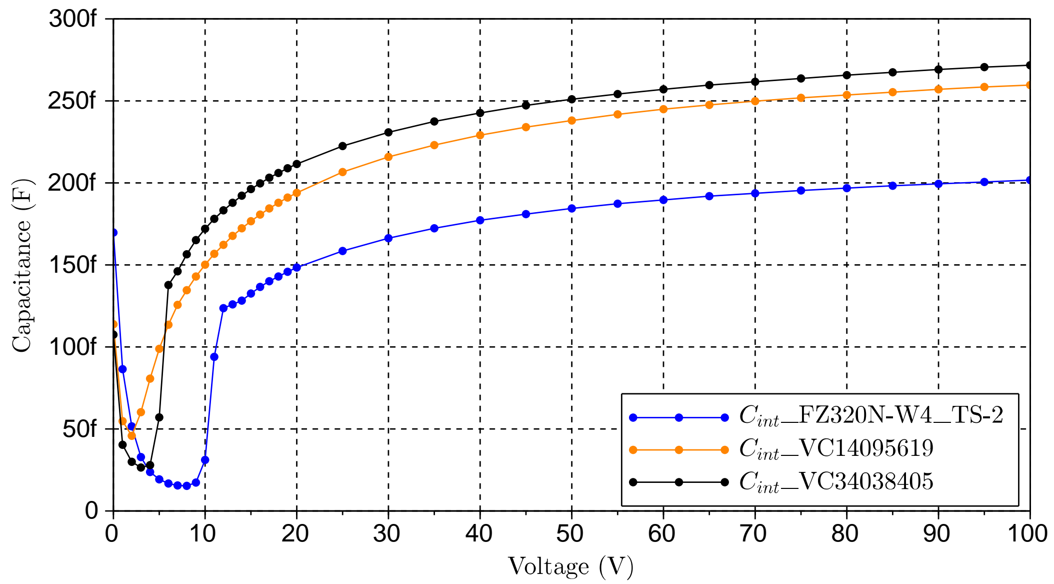
Table 8: Parameters for the C_{int}-measurement.

4.5 Interstrip capacitance C_{int}

For the measurement of the interstrip capacitance, the CAP-TS-AC structure was connected to the LCR-meter via the decoupling box, with the H-Dut-exit to the middlemost strip and the L-Dut-exit to its two adjacent strips. The SMU was connected with the HI-terminal to the backplane and with the grounded LO-terminal to the bias ring. The capacitance was then measured while the bias voltage was ramped from 0 to 100 V (+100 V for n-type and −100 V for p-type). In the programs used for these measurements, the 'CEC voltage ramp' was selected and modified, so that, up to $|V_{bias}| = 20$ V, there was measured in steps of 1 V, to ensure that the deviations in the small voltage range are not due to inaccuracies in the measurement resolution. For $|V_{bias}| >$ 20 V the stepsize was 5 V. The used programs were 'CINT_ntype_rampslow.vi' and 'CINT_ptype_rampslow.vi' for n- and p-type, respectively. For the p-type with p-stop 'CINT_ptype_rampveryslow.vi' was used, where the stepsize between $0 < |V_{bias}| < 5$ V was reduced to 0.2 V. All parameters are listed in table 8. The results were divided by the strip length, which was 3.475 cm for HPK and 3.521 cm for Infineon, and plotted in fig. 28. As mentioned in section 3.4, the values in the range of small bias voltages are variable, but the capacitance stays more or less constant for $|V_{bias}| \geq 20$ V.

4.6 Interstrip resistance R_{int}

For the interstrip resistance measurement, the SMU was connected to the middlemost strip of the CAP-TS-DC structure with the HI-terminal and with the LO-terminal to its two adjacent strips, which were grounded. The SMU2 (K2410) was used to apply the bias voltage between the backplane (HI) and the bias ring (ground). The bias voltage was then ramped from 0 to 200 V (+200 V for n-type and −200 V for p-type) in steps of 10 V. At each bias voltage step, a small voltage ramp was applied with the SMU (from −2 to 2 V in steps of 0.5 V) and the current was measured. From these IV curves,



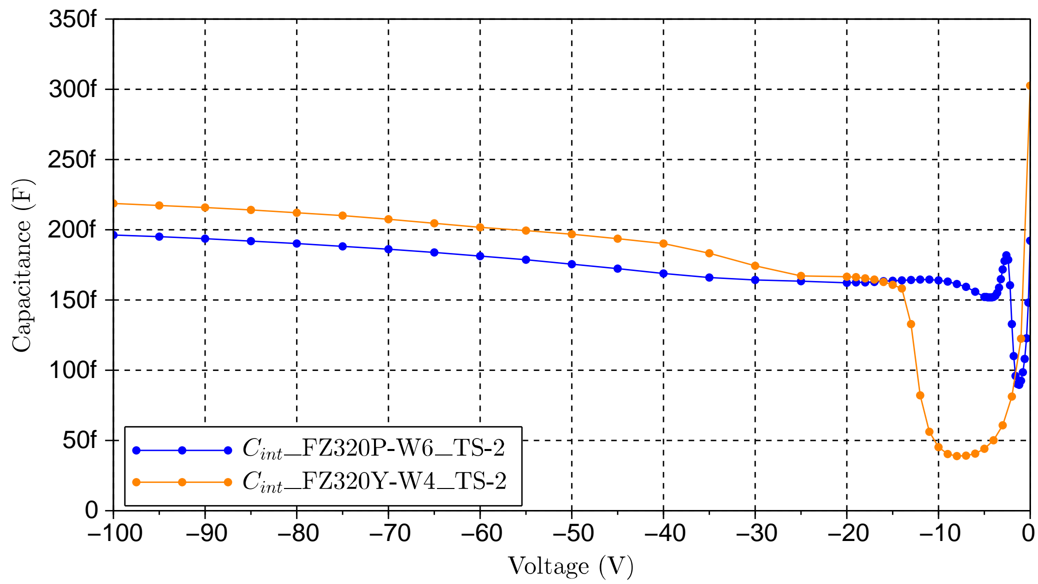


Figure 28: Interstrip capacitances for n-type (top) and p-type (bottom) structures (per cm strip length).

SMU (K237)	
U_{min}	$-2\,\text{V}$
U_{max}	$+2\,\text{V}$
Compliance	$10\,\mu\text{A}$
Stepsize	$0.5\,\text{V}$
SMU2 (K2410)	
V_{start}	$0\,\text{V}$
V_{max}	$\pm 200\,\text{V}$
Stepsize	$10\,\text{V}$
Compliance	$10\,\mu\text{A}$
Wait	$1000\,\text{ms}$

Table 9: Parameters for the R_{int}-measurement.

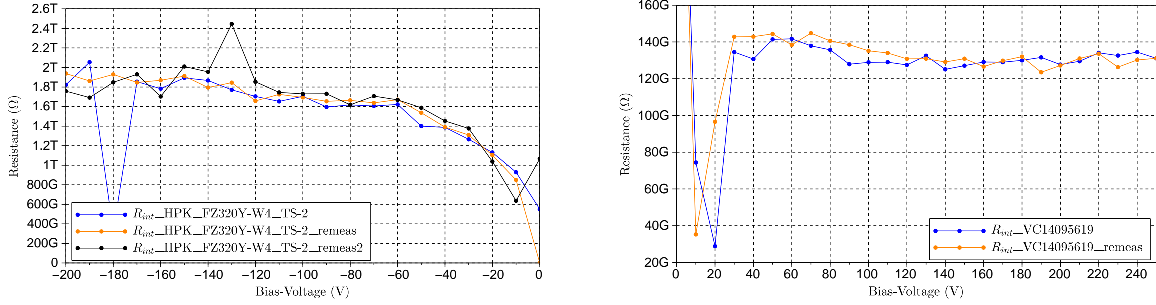


Figure 29: Interstrip resistances of the p-type wafer with p-spray (left) and the n-type wafer from Infineons run 1 (right side).

the resistance values were determined as the slopes of linear fits to these curves. This was done with the programs 'RINT_ntype.vi' and 'RINT_ptype.vi' for n- and p-type, respectively, and the parameters listed in table 9.

The problem with these measurements was, however, that in most cases the fits were not linear, and so the resistance values were very erratic and did not yield an useful curve. Only the IV ramps at the p-type wafer with p-spray and the wafer from Infineons run 1 were sufficiently linear that some useful resistance values were obtained, which are plotted in fig. 28. Apart from the first few bias voltage steps, where the voltage ramp probably influences the depletion field (as mentioned in section 3.5), the resistance value stays tolerably constant. However, one can see that the several remeasurements are not wholly identical and show many outliers. Nevertheless, one finds out that the resistance value of the Infineon wafer is more than one order of magnitude lower than that of the HPK wafer, but still it is more than two orders of magnitude higher than the specification of $R_{\text{int}} > 1\,\text{G}\Omega$ [7].

Though, to ensure reliable results of this measurement, there should be checked the

SMU (K237)	
V_{start}	0 V
Wait	500 ms
Compliance	10 / 20 / 30 / 50 / 100 μA
V_{stop} (Poly-Si)	10 V
Stepsize (Poly-Si)	1 V
V_{stop} (Metal)	0.01 V
Stepsize (Metal)	0.001 V
V_{stop} (Implant n- / p-type)	10 V / 5 V
Stepsize (Implant n- / p-type)	1 V / 0.5 V
SMU2 (K2410)	
V_{bias}	180 V / −175 V / −150 V / 300 V
Compliance	10 μA

Table 10: Parameters for the sheet-measurements.

quality of the fits in the Labview program and the measurement should be enhanced to yield more linear IV curves.

4.7 Sheet resistances

The sheet resistances were measured on the sheet structures that have some meander shaped structures of different width and length for each conductive layer. The resistance value was extracted, as at the R_{int}-measurement, with a small voltage ramp and a fit of the resulting IV curve. Therefore, the SMU was connected with its HI-terminal to one end of such a meander, and with the grounded LO-terminal to the other end. With the SMU2 (K2410), a bias voltage was applied between the backplane (HI) and the bias ring (ground). However, the problem was that the HPK half moons had no bias ring around the sheet structures. Hence, it was tried to bias these structures via the implant meanders, as they were the single contacts to the implant, but with limited success. The structure of the n-type half moon of HPK could only be biased with 180 V because at higher voltages the SMU2 would go into compliance. The p-type structure with p-stop had a breakthrough at −178 V and, therefore, was only biased with −175 V. The p-type structure with p-spray could only be biased with −150 V for the same reason. All structures with bias ring were biased with 300 V. The measurements were controlled with the program 'Rsheet_IVmeasurement.vi', however, this program had the disadvantage of having to set the voltage range of the IV ramp. Naturally, this is very different between the layers, as their resistances are very different, but the compliance value of the SMU for the current shall be (roughly) the same. Therefore, the values of the voltage ramps are listed for all layers separately in table 10 with all the other parameters.

The sheet structures were all measured with and without bias voltage and the results were compared. The edge implants and p-stop and p-spray implants on the HPK wafer, however, could not be biased via the strip implant structure. There must have flowed

some leakage currents that drove the SMU2 into compliance at voltages less than 1 V. Though, this problem could be solved by changing the measurement circuit, so that the SMU2 was floating and not connected to ground, as the other SMU was.

Moreover, there was also measured a CMS-W7A structure from the CMS 6inch cut offs[17], because this structure has a bias ring and, thus, could be biased with 300 V. This structure is of n-type and has, as the sheet structures from Infineon, no edge implant meander.

To increase the measurement accuracy, the meander were measured at least two times and the mean values were calculated. Then, the results with- and without bias voltage were compared, which led to the following conclusion: The metal layer shows identical performance, the polysilicon layer very small differences in the range of a few per cent, and for the implants, as expected, the differences were larger. For the p-type implants they lay in the range of $15 - 20\,\%$, for the n-type implants of HPK at $\sim 45\,\%$,

and at the Infineon structures they were small[18]. However, for the HPK structures of the CMS 6inch cut offs, surprisingly, there was no difference between the measurements with and without bias voltage.

To calculate the sheet resistances in $\Omega/sq.$, the square numbers are needed. They were obtained from the following references: The square numbers of the three HPK half-moons (FZ320N_W4_TS-2, FZ320P_W6_TS-2 and FZ320Y_W4_TS-2) were taken from [17], table A.2 in appendix A.2.2., those of the Infineon HMs were taken from the layout files (they are labeled directly on the structures and can also be read under the microscope) and those of the CMS-W7A HM had to be measured directly out of the structure under the microscope.

However, the corner squares of the meander cannot be counted as full squares, because in the inner curve the current has a shorter path to take and thus a lower resistance. Therefore, the current density is distributed inhomogeneously, as illustrated in fig. 30. This is explained in [22] and was calculated by [23]. As a result of this, when the current takes a 90-degree turn, the corner square only counts as 0.56 squares for the resistance.

Hence, from the square numbers, there was subtracted $0.44 \cdot no.\,of\ corners$ to obtain the effective square numbers relevant for the sheet resistances R_{sheet}. This is listed in tab. 11.

Now, the sheet resistances in $\Omega/sq.$, that are listed in tab. 12, were calculated the following way: First, the mean values of all measurements of the meander with bias voltage were taken, then, they were multiplied with the corresponding square numbers, and then, the mean value over all meander of one layer was taken. Beside these mean values of one wafer, also the mean values over all three HPK-wafers and over the two Infineon-wafers are listed.

Later, new drivers for the SMU were written to apply a current and measure the voltage. They were used in the new program 'Rsheet_VvsImeasurement_withBiasRamp.vi', which led to the big advantage that a current ramp can be applied (from 0 to 10 μA in

[17] There was used the structure with serial no. 3022134190018 and lot no. SWB63642.

[18] However, there was the problem that most IV ramps without bias voltage were nonlinear, only one structure yielded a reasonable value, here the difference was $\sim 5\,\%$, but due to the little statistics this is not very significant.

Layer	HPK			Infineon			CMS-W7A		
	Square no. from [17]	No. of corners	Sq.no. relevant for R_{sheet}	Square no. from layout-file	No. of corners	Sq.no. relevant for R_{sheet}	Sq. no. measured under microscope	No. of corners	Sq.no. relevant for R_{sheet}
Poly-Si 1	-	-	-	500	74	467.44	2850	55	2826
Poly-Si 2	-	-	-	500	74	467.44	2850	55	2826
Poly-Si 3	453	80	417.8	500	112	450.72	2850	55	2826
Poly-Si 4	156	40	138.4	500	144	436.64	-	-	-
Poly-Si 5	306	54	282.24	500	144	436.64	-	-	-
Poly-Si 6	606	56	581.36	-	-	-	-	-	-
Metal 1	4916	18	4908.1	10000	40	9982.4	62	4	60
Metal 2	13758	26	13747	10000	20	9991.4	182	4	180
Metal 3	-	-	-	-	-	-	447	4	445
Implant 1 (all types)	2940	10	2935.6	5000	20	4991.2	55	4	53
Implant 2	5870	10	5865.6	5000	8	4996.5	132	4	130
Implant 3	-	-	-	-	-	-	246	4	244

Table 11: Square numbers for the sheet resistances R_{sheet}.

Layer	HPK_FZ320N-W4_TS-2	HPK_FZ320P-W6_TS-2	HPK_FZ320Y-W4_TS-2	Mean value of HPK wafers	Infineon_VC14095619	Infineon_VC34038405	Mean value of Infineon	CMS-W7A
Poly-Si	3437	3399	3331	3389	1130	4227	(2678)	541
Metal	0.029	0.027	0.03	0.029	0.04	0.023	0.032	0.078
p^+ in n	105	-	-		367	341	354	448
n^+ in n	116	-	-		-	-		-
n^+ in p	-	28	27	28	-	-		-
p^+ in p	-	17	16	17	-	-		-
p-stop	-	29	-		-	-		-
p-spray	-	-	29		-	-		-

Table 12: Sheet resistances in Ω/sq. For the values listed here, the mean values of all measurements of the meander with bias voltage were taken, then, they were multiplied with the corresponding square numbers, and then, the mean value over all meander of one layer was taken.

SMU (K237)	
C_{start}	$0\,\mu$A
C_{stop}	$10\,\mu$A
Stepsize	$1\,\mu$A
Wait	500 ms
Compliance	1000 V
SMU2 (K2410)	
$V_{\text{bias, start}}$	0 V / 0 V
$V_{\text{bias, stop}}$	200 V / 10 V
Stepsize	10 V / 1 V
Compliance	$10\,\mu$A

Table 13: Parameters for the sheet-measurements with V vs I ramp and bias voltage ramp.

steps of $1\,\mu$A) that is the same for each layer. In exchange, the voltage depends on the resistance of the layer, but this is very unproblematic, as the voltage compliance can be set up to 1000 V, since the current is limited due to the stop-value of the current ramp. Furthermore, this program can perform a bias voltage ramp to measure the resistance at each bias voltage step and, thus, produce a resistance versus bias voltage characteristic. This was done for several structures (with the same measurement circuit as explained above and the parameters in tab. 13) and could confirm the previous measurements. In fig. 31, for example, one can see that the resistance of the HPK n-type structures varies over a great range in the first view voltage steps, but for the p-type structures this was much less. And the absolute value of the resistance agrees with 371 kΩ exactly with the previous measured. It also reveals that it is not necessary to bias the structures with 300 V, because for $V_{\text{bias}} \gtrsim 50$ V the resistance stays constant. Therefore, it doesn't matter at which bias voltage the previous measurements were performed, since they were all much greater than 50 V.

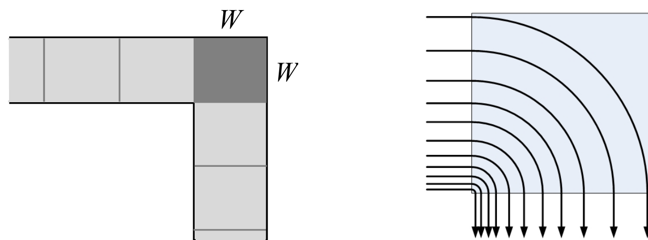


Figure 30: Left: Square counting, right: Current flow around a corner, the spacing of the arrows illustrates the current density [22].

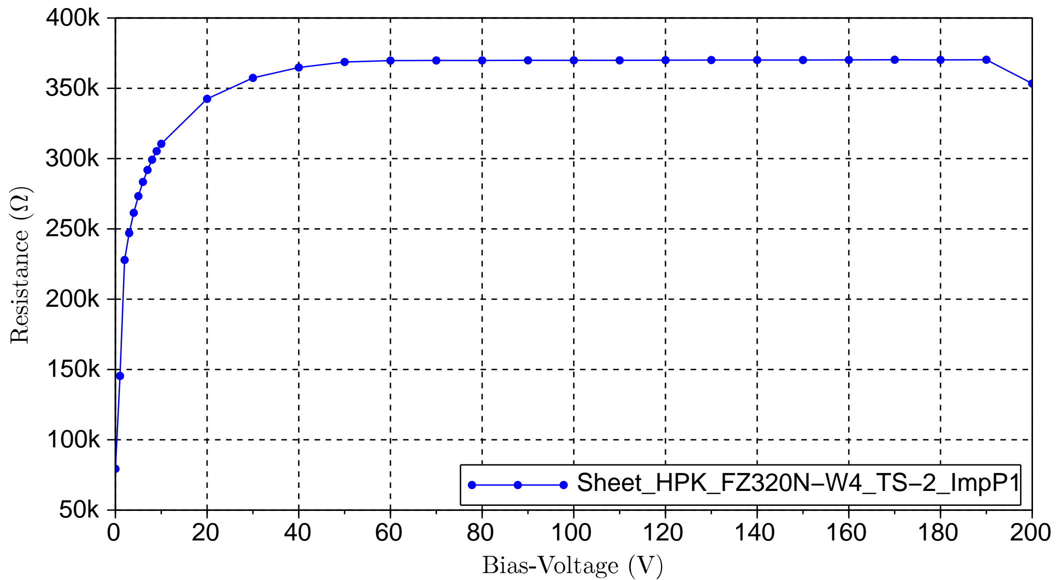


Figure 31: Resistance vs. bias voltage curve of a p-implant structure of HPK_FZ320N-W4_TS-2.

5 Detailed investigation of MOS structures

In the following section, more detailed studies of MOS structures are presented. They were carried out, amongst others, on MOS from Infineons run 3.5 and 4 with additional nitride-layer and with several different passivations. Also MOS from Infineons run 5 were analysed, which are n-type but have different variations of an additional n-spray layer. Furthermore, charge up effects were examined and tried to provoke on various MOS structures.

5.1 MOS with nitride-layer and several different passivations

In addition to the normal MOS structure, at Infineons run 3.5 and 4, a further MOS with an additional nitride-layer was available. This nitride-layer is placed above the oxide-layer under the gate-metal and is normally used to increase the stability against breakthroughs.

Moreover, Infineon tested several different compositions of passivation and one sawing processes without- and another with CO_2-bubbler[19]. In contrast to run 3.5, run 4 had a new mask layout, but this didn't affect the test structures. All these properties are listed in tab. 14 for all available wafers.

For these measurements, the LCR-meter and the SMU were connected in the same

[19]The CO_2-bubbler shall reduce a possible charge generation during the sawing process.

wafer	run 4	run 3.5	800 nm SNIT	400 nm SNIT	800 nm SNIT + 140 nm aSi	800 nm SNIT + 400 nm PSG	400 nm SiO_2	sawed with CO_2-bubbler	sawed without CO_2
4	x		x						x
5	x			x				x	
6	x			x				x	
7	x						x	x	
11	x				x			x	
18		x	x					x	
19		x	x						x
20		x			x			x	
21		x			x			x	
22		x			x				x
23		x				x		x	
24		x				x		x	
25		x				x			x

Table 14: List of all available wafers with wafer number, run, passivation and sawing process. SNIT is an acronym for 'Schutz-Nitrid' and means protective nitride, aSi means amorphous silicon and PSG stands for phosphorus-silicate-glass.

SMU	
V_{min}	$-5\,\mathrm{V}$
V_{max}	$+5\,\mathrm{V}$
Stepsize	$0.2\,\mathrm{V}$
Compliance	$10\,\mu\mathrm{A}$
Wait	$1000\,\mathrm{ms}$
LCR initialisation	
Voltage level	$250\,\mathrm{mV}$
Current level	0
Frequency of AC signal	$1\,\mathrm{kHz}$

Table 15: Parameters for the CV-measurement of the MOS with nitride-layer.

way as for the previous MOS-measurements (see circuit diagram in fig. 18 in sec. 4.2). The CV-curve was measured with the program 'DiodeMeasurement.exe'[20] using the parameters listed in tab. 15.

The results show the difference between the normal MOS structures and those with additional nitride-layer. In the region of accumulation the curves of the first ones are higher than those of the latter, as shown in fig. 32. Obviously, the nitride-layer-MOS has a lower oxide capacitance C_{ox} due to the larger thickness, which derives from the additional nitride-layer (and the dependency of $C_{\mathrm{ox}} \propto \frac{1}{d}$ of eq. (6)). Moreover, the flatband voltages differ in a range of approximately $1.5\,\mathrm{V}$, which is more than the deviation of less than $0.5\,\mathrm{V}$ between the two curves of the normal MOS of the different half moons of the same wafer. This difference in the flatband voltages may be there, because the additional nitride-layer accumulates negative charges that influence V_{fb}-shift, as proposed in [19] for MOSFET and DEPFET structures.

The CV-curves of the normal MOS with different compositions of passivation are very similar, as can be seen in fig. 33. There are only very small differences between the MOS of run 3.5 and those of run 4: The oxide capacitances of the latter are slightly higher ($\Delta C_{\mathrm{ox}} \lesssim 100\,\mathrm{pA}$) and therefore the oxide thickness is somewhat smaller. Furthermore, the flatband voltages of the latter are shifted a bit further to more positive voltages (around $1.75 - 2\,\mathrm{V}$) compared to the first ones (which are around $1.25 - 1.5\,\mathrm{V}$). So for the normal MOS, the different types of passivation have no significant influence on the CV-characteristics. This was to be expected, as virtually the whole gate is free of passivation and only the rim regions of the metal are overlapped with passivation by a few micrometer.

However, the MOS with additional nitride-layer show some strange results, shown in fig. 34. Most of the curves are very identical and have nearly the same flatband voltage ($V_{\mathrm{fb}} \approx 0.5\,\mathrm{V}$), but four wafers show a differently shaped curve. They have not just one sharp decline with constant slope, but first descend with steadily decreasing slope until the curve is almost flat and then have a kink and fall with steep slope to the inversion

[20] V 7.0.5, Wolfgang Brandner, HEPHY.

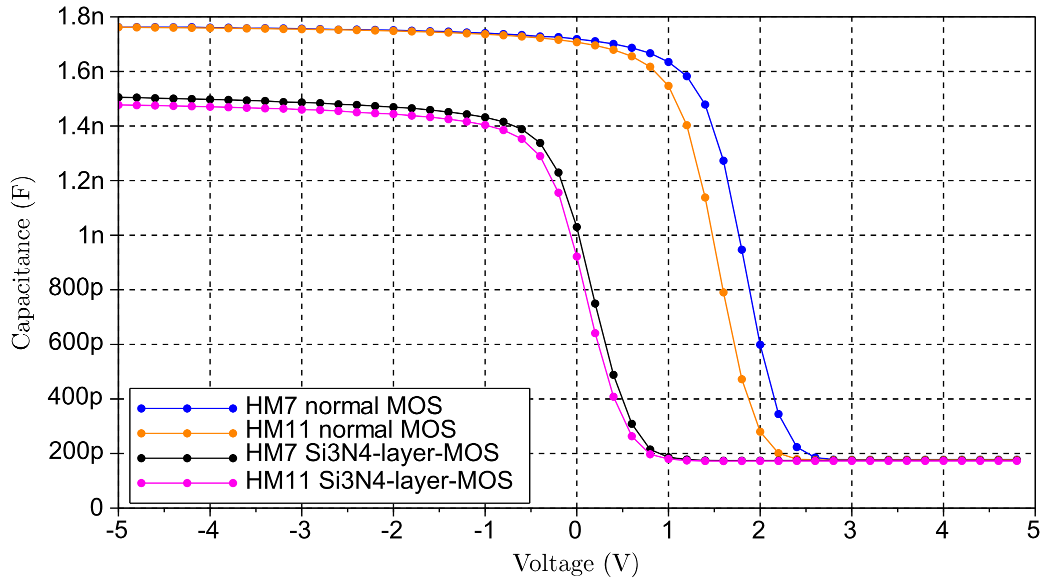


Figure 32: Difference of MOS with additional nitride-layer and normal MOS of both half moons of the structure VC34038407.

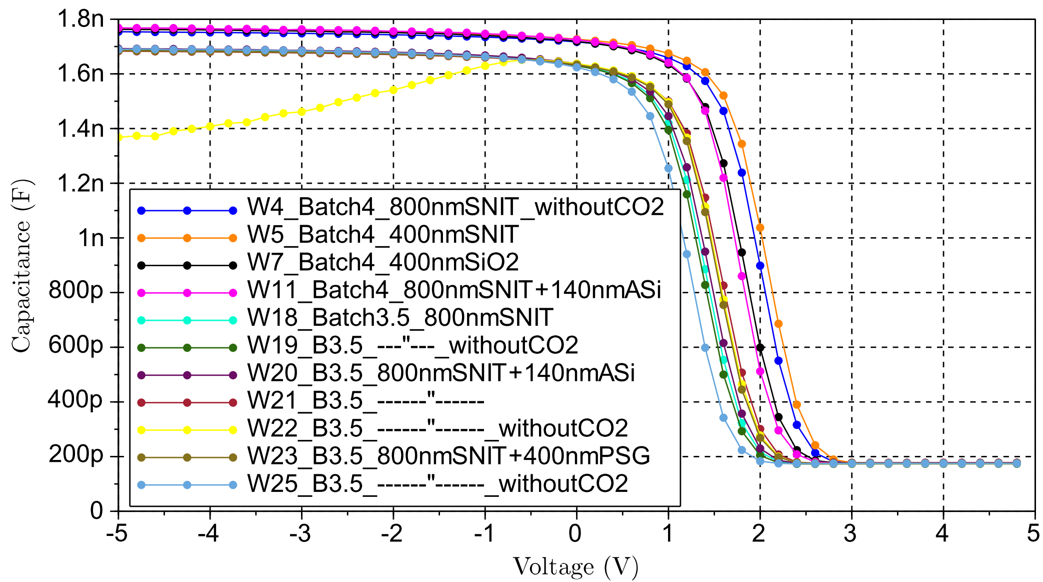


Figure 33: CV-curves of normal MOS with different variations of passivation.

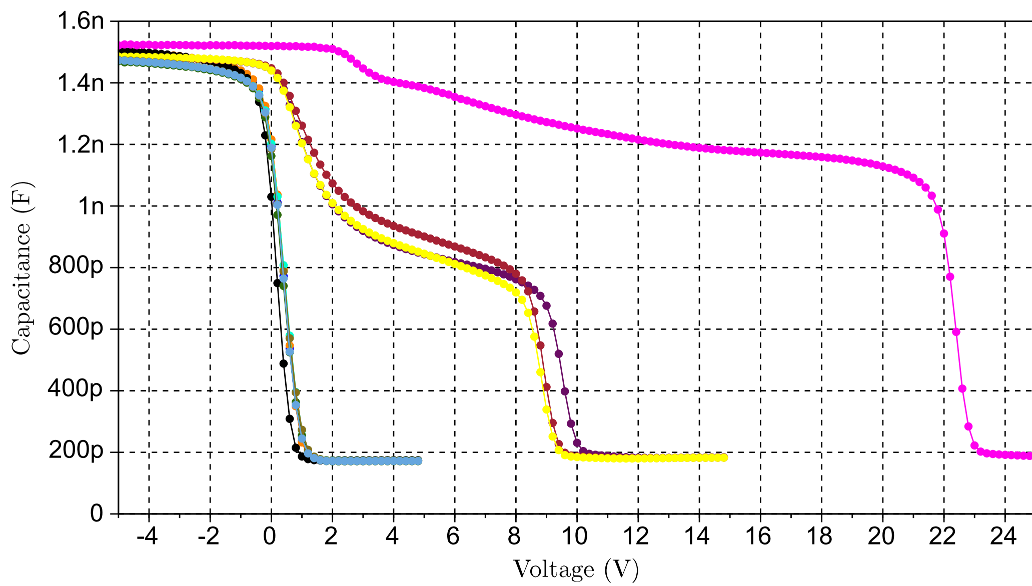


Figure 34: CV-curves of nitride-layer-MOS with different variations of passivation (the most right curve (pink) is from wafer 11 (run 4) with 800 nm SNIT + 140 nm aSi, the middle three curves are from wafer 20 (purple), 21 (wine red) and 22 (yellow), all from run 3.5 and also with 800 nm SNIT + 140 nm aSi, W22 was sawed without CO_2-bubbler; for a full legend see fig. 33).

level (three of them at 9 or 9.5 V and one at 22.5 V[21]). These four wafers are all of the passivation type SNIT+aSi. This is very unexpected, because the passivation should have no relevance since most of the device is free of passivation (as explained above). Moreover, it is remarkable that the nitride-layer-MOS behave so different compared to the normal MOS of the very same half moons with the same passivation.

As several remeasurements yielded the same results, some more were performed with other frequencies (10 kHz and 100 kHz) and with reversed ramp direction of the gate voltage (from plus to minus). However, this didn't change the curves at all, so it is probably not the same effect as the one that was seen at the p-type MOS with p-spray (fig. 25 in sec. 4.3).

Another possible explanation is that charges might be induced in the passivation around the gate by the sawing process, as it appeared on some sensors of Infineon (i.e. see [12] sec. 7.3.1). The half moons are sawn at one single edge and the MOS with the nitride-layer is located adjacently to this edge while the normal MOS is located more distantly to it. This could explain a difference between these two MOS, and as charge is suspected to be induced in the passivation, the type of passivation might play a role.

In [12] the charge accumulation was removed by a bathing procedure, also described in [20]. Therefore, the device was singly put into deionised water for some time. The water should provide a better dissipation of static charges located at the surface and thus remove or diminish a charge accumulation.

So the half moons of all four affected wafers were put into deionised water for 24 hours and remeasured after this bathing procedure. However, the CV-curves did not change due to this treatment.

Later in section 5.3, it was tried to provoke a charge accumulation in MOS devices and its behaviour was studied.

The difference in the sawing process, obviously, did not lead to any noticeable differences in the MOS-characteristics, as can be seen in fig. 33 and 34.

5.2 N-type MOS with n-spray layer

Normally, on n-type sensors no n-spray is necessary in contrast to p-spray on p-type sensors. Nevertheless, at Infineons run 5 different n-spray layers were tested. At the previous runs of Infineon, however, charge accumulations occurred on the sensors, which are treated in [12]. Hence, it was tried to prevent these charge accumulations by adding an n-spray layer over the whole wafer.

Therefore, wafers with three different n-spray layers (A, B and 2B) and without n-spray (denoted with '0' in the figures) were produced. For each n-spray type, three wafers in two different thicknesses were manufactured. One of the respective wafers of the same thickness was sawn without- while the others were sawn with CO2-bubbler. So in total, this run should consist of 12 wafers, however, wafer 1 got broken during the manufacturing process and thus was not available for measurements. In addition, this run also had MOS structures with additional nitride-layer, like the previous one.

[21] For this reason these structures were of course measured up to $V_{\mathrm{max}} = 15\,\mathrm{V}$ and $25\,\mathrm{V}$, respectively.

SMU	
V_{min}	$-10\,\text{V}$ / $-15\,\text{V}$
V_{max}	$+5\,\text{V}$
Stepsize	0.2 V
Compliance	1 mA
Wait	1000 ms
LCR initialisation	
Voltage level	250 mV
Current level	0
Frequency of AC signal	10 kHz

Table 16: Parameters for the CV-measurement of the MOS with n-spray layer.

The measurements were controlled with the program 'DiodeMeasurement.exe' using the parameters listed in tab. 16. However, a different measurement circuit was used, where the high voltage lies at the gate and the backplane at ground potential (for explanation see sec. 5.3 and the circuit diagram in fig. 37). Therefore, the resulting CV-characteristics are mirrored to them of the previous sections. For n-type MOS, the region of inversion is now on the left side (at negative gate voltages) and that of accumulation on the right side (at positive gate voltages).

As the first two wafers (W2 and 3) didn't yield very feasible results, different frequencies (1 kHz, 10 kHz and 100 kHz), different waiting times (1 s, 2 s and 5 s) and different voltage levels (5 mV, 50 mV, 100 mV and 250 mV) were tested. The waiting times had no noticeable influence on the CV-characteristics, hence there was chosen $Wait = 1\,\text{s}$ for the subsequent measurements. Concerning the other parameters, the best results were obtained for those listed in tab. 16 (10 kHz and 250 mV).

Nonetheless, the results of the wafers 2 and 3 showed a step at a gate voltage of $-2\,\text{V}$ but only one of about 60 pF of height[22] and in a range between 200 and 300 pF. Moreover, the higher side of the curve was on the left side (at negative gate voltages), which was very unexpected using this measurement circuit. Thus, these two wafers were measured in a wider range (from $V_{\text{gate}} = -80\,\text{V}$ up to $+40\,\text{V}$), but the curves stayed constant and didn't show any other steps.

The other wafers, however, show very useful MOS-characteristics. The steps are of about 1.6 nF and 1.3 nF of height for the normal MOS (seen in fig. 35) and the nitride-layer-MOS (seen in fig. 36), respectively. This is in agreement with section 5.1 (e.g. fig. 32 but mirrored due to the changed measurement circuit). While the steps of the wafers with no n-spray are close to zero (at about $-2\,\text{V}$ for the normal MOS and $-0.5\,\text{V}$ for the nitride-layer-MOS), those of the wafers with n-spray are shifted to more negative gate voltages. For n-spray B, this shift is about 4 V (for the nitride-layer-MOS almost 5 V) and for n-spray 2B the shift is quite accurate twice as much.

Furthermore, the curves of the 200 μm thick normal MOS with n-spray B and without n-spray are slightly shifted left to that of the 300 μm thickness, which coincide almost

[22] Normally, the step of a CV-MOS-curve is several hundred pF high ($\sim 1.6\,\text{nF}$).

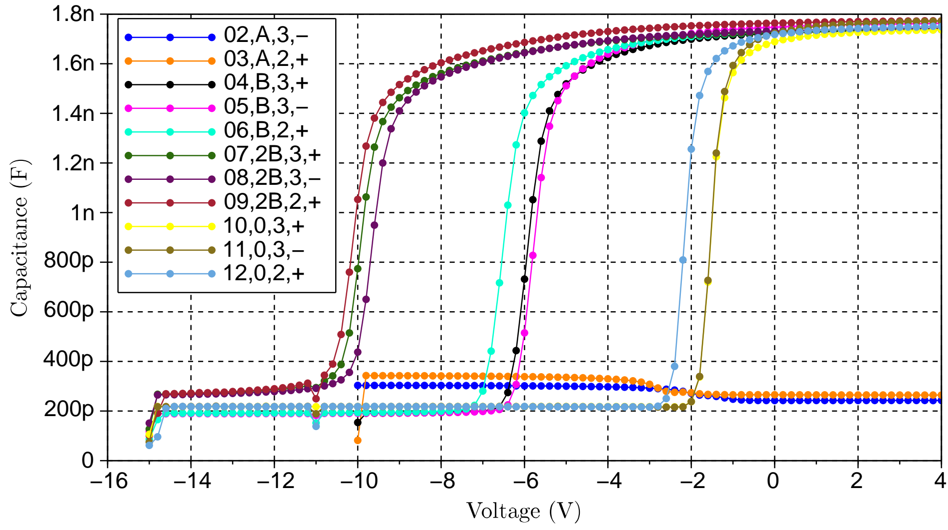


Figure 35: CV-curves of normal MOS with different n-spray layers. The legend denotes from left to right the wafer number (02-12), the type of n-spray (A, B or 2B; 0 means no n-spray), the thickness of 300 μm (3) or 200 μm (2), and whether the wafer was sawed with CO_2-bubbler (+) or without (-).

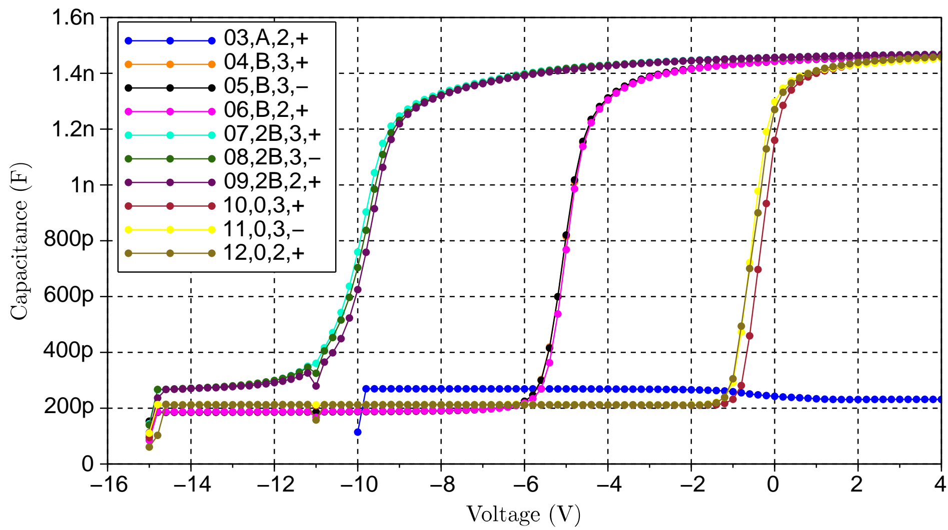


Figure 36: CV-curves of nitride-layer-MOS with different n-spray layers. The legend notation is the same as in fig. 35.

exactly. At the wafer with n-spray 2B, however, all curves are near each other and for the nitride-layer-MOS there is no influence of the thickness noticeable at all.

As the CV-characteristics of the wafers with n-spray B and 2B show very plausible behaviour, it is obvious that the layout with n-spray A is not usable, or at least destroys the characteristics of a MOS.

5.3 MOS long term charge up measurements

As briefly mentioned in the previous subsection (5.2), charge accumulations occurred on Infineon sensors that affect the electrical characterisations thereof (e.g. the single strip parameters). This was first observed in [4] and is described in detail in [12].

The aim of this subsection was to provoke charge accumulations on MOS test structures and to examine the consequential effects on the electrical characterisations of the MOS. Also the long term behaviour of the effects was examined and whether they could be diminished or erased by a bathing procedure, as described before in sec. 5.1.

To provoke a charge accumulation a (high) voltage was applied at the gate of the MOS for some time (HV-stress), as it was described in [21]. As a consequence, charges were introduced into the dielectric layer, which affect the CV-characteristic of the MOS.

First attempt of HV-stress on normal MOS. To compare Infineon and HPK, some normal MOS structures[23] were measured at the beginning of this survey, since they were available from both vendors. The measurements were carried out with the standard MOS-measurement circuit used in sec. 4.3 and drawn in fig. 18 (with HV at BP and ground at the pad). They were controlled with the program 'Diode_Measurement.exe' using the measurement parameters listed in tab. 17. The HV-stress was applied with the SMU2 (Keithley 2410), which was connected with an additional needle with the HI-output to the pad and the LO-output (ground) to the backplane. In this experiment the SMU2 was controlled manually. After the HV-stress the pad was (momentarily) connected to ground with a third needle, to allow possible remaining charges on the pad to flow off. This should prevent the LCR-meter from any abrupt discharge when connecting it to the structure.

The measurements were carried out in the following way: At first, two initial CV-characteristics were measured to ensure that the bias ramp itself doesn't influence the characteristic. Then, various HV-stresses were applied to the structures and immediately after every HV-stress a new CV-curve was measured. The structures and the respectively applied voltages are listed in tab. 18. The voltage of the HV-stress was ramped manually in steps of 10 V and applied for approximately[24] 30 s, 60 s or 300 s, respectively, as noted in tab. 18. The magnitude of the HV-stress was increased with every repetition until there was some kind of breakthrough that probably destroyed the MOS. After

[23] VC34038405 HM 7 and HM11 and VC34038411 HM 7 from Infineon and HPK-FZ200N-W1_TS-2. For a description see analogue structures in tab. 1

[24] From begin of upramp to begin of downramp, ramping needed up to approx. 7 seconds for −400 V. This inaccurate procedure suffices for qualitative results but was later implemented in the program to determine the time exactly.

SMU	
V_{min}	-5 V
V_{max}	$+10$ V
Stepsize	0.5 V
Compliance	10 μA
Wait	1000 ms
LCR initialisation	
Voltage level	250 mV
Current level	0
Frequency of AC signal	100 kHz

Table 17: Parameters for the first attempt of the long term charge up measurements of the normal MOS.

this breakthrough the inversion region of the MOS-curve wasn't constant anymore, but steadily decreasing. Furthermore, neither any greater negative nor any positive voltage could be applied without driving the SMU into compliance.

But all these HV-stresses did not deviate the CV-curves at all and so the measurement was revised, simplifying the measurement procedure.

HV-stress at nitride-layer-MOS with improved measurement circuit. For the subsequent examinations, only nitride-layer-MOS were used, as in [21] only such structures were treated with HV-stress. Consequently, only MOS from Infineon could be used, as from HPK no MOS with additional nitride-layer were available.

In order to to make the time of application exactly determinable, a control for the HV-stress was implemented to the Labview program[25]. Furthermore, the measurement circuit was changed. The idea was to measure the CV-characteristic immediately after the HV-stress, without contacting three different needles. Consequently, the momentarily grounding with the third needle was skipped [26]. Moreover, the HV-stress was intended to be applied with the same needle, which was used for the bias ramp of the CV-measurement. As the HV-stress has to be applied at the gate, therefore, the measurement circuit had to be changed the following way: The high voltage had to be applied at the gate and ground at the backplane. First, of course, it was tried to simply change the cables from needle and backplane. But as this drove the LCR-meter into overload immediately, the measurement circuit had to be rearranged another way. Thus, the HI-terminal of the SMU was connected with the HV-Low-terminal of the DCB and the LO-terminal of the SMU with the HV-in-terminal of the DCB. This resulted in the circuit diagram shown in fig. 37, where the high voltage was present at the L-Dut-terminal of the DCB and the H-Dut-terminal lay at ground-potential.

The changed circuit diagram leads to a mirrored CV-characteristic, where the region

[25] The enhanced program was saved as 'MOS_CV_nptype_afterHVstress.vi'.

[26] The pad was set to 0 V after the HV-stress and before ramping to the start voltage for the CV-measurement, anyway.

	Infineon (VC340384)			HPK-FZ200N		Nitride-layer-MOS (VC340384)	
	HM7 W5	HM7 W11	HM11 W5	W1 TS2		HM11 W5	HM7 W5
initial	2x	-	2x	2x	initial	2x	2x
−30 V	30 s			60 s	±10 V	30 s	60 s
−50 V	30 s			60 s	±20 V	30 s	60 s
−100 V	30 s			60 s	±30 V	30 s	60 s
−200 V	30 s			60 s	±40 V	-	60 s
−400 V	30 s			60 s	±40 V	-	120 s
−600 V	*			60 s	±40 V	-	300 s
−800 V				*	−40 V	-	600 s
+50 V		-	60 s	-	−60 V		60 s
+100 V		-	60 s	60 s	−80 V		60 s
+150 V		-	300 s	-	−100 V		60 s
+170 V		*	-	-	−100 V		120 s
+200 V			300 s	60 s	−100 V		300 s
+300 V			300 s	-	−100 V		600 s
+400 V			*	*	−100 V		1800 s

Table 18: Magnitudes and application times of the HV-stresses on normal MOS (left side) and nitride-layer-MOS (right side). '*' labels a breakthrough of the MOS, '-' means that no measurement was performed at this voltage.

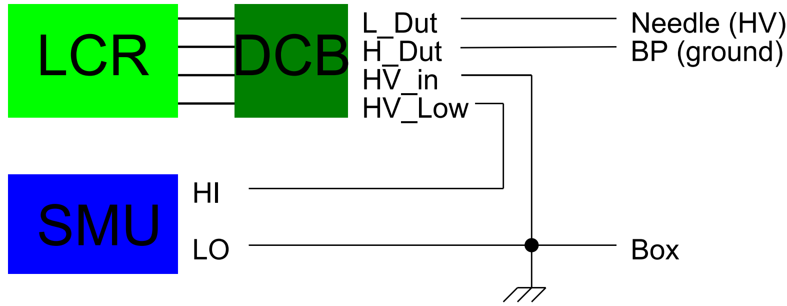


Figure 37: Changed circuit diagram for the CV-MOS-measurements with HV at the gate.

SMU	
$V_{\text{HV-stress}}$	listed in separate tables (18 and 20).
Time of HV-stress	
V_{min}	$-5\,\text{V}$
V_{max}	$+5\,\text{V}$
Stepsize	0.5 V
Compliance	1 mA
Wait	1000 ms
LCR initialisation	
Voltage level	250 mV
Current level	0
Frequency of AC signal	100 kHz

Table 19: Parameters for the long term charge up measurements of the nitride-layer-MOS with the changed measurement circuit of fig. 37.

of inversion is on the left side (at negative gate voltages) and the region of accumulation is on the right side (at positive gate voltages).

Moreover, the HV-stress was applied without ramp and, therefore, the compliance value of the SMU was set to 1 mA. A list of all parameters can be found in tab. 19.

Although the structures were treated with HV-stresses up to $-100\,\text{V}$ with duration times of up to half an hour, as listed in the right-hand columns of tab. 18, no effects on the CV-characteristics could be determined. Hence, a heat treatment of the structure (during the HV-stress) was considered to examine whether this may favour the accumulating of charges in the dielectric layer.

Heating. Thus, the probe table was heated with the Peltier elements and the secondary cooling circuit, as mentioned in sec. 4.

So the structure was heated to 50° C first and then to 65° C[27] and treated with HV-

[27] The secondary cooling circuit, of course also usable as heating circuit, was set 20° C below the set temperature of the probe table top.

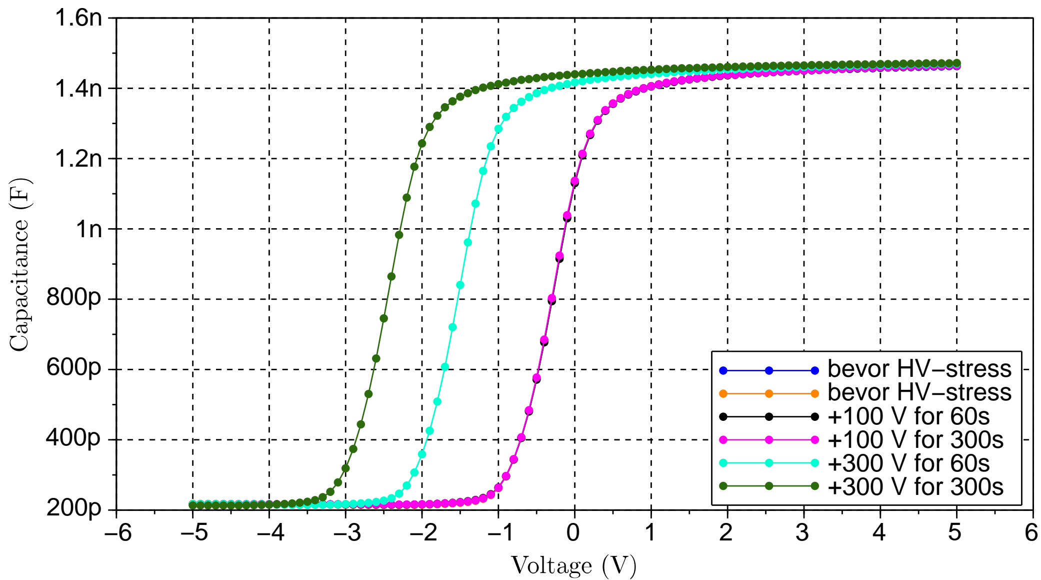


Figure 38: Shifts of the CV-curve after HV-stresses of +300 V for 60 s and 300 s (at 65° C). The first four curves of the legend are lying directly upon each other, so that one can only see the pink one.

stresses up to ±100 V for 300 s and 600 s, respectively, but the results remained unchanged. Hence, it was decided to use much higher voltages for the HV-stress, in spite of risking a breakthrough.

First successes with higher voltages. Thus, the nitride-layer-MOS of HM7 of W5 was stressed with +300 V for 60 s (at 65° C), and consequently, the MOS-characteristic was shifted about 1.2 V to more negative voltages. Another HV-stress of +300 V for 300 s shifted the curve further to the left, as shown in fig. 38.

To study the long term behaviour, this structure was measured again 16 h and 5 days after the last HV-stress (at room temperature). The resulting curves were shifted about 0.5 V to the right (with respect to the last HV-stress of +300 V for 300 s), so the total shift was diminished to approximately 1.5 V (see fig. 39).

So the shift due to HV-stress is long-lasting, however, whether it decreases with time or due to the difference in temperature needs further examination.

Reproducibility at room temperature. To examine the reproducibility at room temperature, another structure (the nitride-layer-MOS of HM11 of W5) was treated with HV-stress (2x initial, +100 V, +200 V and +300 V, each 60 s at 23.6° C). The curves measured after +200 V of HV-stress for 60 s were still completely identical to the initial

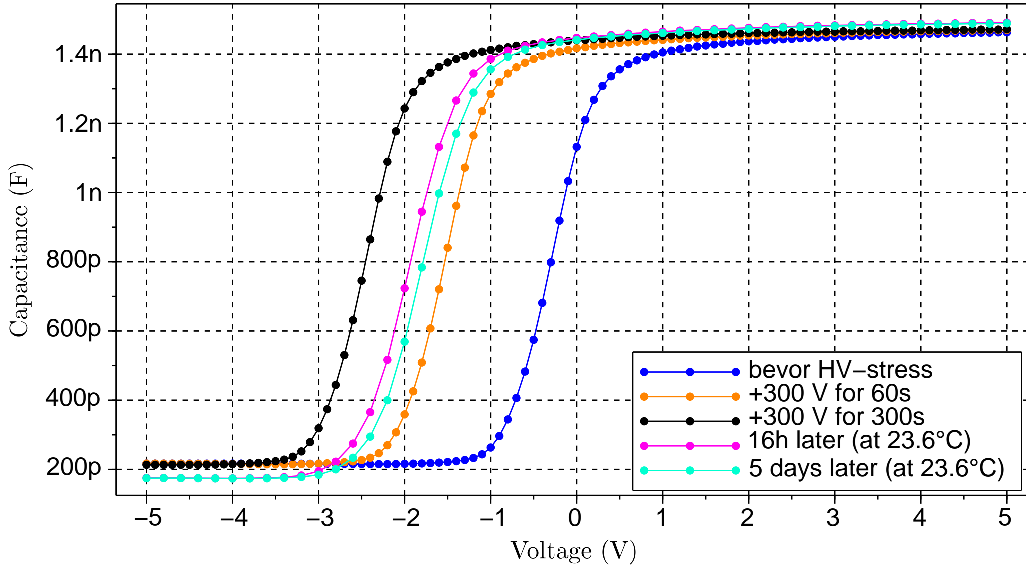


Figure 39: Shifts of the CV-curve after HV-stresses of +300 V for 60 s and 300 s (at 65° C) and remeasurements after 16 h and 5 days (at room temperature).

measurements, whereas, after +300 V of HV-stress for 60 s the curve was shifted 1 V to the left.

Negative HV-stress. To examine the effect of negative HV-stress, a new structure was taken (HM7 of W6) as well as the structure that showed a shift from the positive HV-stress from above (HM11 of W5). Both structures were treated with negative HV-stresses up to −300 V for duration times up to 300 s at room temperature, the first one also at higher temperatures (see tab. 20).

The results of the first structure, however, showed only diminutive deviations that could be measuring inaccuracies as well. The curve of the latter was shifted approximately 0.4 V to the right (with respect to the last positive HV-stress of +300 V for 60 s) after the first negative HV-stress, and from the second HV-stress onwards, it was only shifted infinitesimally further and didn't reach the initial curve.

Hence, the HV-stresses were increased up to −400 V, which finally resulted in a noticeable shift of 0.5 V to the right with respect to the initial curve. Longer HV-stresses for 300 and 600 s shifted the curves 0.4 V and 0.3 V further to the right, respectively.

So it became clear that the shift is not dependent on temperature, but apparently needs a sufficient high voltage. The magnitude of the negative HV-stress, obviously, has to be much higher for a shift to the right than that of the positive HV-stress for a comparable shift to the left.

	HM7 W6	HM11 W5	HM7 W6		
	at RT		35° C	50° C	65° C
initial	2x	-	2x	1x	1x
−100 V	-	-	60 s	60 s	60 s
−150 V	-	-	60 s	60 s	60 s
−200 V	60 s	-	60 s	60 s	60 s
−220 V	60 s	-	-	-	-
−240 V	60 s	-	-	-	-
−250 V	-	-	60 s	60 s	60 s
−260 V	60 s	-	-	-	-
−280 V	60 s	-	-	-	-
−300 V	60 s	60 s(2x)	60 s	60 s	60 s
−300 V	120 s	120 s	120 s	120 s	120 s
−300 V	300 s	300 s(2x)	300 s	300 s	300 s
−320 V					60 s
−340 V					60 s
−360 V					60 s
−380 V					60 s
−400 V					60 s
−400 V					120 s
−400 V					300 s
−400 V					600 s

Table 20: Magnitudes and application times of the negative HV-stresses.

Compensation of the shift. Along with this important knowledge, it was tried to compensate the previous shift of this structure (HM7 of W6) with positive HV-stresses, and afterwards with negative ones again[28]. These measurements showed that applying a positive HV-stress easily overcompensates a shift to the right due to negative HV-stress, as the first application of +200 V shifted the curve back to the initial one, and the following further to the left side. Though, the shift got smaller with every repetition for constant voltage and time and didn't increase until the voltage was raised. In the opposite direction, the shift was also compensated to the initial curve after the first application of −400 V, but the further shifts to the right side got very small with continuing repetitions and didn't increase until the duration of the stress was raised. Yet they didn't reach the first curve of the −400 V HV-stress for 600 s. The behaviour of V_{fb} after consecutive positive and negative or consecutive negative and positive HV-stresses can also be seen later in the plots of V_{fb} versus the time of duration of the HV-stress in fig. 41 or fig. 42, respectively.

Time dependency. Furthermore, the dependency of the V_{fb}-shift on the time of application of the HV-stress was examined using a new structure (HM7 of W23). Particularly, the effect of very short HV-stresses of only a few seconds was examined in a first test. The sample was stressed with +300 V for times from 1 s increasing up to 60 s[29]. The results yielded that even a HV-stress of only 1 s induces a small but noticeable shift (at repetition the further shift gets smaller), and for longer times of HV-stress the shift increases steadily, but non linear (see fig. 40 top). Afterwards the structure was stressed with −400 V for the same duration times[30]. There could be seen that the first step was greater, the following were very evanescent, and last ones (for duration times longer than 8 s) got greater again (see fig. 40 bottom). These measurements were also plotted as V_{fb} vs. time in fig. 41.

Furthermore, in a the second test, several HV-stresses of the same time (10 s) were applied. In addition, the order of positive and negative HV-stresses was reversed, so the structure was first stressed with −400 V (9 times consecutively), afterwards with +300 V (also 9 times) and finally again with −400 V (9 times as well). The negative HV-stresses effected very small shifts that got smaller with every repetition. The first positive HV-stress overcompensated the negative one and shifted the curve to 0.5 V to the left of the initial curve. Then the shifts also got smaller with every further repetition. The recent negative HV-stresses effected a great shift of 1 V for the first stress and small ones for the following (in the same order of magnitude as the previous negative HV-stresses). However, the curve didn't reach the initial curve, as can be seen in fig. 42, where the flatband voltage is plotted versus the time steps.

[28]Therefore, the following conditions were applied (after the previously described negative HV-stress up to −400 V for 600 s): +100 V, 5 times +200 V and once +250 V, each for 60 s, and afterwards −400 V 4 times for 60 s, once for 300 s and once for 600 s.

[29]Precisely: 3 times 1 s and once 2 s, 4 s, 8 s, 16 s, 30 s and 60 s.

[30]Except 1 s only 2 instead of 3 times.

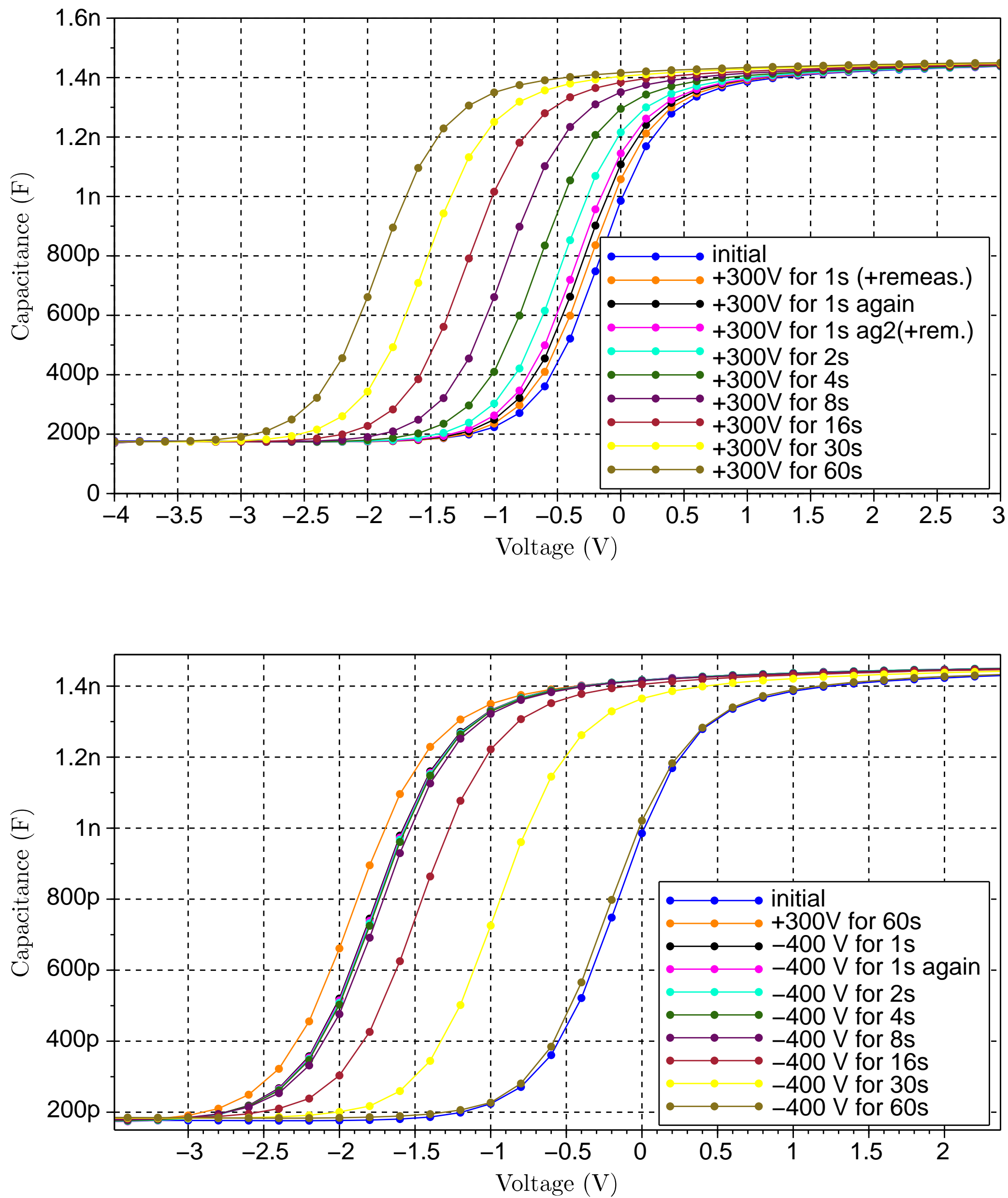


Figure 40: Shift of the CV-curves after HV-stresses of +300 V (top) and −400 V (bottom), respectively, for times of 1 s , 2 s, 4 s, 8 s, 16 s, 30 s and 60 s. A plot of the flatband voltage vs. the time can be seen in fig. 41.

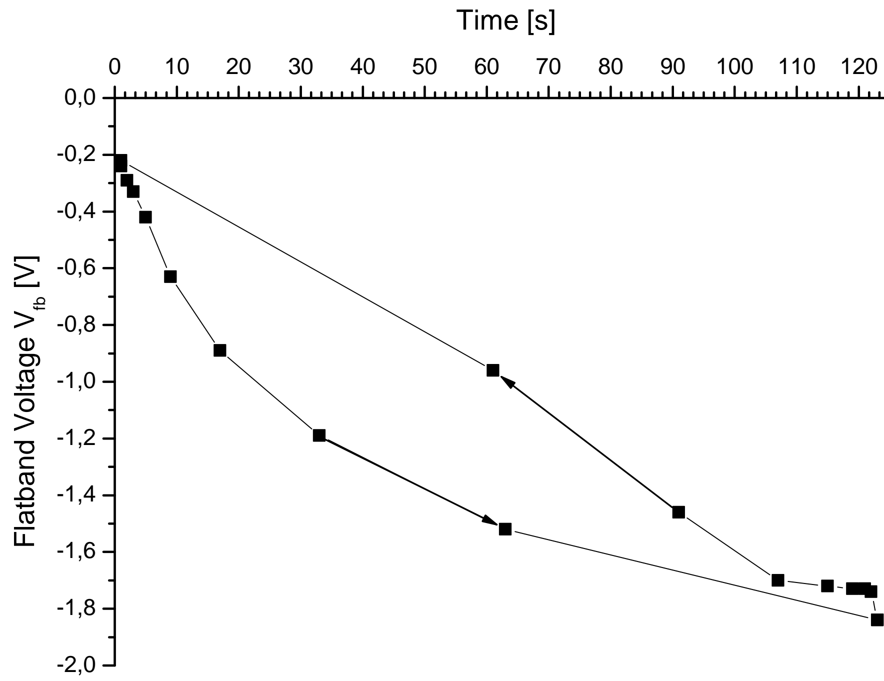


Figure 41: Shift of the flatband voltage V_{fb} after consecutive HV-stresses of $+300\,\mathrm{V}$ (lower curve, from left to right) and $-400\,\mathrm{V}$ (upper curve, from right to left), respectively, for times of 1 s, 2 s, 4 s, 8 s, 16 s, 30 s and 60 s.

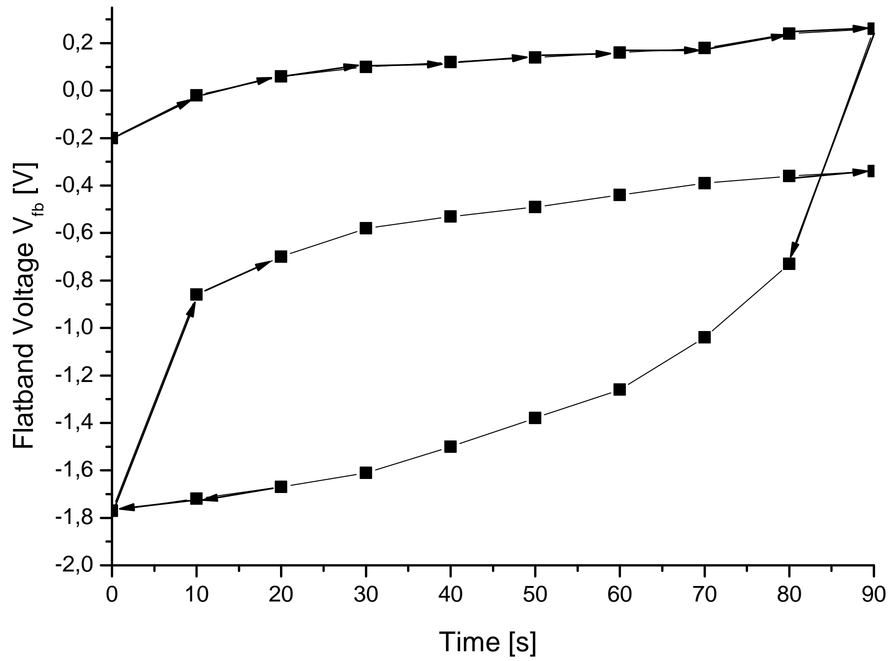


Figure 42: Time dependency of the shift of the flatband voltage V_{fb} after HV-stresses of -400 V for 10 s each time and 9 times consecutively, then $+300$ V, again for 10 s each time and 9 times consecutively, and afterwards again with -400 V 9 times for 10 s. The order of the measurements follows the direction of the arrows, the positive HV-stress is plotted from right to left.

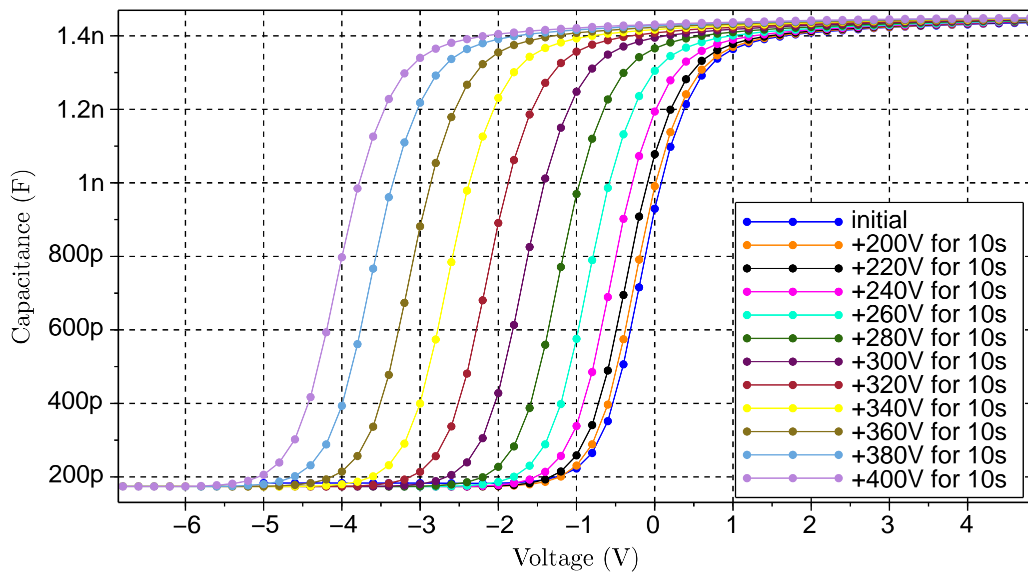
Voltage dependency. The voltage dependency of the shifts after HV-stress was examined by applying various HV-stresses starting with +200 V and increasing the voltage in steps of 20 V up to +400 V. This was done once with 1 s for each stress (on HM7 of W24) and once with 10 s (on HM11 of W24). The results were very alike (except, of course, for the maximum shift that was −2.4 V for the first one and −3.9 V for the latter), the shifts started very small and got greater until they were more or less constant. In fig. 43 the latter results can be seen, on top the CV-curves and at the bottom the shift of the flatband voltage V_{fb} versus the voltage of the HV-stress.

Influence of temperature. To survey the influence of the temperature on the flatband voltage, at first, a CV-characteristic of a nitride-layer-MOS (of HM7 of W6) without HV-stress was measured at different temperatures (from room temperature up to 65° C). The results in fig. 44 show that the CV-curve is shifted a little to the left, the region of inversion is raised and the region of accumulation is lowered very slightly. Here, the difference between room temperature and 65° C is 0.2 V of shift in depletion-, 40 pF of raise in inversion- and 20 pF of lowering in accumulation-zone. Then, another structure (HM7 of W18) was treated with +300 V HV-stress 9 times for 10 s, at different temperatures, varying between 23° C and 65° C. The results were compared to those of HM7 of W23, which was also treated with the same positive HV-stresses of +300 V 9 times for 10 s, but at room temperature (23.6° C).

The results are plotted in fig. 45 with two abscissas: V_{fb} vs. time and vs. temperature. The green curve is V_{fb} vs. time at constant temperature (23.6° C). The blue one is V_{fb} vs. temperature with the same time steps as the green curve. The first two blue points are stacked upon each other, because the initial measurement and that after the first HV-stress were both performed at 23° C, but according to the time, the upper one should be counted to 0 s and the lower one to 10 s. The temperature dependency of V_{fb} without any HV-stress can be seen in the purple curve.

Obviously, the two curves after HV-stress are very alike. With increasing temperature they diverge, as the blue curve declines more than the green one. Since the flatband voltage decreases with temperature without any HV-stress as well, one can conclude that the temperature has no significant influence on the charge accumulation due to HV-stress.

Further studies. To survey the long term behaviour, extensive bathing tests were performed. The procedure was the very same as described above in sec. 5.1. The three mostly stressed structures (HM7 of W5, HM11 of W5 and HM7 of W6) were put into deionised water for several different times and, after every bathing procedure, a further CV-characteristic was measured. The bathing periods were increased after every procedure, as listed in tab. 21. However, even a week of bathing didn't change the CV-characteristics at all, so one can conclude that the charge accumulation due to HV-stress is long-lasting.



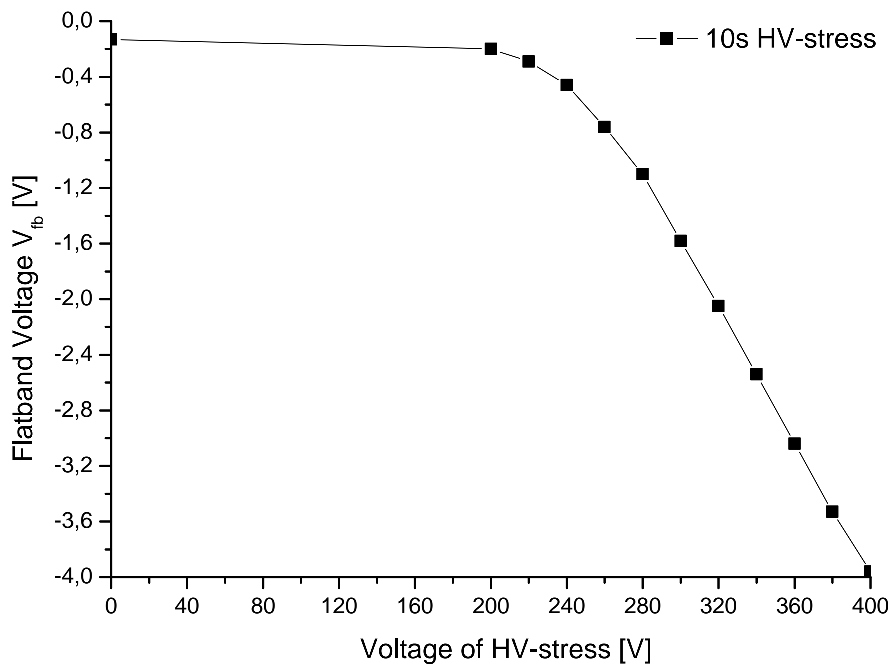


Figure 43: Voltage dependency of the shifts after HV-stress, on top the CV-curves and at the bottom the shift of the flatband voltage V_{fb} versus the voltage of the HV-stress.

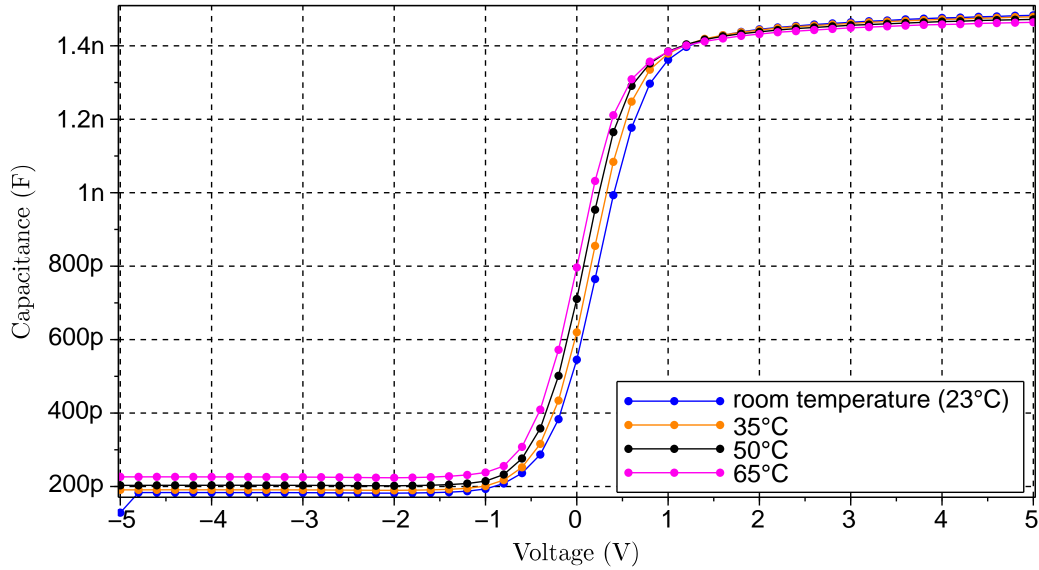


Figure 44: Influence of the temperature on the CV-characteristic (of the nitride-layer-MOS of HM7 of W6). The difference between room temperature and 65° C is here 0.2 V of shift in depletion, 40 pF of raise in inversion and 20 pF of lowering in accumulation.

HM7 of W5	HM11 of W5	HM7 of W6
15 min	22 h	1 h
1 h	74 h	95 h
4 h	7 days 4.25 h	7 days 4 h
91 h		
7 days 4.5 h		

Table 21: Duration of each bathing procedure.

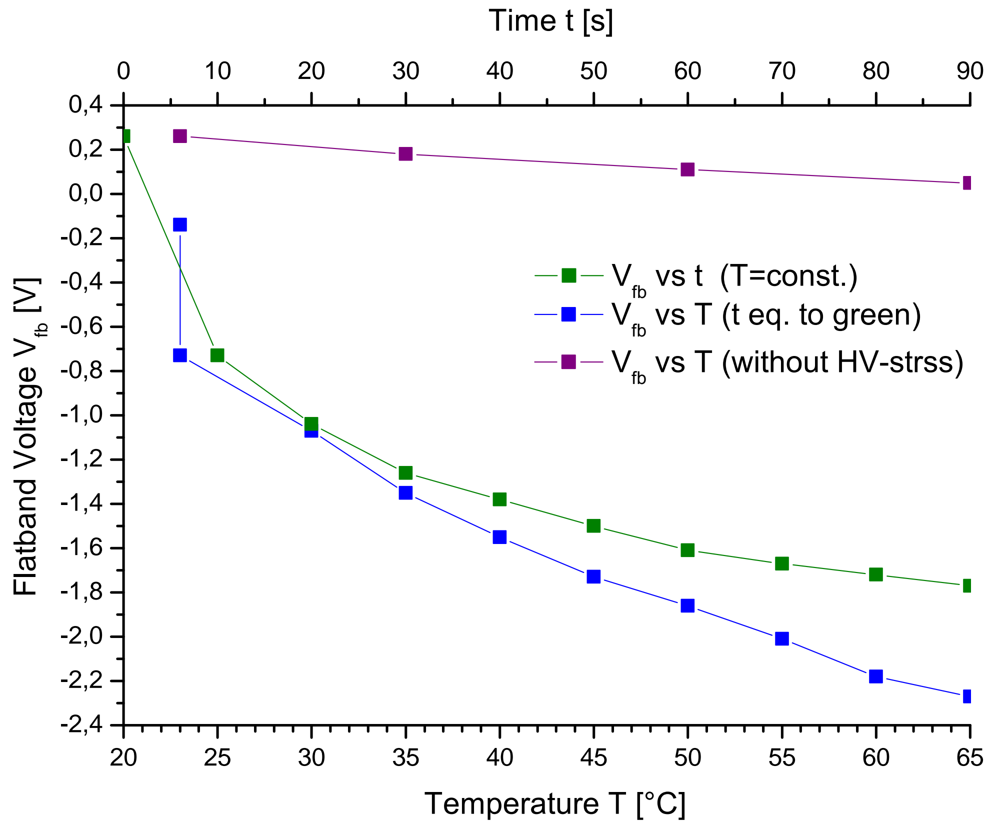


Figure 45: Influence of the temperature on the flatband voltage V_{fb}. The green curve is V_{fb} vs. time at constant temperature (23.6° C). The blue one is V_{fb} vs. temperature with the same time steps as the green curve. The first two blue points are stacked upon each other, because the initial curve and that after the first HV-stress are both measured at 23° C, but according to the time, the upper one should be counted to 0 s and the lower one to the first 10 s of HV-stress. The purple curve shows the temperature dependency of V_{fb} without any HV-stress.

Moreover, it was rechecked, if charges could also be introduced into an dielectric without additional nitride-layer using the knowledge and improvements obtained in the previous studies. Thus, a normal MOS (of HM11 of W6) was treated with HV-stress in the same way as all the nitride-layer-MOS mentioned above. Though, a HV-stress of −400 V for 60 s and then again for 600 s didn't change the CV-characteristic noticeably. Finally, a HV-stress of +300 V resulted in a destructive breakthrough, which confirmed that normal MOS are less stable than such with additional nitride-layer.

6 Conclusions for new designs and further measurements

In the so-called phase II upgrade, the tracker of the CMS-experiment will be renewed. Therefore, new sensors have to be developed with new technology or materials that exhibit higher radiation hardness.

In the course of this work, all the standard measurements on test structures of the two vendors *Hamamatsu Photonics K. K.* (HPK) and *Infineon Technologies Austria AG* (Infineon) were performed and analysed. In addition, some of the Labview software used for the measurements of the test structures were revised and enhanced. For the sheet resistance measurements, for instance, the program has been fundamentally changed, such that a current ramp can be applied and the voltage is measured. This allows to measure all different sheet structures with the same adjustments and without a priori knowledge about the range of the sheet resistance. Furthermore, a bias voltage ramp was implemented to generate resistance versus bias voltage graphs.

With this new measurement method, it was discovered that the resistance of the implant varies strongly for low voltage levels, but stays constant when the bias voltage exceeds a certain value that is, however, much lower than the full depletion voltage. Furthermore, all sheet structures should be encircled by a bias ring to ensure a good extension of the depletion zone. Yet, this was implemented in the current HPK-design.

Additionally, MOS structures from Infineon were examined in detail, using many different passivations and an additional nitride-layer and n-spray-layer.

During this examinations, there has been noticed that one special passivation affects the MOS-characteristic, but only in combination with the additional nitride-layer. This is surprising as virtually the whole structure is free from passivation. However, the MOS with standard passivation was not affected.

The additional n-spray-layer on the MOS also influenced the CV-curve by shifting the flatband voltage V_{fb}. This was to be expected, as the n-spray-layer changes the doping profile of the structure.

Furthermore, some structures were treated with HV-stress. This also shifts the flatband voltage, dependent on the polarity of the applied high voltage. This shift is long-lasting and can only be diminished or (over-)compensated by applying a reversed HV-stress. However, it seems peculiar that the different polarities of the HV-stress cause shifts of different magnitude, respectively one needs a higher voltage to obtain the same shift. There can also be said that the voltage has to be sufficiently high to affect the CV-characteristic at all, but even a short time of application of only one second suffices

to obtain a noticeable shift.

Moreover, these effects only occurred when dealing with the nitride-layer-MOS. So it is presumed that the nitride-layer is more sensitive to charge accumulations, as it also shows not understood effects with special passivations.

Generally, one can conclude that the test structures of Infineon with similar composition are comparable to that of HPK, which are well-probed from previous works (i.e. [13] and [17]). The only exception are the GCDs of Infineon, which have very irregular characteristics that could not have been understood in spite of many measurements. This leaves open a field for further studies.

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