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DIPLOMARBEIT

READOUT SOFTWARE FOR THE BELLE II SILICON VERTEX DETECTOR AND BEAM TEST DATA ANALYSIS

Ausgeführt am

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in Zusammenarbeit mit

Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften

Unter der Anleitung von
Privatdoz. Dipl.-Ing. Dr.techn. Christoph SCHWANDA
und
Univ.Lektor Dipl.-Ing. Dr.techn. Thomas BERGAUER
durch

Hao Yin Kölblgasse 1/2, 1030 Wien

Datum	Unterschrift (Student)

Abstract

The Belle experiment located at Tsukuba (Japan) was designed to ingestive CP violations during quark mixing processes. After a decade of successful operation the Belle detector is going to be upgraded. The upgrade includes an increase of luminosity from 2.11×10^{34} to about $8 \times 10^{35} \text{cm}^{-2} \text{s}^{-1}$. In order to cope with a 40 times higher luminosity the vertex detector (VXD) has been redesigned. The inner part of the VXD consists of two layers of silicon pixel detectors (PXD). Together with the silicon vertex detector (SVD) comprising of four layers of double sided silicon strip detectors (DSSD), the new BELLE II VXD will be able to perform high precision vertex measurements.

The most time consuming task of this work was to continue the development of the control software (TuxDAQ) and the design of an online data quality monitoring application (TuxOA) for the SVD system. Both applications has been successfully tested during a beam test at DESY, Germany. Parts of both software systems will be implemented into the future SVD slow control system.

The DESY beam test was the first integration test of SVD and PXD subsystems. During the measurements, several noise problems occurred. The impact of the noisy data and the effects on the analysis are discussed in this work.

During the beam test at DESY the data was taken from four rectangular DSSDs at several temperatures. The DSSDs are samples taken from the barrel part of each layer of the SVD. The results were evaluated with TuxOA.

Zusammenfassung

Das Belle-Experiment in Tsukuba, Japan, war konzipiert um CP Verletzungen zu untersuchen, die durch Quarkmischung-Prozesse erzeugt werden. Der Belle-Detector wird nach einer Dekade erfolgreicher Operation aufgerüstet. Das Upgrade inkludiert eine Erhöhung der Luminosität von 2.11×10^{34} zu $8 \times 10^{35} \mathrm{cm}^{-2} \mathrm{s}^{-1}$. Um mindestens die gleiche Präzision mit einer 40-fach größere Teilchenrate zu erhalten, wird der Vertex-Detektor (VXD) umkonstruiert. Die innersten zwei Schichten werden durch Pixel-Detektoren ersetzt. Zusammen mit dem Silizium-Vertex-Detektor (SVD), bestehend aus vier Lagen an doppelseitigen Silizium-Streifendetektoren (DSSD), kann der neue BELLE II VXD Vertex-Messungen mit einer besseren Auflösung durchführen.

Der zeitaufwendigste Teil dieser Arbeit war die Weiterentwicklung eines vorhandenen Steuerungssystems (TuxDAQ) und das Design der Online-Monitoring Software (TuxOA) für das SVD-System. Beide Applikationen wurden in einem Teststrahl am DESY, Deutschland, erfolgreich getestet. Teile beider Systeme werden in der kommenden SVD Slow Control implementiert.

Der Teststrahl am DESY war der erste Integrationstest von SVD und PXD. Während der Messungen sind einige Probleme aufgetreten, die durch das Einspeisen von Rauschen in die Ausleseelektronik verursacht wurden. Die Auswirkungen auf die Analyse wird in Zuge dieser Arbeit diskutiert.

Beim DESY-Teststrahl wurden vier rechteckige DSSDs bei unterschiedlichen Temperaturen untersucht. Die vier Sensoren waren Prototypen des SVDs. Die Ergebnisse wurden mit TuxOA ausgewertet.

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Chapter 1

Belle II detector

1.1 Physics motivation

The standard model (SM) of particle physics offers predictions with an astonishing precision. This theory describes the interactions of subatomic particles and unifies three out of four known fundamental interactions. However there are still a lot of open questions left. One of those puzzles is the asymmetry of matter and antimatter. In 1967, Andrei Dmitrievich Sakharov proposed the following requirements for this asymmetry [14]:

- baryon number violation,
- thermal non-equilibrium,
- charge (C) asymmetry and
- charge and parity (CP) asymmetry.

Regarding the latter, CP violation was first experimentally observed in neutral kaon decays by Cronin and Fitch [2] and later theoretically explained by the three-generation quark mixing introduced by Kobayashi and Maskawa [12]. The current models of cosmology however find this amount of CP violation to be insufficient for explaining the baryon density of the Universe. New sources of CP violation naturally arise in physics scenarios beyond the Standard Model (so-called 'New Physics'), which are the focus of the current research in particle physics. There are two distinct approaches for searching for New Physics:

New Physics comes with new particles and resonances. So, one approach is to study particle collisions at the very highest energies and to search for the direct production of new particles. This approach is currently spearheaded by the LHC collider at CERN (Switzerland) and the general purpose experiments ATLAS and CMS located at the interactions regions of this machine. Research at CERN has effectively led to the discovery of a new particle, the Higgs boson at a mass of 125 GeV. The experiments are going on to further probe the properties of the Higgs and to search for further new particles predicted in scenarios such as Supersymmetry.

On the other hand, new heavy particles introduce virtual contributions in processes at lower energies. New Physics can thus also reveal itself as a deviation from the Standard Model prediction, provided that experiment and theory are sufficiently precise. This is the

approach followed the Belle experiment and its successor Belle II, located at the KEK lab in Tsukuba, Japan. Belle has discovered CP violation in B meson decays and confirmed the quark mixing mechanism introduced by Kobayashi and Maskawa. Belle II will repeat these measurements with about 50 times more data to probe New Physics models with precision data.

1.1.1 \hat{V}_{CKM} and CP Violation

The matter described by the SM consists of three generations of particles. Each generation contains two quarks and two leptons. Prior to Kobayashi and Maskawa Cabibbo theorized, that the weak eigenstates are a linear combination of the flavour states:

$$\begin{pmatrix} d' \\ s' \end{pmatrix} = \begin{pmatrix} \cos(\theta_c) & \sin(\theta_c) \\ -\sin(\theta_c) & \cos(\theta_c) \end{pmatrix} \begin{pmatrix} d \\ s \end{pmatrix}$$
 (1.1)

with d' and s' representing the weak eigenstates, d and s the flavour eigenstates. θ_c is the Cabibbo angle. At that time, the charm, bottom and top quarks were not discovered yet. Kobayashi and Maskawa postulated a third generation of quarks extending the rotation matrix in eq. (1.1) to:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \hat{\mathbf{V}}_{\text{CKM}} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{1.2}$$

Three angles θ_1 , θ_2 , θ_3 and a complex phase δ are needed to parametrise $\hat{\mathbf{V}}_{\text{CKM}}$ [12]:

$$\hat{\mathbf{V}}_{\text{CKM}} = \begin{pmatrix} V_{\text{ud}} & V_{\text{us}} & V_{\text{ub}} \\ V_{\text{cd}} & V_{\text{cs}} & V_{\text{cb}} \\ V_{\text{td}} & V_{\text{ts}} & V_{\text{tb}} \end{pmatrix} = \begin{pmatrix} c_1 & -s_1 c_3 & -s_1 s_3 \\ s_1 c_2 & c_1 c_2 c_3 - s_2 s_3 e^{i\delta} & c_1 c_2 s_3 + s_2 c_3 e^{i\delta} \\ s_1 s_2 & c_1 s_2 c_3 + c_2 s_3 e^{i\delta} & c_1 s_2 s_3 - c_2 c_3 e^{i\delta} \end{pmatrix}$$
(1.3)

 c_i and s_i are $\cos(\theta_i)$ and $\sin(\theta_i)$, respectively. The additional phase δ causes the CP violation. The unitary property of $\hat{\mathbf{V}}_{\text{CKM}}$ requires the following:

$$\sum V_{ij}V_{ik}^* = \delta_{jk} \tag{1.4}$$

For $j \neq k$ the unitary condition can be represented as a triangle in the complex plane. The so called unitary triangle, determined by eq. (1.4) for $j \neq k$, can vary in shape, but the enclosed area is preserved. Figure 1.1 shows an example of an unitary triangle. The aim of Belle experiment was to determine the sides and angles.

1.2 The KEKB collider and upgrade to SuperKEKB

KEKB is the asymmetric energy electron positron collider, at which the Belle experiment was located. [17]. The circumferential length is about 3 km. The collider operates with two particle beams at different energies. After reaching the requested kinetic energies in the linear accelerator the particles are fed into two different storage rings. The electrons are injected into the high energy ring at 8 GeV and the positron into the low energy ring at 3.5 GeV. The design luminosity (i.e., the event rate in units of the e^+ e^- cross-section) 10^{34} cm⁻²s⁻¹.

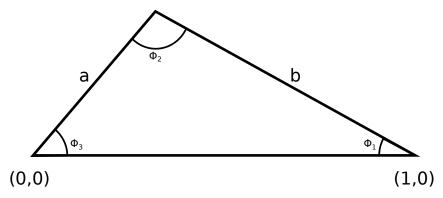


Figure 1.1: Unitary triangle with $a = \left| \frac{V_{td}V_{tb}^*}{V_{cd}V_{cb}^*} \right|$ and $b = \left| \frac{V_{ud}V_{ub}^*}{V_{cd}V_{cb}^*} \right|$.

At the interaction point the centre mass energy is 10.58 GeV, corresponding to the $\Upsilon(45)$ resonance that in turn decays into B and \overline{B} pair. Due to the asymmetric energies the created particles gain a relativistic boost in direction of the electron beam, thus increasing their travelled distance. The differences in decay time Δt can be measured by distance Δz between the vertices of B and \overline{B} :

$$\Delta z = \beta \gamma c \Delta t,\tag{1.5}$$

with $\beta = \frac{v}{c}$ and $\gamma = \sqrt{1 - \beta^2}^{-1}$. c represents the vacuum speed of light and v the centre of mass velocity.

KEKB is going to be upgraded to SuperKEKB by reusing most of the components. The upgrade is based on the nano beam scheme [17]. The expected luminosity is about $8 \cdot 10^{35}$ cm⁻²s⁻¹. Further more the diameter of the beam pipe at the interaction region will be reduced to 20 mm [17] allowing a better vertex resolution. However at such distances the particle density and background radiation poses a considerable challenge for the particle detectors. Figure 1.2 shows the schematics of SuperKEKB accelerator.

1.3 The Belle II detector

The Belle detector is located at the one and only interaction point of the KEKB collider. It was designed to precisely measure B meson decays. Since the upgrade to SuperKEKB includes an increase of the luminosity by a factor 40, the Belle detector is also going to be upgraded to the Belle II system in order to cope with a greater occupancy and background radiation. The sub-detectors, figure 1.3, are described in the following:

Pixel detector (PXD)

By employing the nano beam scheme the radius of the beam pipe at the interaction region will be reduced to 10 mm. The greater luminosity and background radiation, that increases with inverse square of the radius, will induce a higher occupancy, see figure 1.4, of strip sensors making it nearly impossible to reconstruct any high resolution vertices. Thus the two innermost layers will be replaced with pixel detectors with a greater number of readout channels. The first layer is placed at a radius of 14 mm consisting of 50 μ m × 50 μ m pixels and the second layer at 22 mm with 50 μ m × 75 μ m pixels.

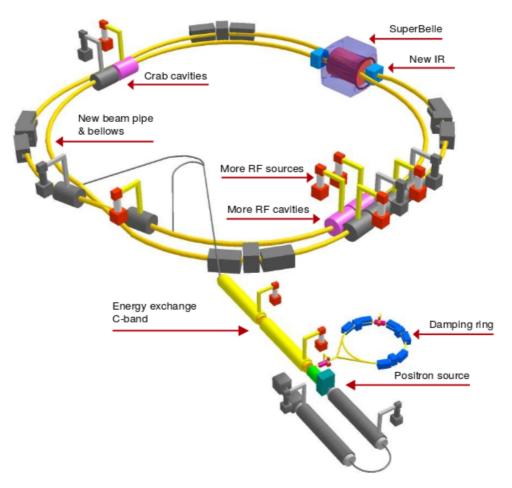


Figure 1.2: Schematics of SuperKEKB [5]

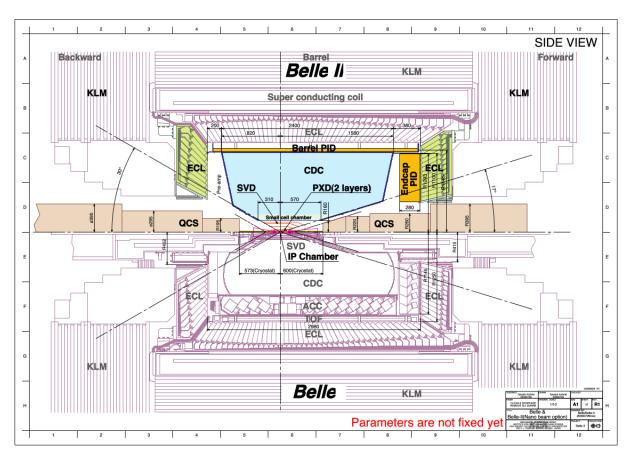


Figure 1.3: The upper part shows the Belle II detector and the lower part the current Belle detector [17].

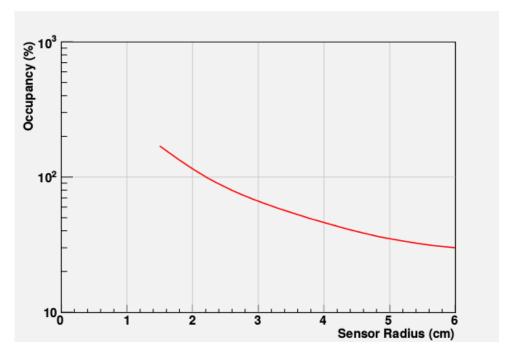


Figure 1.4: Expected occupancy of SuperKEKB [17].

The pixel detectors are based on the depleted field effect transistor (DEPFET) technology, that allows thinner sensors thus reducing multiple scattering in the sensitive area. Oversimplified a pixel is a p-channel MOSFET. The sensitive area consist of a silicon bulk depleted by the negative biased back plane. A potential minimum is created by sidewards ionisation. An incident particle creates electron-hole pairs inside the silicon bulk. While the holes drift towards the back plane, the electrons accumulate at the potential minimum. The same charge accumulation can be repeatedly read out by measuring a change in the current signal of the channel. A punch through from a neighbouring n⁺ contact clears the build-up at the minimum.

The thickness of the detector is tinned to 75 μ m yielding a radiation length of about 0.19% X₀ [17]. Due to the large number of readout channels it is not feasible to readout all the channels. In order to reduce the data output rate a fast online track fit is performed with the data taken from SVD. Only the intersections of the fitted tracks and the pixel detectors, the so called "region of interest" (ROI), are read out.

Silicon strip detector (SVD)

One of the task of SVD is to measure the vertices of the B mesons together with PXD and CDC. The data provided by SVD is also used to calculate ROIs to reduce the output rate of PXD and provides an estimate of the momenta by measuring the deflection of charged particles in the solenoid magnetic field.

Figure 1.5 shows the placement of the silicon strip sensors in the Belle II detector. Four layers of double sided silicon strip detectors (DSSD) surround the innermost detector

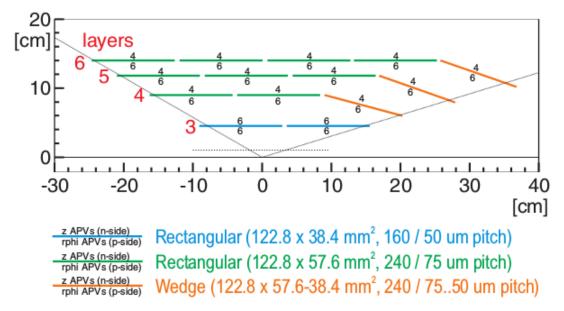


Figure 1.5: Layout of SVD [17]. The number above each coloured line represents the number of the APV25 readout chips on the p-side and below each coloured line the number of chips on the n-side.

system (PXD). The polar angle coverage (defined relative to the beam axis) ranges from 17° to 150°. The relativistic boost in the direction of the electron beam is reflected in the design of the detector. While the first layer is arranged in a cylindrical layout, the

remaining layers have a conical part comprising of trapezoidal shaped DSSD, figure 1.5 (orange lines). The following chapter will cover a more detailed description of the SVD system.

Central drift chamber (CDC)

The central tracking device of Belle and Belle II is a drift chamber filled with a helium ethane gas mixture [17]. The main task of CDC is to measure particle tracks, momenta and the energy loss inside the detector. Additionally it is used as a trigger source for charged particles.

Incident particles cause ionization along their track inside the gas chamber. Secondary ionizations are caused by electrons, that are accelerated towards the anode/sense wires. Each sense wire is surrounded by field wires at ground potential, that shape the electromagnetic field.

Particle identification devices (PID)

In the barrel part of Belle II the PID consists of 16 time-of-propagation detectors (TOP) surrounding the outer wall of CDC. The device measures the propagation time and emission angle of Cherenkov photons. Micro channel plates at one end of the TOP allows the measurement of the lateral position and a precise timing, from which the Cherenkov image can be reconstructed.

In the forward endcap aerogel ring imaging Cherenkov counters (ARICH) are deployed to identify traversing particles. The Cherenkov photons generated inside the aerogel radiator. An expansion volume allows those photon to form rings on position sensitive detectors.

Electromagnetic calorimeter (ECL)

The electromagnetic calorimeter consists of a 3 meter array of thallium-doped caesium iodide crystals. Its main task is to detect photons produced by B meson decays that ranges from 20 MeV to 4 GeV. Additionally it also generates trigger signals.

Kaon and muon detection system (KLM)

The outermost system of Belle II is designed to detect K_L and μ . The KLM consists of alternating ion plates and detector material. The ion plates allows the incident particles to shower hadronically, scattering products are in turn measured by detector layers. Due to different radiation environments different detectors have been deployed: In the barrel section the alternating detector layers consists of glass electrode resistive plate chambers (RPC). The RPC comprises of two parallel glass plate with a bulk resistivity of $\sim 5 \times 10^{12}$ Ω cm. By applying a strong electrical field the impinging particle causes a streamer between the glass plates. The external pickup strips detect the location and time of the discharge. Due to greater radiation levels at the endcaps the RPCs are replaced with plastic scintillator strips. The produced photons are detected by silicon photomultipliers.

Chapter 2

SVD system

2.1 Silicon strip sensor

Each electron in an isolated atom has discrete an energy level determined by the electromagnetic potential of the nucleus. In a solid the distance between atoms are short enough to effectively distort the binding potential of each nucleus, therefore shifting the energy levels of their bound electrons in such a way that continues energy bands are formed. The upper bound of valence band is defined by highest possible energy state E_V that electrons can occupy at the temperature T=0 K. The next possible energy state E_C is the lower bound of the conduct band, where electrons can move more freely inside the solid. In a semiconductor the gap $E_G=E_C-E_V$ is small enough that thermal excitations can lift an electron from the valence to the conduct band and leave a hole in the valence band which can be regarded as a positive charge carrier, figure 2.1.

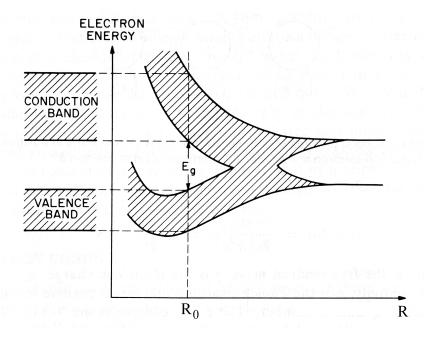


Figure 2.1: The band structure of silicon as a function of the distance R between each atom. R_0 is the lattice parameter and E_g the band gap [15].

The state density of electrons $N_e(E)$ denotes the number of states per unit energy in

the conduct band. The same idea can be applied to a state density of holes in the valance band $N_p(E)$:

$$N_e(E) = \frac{(2m_e^*)^{\frac{3}{2}}}{2\pi^2\hbar^3} \sqrt{E - E_C}, \quad N_p(E) = \frac{(2m_p^*)^{\frac{3}{2}}}{2\pi^2\hbar^3} \sqrt{E_V - E}$$
 (2.1)

While the effective mass of the electron \mathbf{m}_e^* is proportional to the inversed curvature of the conduction band, the effective mass of the holes \mathbf{m}_p^* is affected by the valance band. The Fermi Dirac distribution F(E) describes the occupation probability of those energy states:

$$F_e(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)}, \ F_p(E) = 1 - F_e(E)$$
 (2.2)

where k_B is the Boltzmann constant, T the temperature and E_F the Fermi level. At the Fermi level the occupation probability yield 0.5. The charge carrier, n for the electron density in the conduct band and p for the hole density in the valance band, is the convolution of the state density and occupation probability. By approximating F(E) with the Boltzmann distribution the convolution becomes:

$$n = \int_{E_C}^{\infty} N_e(E) \cdot F_e(E) dE = n_0 \exp\left(-\frac{E_C - E_F}{k_B T}\right)$$
 (2.3)

$$p = \int_{E_0}^{E_C} N_p(E) \cdot F_p(E) dE = p_0 \exp\left(-\frac{E_F - E_V}{k_B T}\right)$$
 (2.4)

 n_0 and p_0 are the effective state functions, that are unique for each semiconductor (m_e^* and m_p^*) and proportional to $T^{1.5}$. An intrinsic semiconductor is a semiconductor without impurities. The number of positive and negative charge carriers are the same, since each electron lifted to the valance band leaves a hole behind. The intrinsic charge concentration n_i and the intrinsic Fermi level $E_{F,i}$ can be expressed by the following:

$$n_i^2 = n_0 p_0 \exp\left(-\frac{E_C}{k_B T}\right), \ E_{F,i} = \frac{1}{2}(E_C + E_V) + \frac{1}{2}k_B T \ln\left(\frac{n_0}{p_0}\right)$$
 (2.5)

In contrast to metals the conductivity of semiconductors increases with rising temperature. The intrinsic Fermi level is located inside the band gap. In the case of silicon the energy gap is about 1.12 eV. At room temperature T = 300 K the intrinsic charge concentration yields $1.45 \times 10^{10} \text{ cm}^{-3}$.

In an intrinsic semiconductor the hole density is equal the electron density, figure 2.2 (a). By implementing a controlled amount of impurity atoms from the neighbouring groups III or V the Fermi level shifts towards either the valance or the conduct band. This process is also known as doping. The resulting semiconductors are called extrinsic.

The n-type semiconductor has impurity atoms from the group V, also known as donor atoms. The donor energy level of the additional electron E_D is close to the conduct band, thus the electron can easily be exited to the higher energy state. The additional charge carriers in the conduct band shifts the Fermi level of the n-type semiconductor $E_{F,n}$. While $n_i^2 = n \cdot p$ still applies, the majority of the charge carriers are the electrons in the conduct band, figure 2.2 (b).

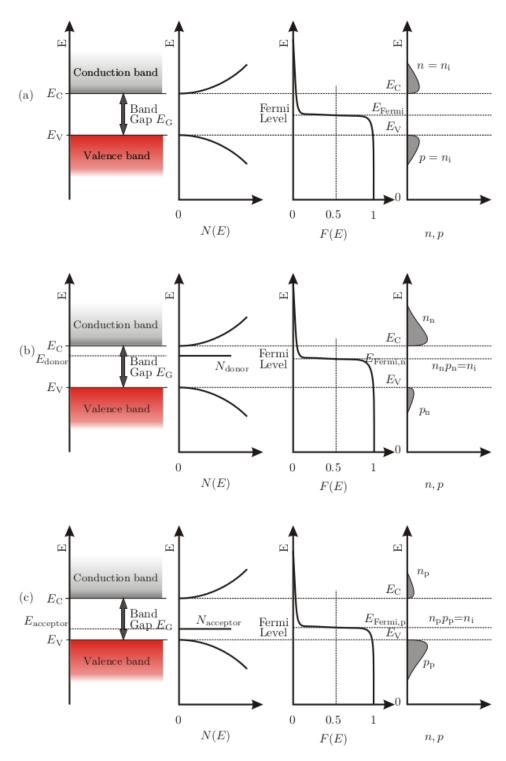


Figure 2.2: From left to right: Valence and conduct band, state density, Fermi Dirac function and charge concentration. (a) intrinsic semiconductor, (b) n-type semiconductor, (c) p-type semiconductor [16].

The same also applies to the p-type semiconductors with impurity atoms from the group III, acceptor atoms. The energy level of the missing 4th valence electron E_A is located slightly above the valence band and thus able to accept electrons, that are thermally exited. In this case the Fermi level shifts towards the valence band and the major of charge carriers are holes in the valence band, figure 2.2 (c).

The electron density of a n-type silicon semiconductor as a function of temperature is plotted in figure 2.3. At T=0 K the charge density is 0. As T increases some donor electrons are thermally excited into the conduct band. The temperature range, where some of the donor atoms are ionized, is called the freeze-out range. The saturation range describes the case, where the thermal energy is too small to create holes in the valance band but efficient enough to ionize all donor atoms. In the intrinsic range T is high enough to lift electrons from the valance band to the conduct band and the charge density approaches the intrinsic charge density. The same temperature dependency also applies to p-type semiconductors with holes as its majority charge carrier.

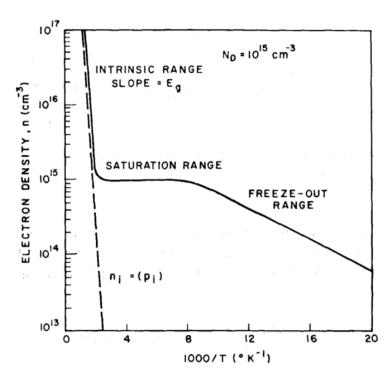


Figure 2.3: The electron density of a n-type silicon semiconductor (solid line) and an intrinsic silicon semiconductor (dashed line) [15].

2.1.1 pn-junction

The pn-junction comprises of a n and p-type semiconductor. At the boundary the quasi free electrons move towards acceptors and holes towards donors to compensate for the charged inhomogeneity. This process creates a region with negatively charged acceptors in p-type semiconductors and a region with positively charge donors in the n-type semiconductors. The charge build-up in turn forms a potential, that limits the diffusion and thus also the recombination process. The region of the charge build is called depletion zone or space charge region SCR. Due to the lack of charge carriers, the resistivity inside SCR increases. The potential at the boundary is know as build in voltage $V_{\rm bi}$. The width

of SCR W_{SCR} is described by the following equations:

$$W_{SCR,n} = \sqrt{\frac{2\epsilon\epsilon_0 V_{bi} N_A}{q_e N_D (N_A + N_D)}}, W_{SCR,p} = \sqrt{\frac{2\epsilon\epsilon_0 V_{bi} N_D}{q_e N_A (N_A + N_D)}}$$
(2.6)

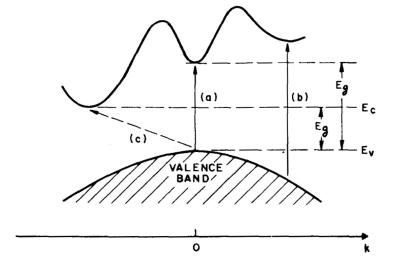
$$W_{SCR} = W_{SCR,n} + W_{SCR,p} = \sqrt{\frac{2\epsilon\epsilon_0 V_{bi}(N_A + N_D)}{q_e N_A N_D}}$$
(2.7)

The index n and p refers to the type of the semiconductors, respectively. N is the impurity atom concentration with the corresponding index A and D denoting acceptors and donors, respectively. ϵ_0 is the dielectric constant in vacuum, ϵ the dielectric constant of the semiconductor material and q_e the electron charge. By applying an external bias voltage V_{bias} , W_{SCR} can be modified. In case of a forward bias, the anode is connected to the p-type semiconductor and the cathode to the n-type one. The applied electric field pushes the electrons and holes towards the SCR consequently reducing V_{bi} and W_{SCR} . At this stage the semiconductor device becomes conductive. In case of a reversed bias the charge carriers are pulled away from the SCR enlarging the volume of depleted charges. The semiconductor remains insulating.

2.1.2 Charge carrier generation

As mentioned in the previous sections, charge carriers are generated by lifting electrons from the valance band to the conduct band. In a so called direct semiconductor the maximum of the valance band and the minimum of the conduct are located at the same crystal momentum \vec{k} . The minimum energy for an impinging particle required to excite an electron to the conduct band is called the band gap. In case of an indirect semiconductor the minimum of the valance band and the maximum of the conduct band have different \vec{k} values. Therefore the transition at the energy of the band gap requires the absorption or creation of a phonon. Consequently the energy loss of the incident particle is more likely greater than the band gap to excite an electron. Figure 2.4 shows a sketch of the mentioned transitions.

Figure 2.4: Sketch of transitions in an indirect semiconductor. (a) and (b) are direct transitions. (c) is an indirect transition involving the creation or absorption of a phonon in order to conserve the crystal momentum. [15]



As charged particles traverse through matter, ionizations and other effects cause the particle to lose energy. Depending on the inertia of the particle the energy loss is described in the following:

Electrons and positrons

The energy loss in matter of high energetic electrons/positrons is dominated by the bremsstrahlung. The ionisation processes are more likely to happen at lower energies. The mean energy loss can be expressed in terms of the so called radiation length χ_0 , where the incident particle losses about e^{-1} of its initial energy. χ_0 is described by the following empirical fit [4]:

$$\chi_0 = \frac{716 \cdot A}{Z(Z+1) \ln\left(\frac{287}{\sqrt{Z}}\right)} \cdot g \text{ cm}^{-2},$$
(2.8)

where A is the mass number and Z the atomic number. This equation applies to materials with Z < 4. In case of silicon with a density of 2.33 gcm⁻³ the radiation length yields $\chi_0^{SI} = 9.36$ cm.

Heavy and charged particles

For heavy particles the bremsstrahlung occurs at higher energies. In this case the mean energy loss $-\left\langle \frac{dE}{dx}\right\rangle$ is described by the Bethe-Bloch formula [4]:

$$-\left\langle \frac{\mathrm{dE}}{\mathrm{dx}} \right\rangle = Kz^2 \frac{\mathrm{Z}}{\mathrm{A}} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2\mathrm{m}_e c^2 \beta^2 \gamma^2 \mathrm{T}_{\mathrm{max}}}{\mathrm{I}^2} \right) - \beta^2 - \frac{\delta(\beta \gamma)}{2} \right], \tag{2.9}$$

with

	•	Description
_	K	 $4\pi N_{\rm A} r_e m_e c^2 \approx 0.307075 \ {\rm MeV \ cm^{-1}}$
	N_A	 Avogadro's number $\approx 6.022 \cdot 10^{23} \text{ mol}^{-1}$
	\mathbf{r}_e	 classical electron radius $\left(\frac{e^2}{4\pi\epsilon_0 m_e c^2}\right)$
	z	 charge of incident particle
	m_e	 rest mass of electron e
	\mathbf{Z}	 atomic number of the target
	A	 mass number of the target
	β	 $\frac{\mathbf{v}}{c}$
		$(1-\beta^2)^{-\frac{1}{2}}$
	$T_{\rm max}$	 maximum possible energy transferred in a single collision
	I^2	 mean ionisation energy of the target
	δ	 density effect correction

Figure 2.5 shows the Bethe-Bloch equation. The minimum is located at $\beta\gamma \approx 3$ regardless of target material type and depends on the rest mass of the incident particle. Particles with an energy at the minimum are called minimum ionizing particles MIPs. MIPs create the least amount of e-h pairs thus becoming an important value for sensor tests.

The Bethe-Bloch formula describes the mean energy loss of a particle in matter. The deposited energy fluctuates around the mean energy loss. For a thick sensor the most probable energy loss approaches its mean value. With decreasing thickness the distribution becomes more skewered and approximates the Landau distribution. The elongated tail towards greater energy deposition is caused by the rare production of highly energetic δ -electrons. Due to this effect the most probable energy loss diverges from the mean calculated using the Bethe-Bloch formula. In case of the silicon strip detector with a width of 320 μ m the most probable energy loss becomes 285 eV/ μ m [1], while the mean energy loss of an MIP yields 388 eV/ μ m [4].

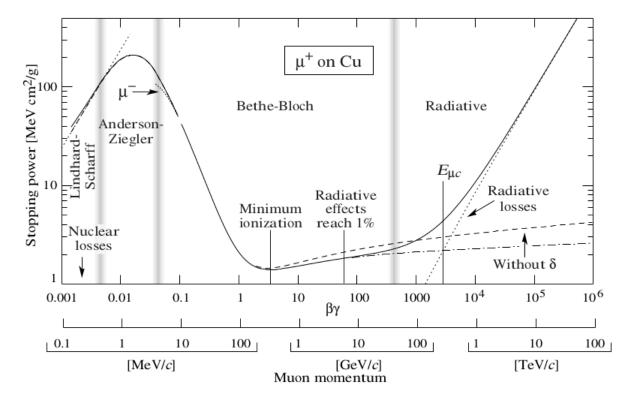


Figure 2.5: Energy loss of positively charged muons in a copper target. The vertical band marks the regions with different approximations. The solid line indicates the total energy loss. $E_{\mu c}$ shows the threshold, where energy loss by radiation is equal to the loss caused by collisions. [15]

2.1.3 Double sided silicon strip sensor

The main task of the DSSDs is to determine the position of an incident particle. The detector area consists of a n-type bulk, that is enclosed by a thin and highly doped p-type implant (p+) on the one side and on other side by a thin and highly doped n-type semiconductor (n+). As the particle traverses through the sensitive area, it creates e-h pairs along its track. The number of e-h pairs is proportional to the energy deposited in the detector material $E_{\rm dep}$. For silicon the minimum energy required for a direct transition to create an e-h pair is about 3.2 eV. Thus the number of charge carriers $N_{\rm e-h}$ for a silicon strip sensor with a thickness of 320 μ m can be approximated by $N_{\rm e-h} \approx E_{\rm dep}/3.2 {\rm eV} \approx 2.85 \cdot 10^4$,

with $E_{\rm dep} \approx 285~{\rm eV}/\mu{\rm m} \times 320~\mu{\rm m}$ representing the most probable energy deposited by a MIP.

At room temperature $T=300~\rm K$ the thermally generated e-h pairs in a 1 cm² detector area yields $n_i \cdot 300~\mu m \cdot 1~\rm cm^2 \approx 4.4 \cdot 10^8$ e-h pairs, with $n_i \approx 1.45 \cdot 10^{10}~\rm cm^3$ representing the intrinsic charge density. In order to suppress the thermal generation, a reversed bias is applied. The bias voltage is adjusted to extent the SCR over the whole sensor volume. Additionally the created electric field forces the e-h pairs generated by an incident particle to drift to the corresponding poles. The moving charge carriers in turn induce a time dependent current at the corresponding electrodes for the readout electronics. In order to

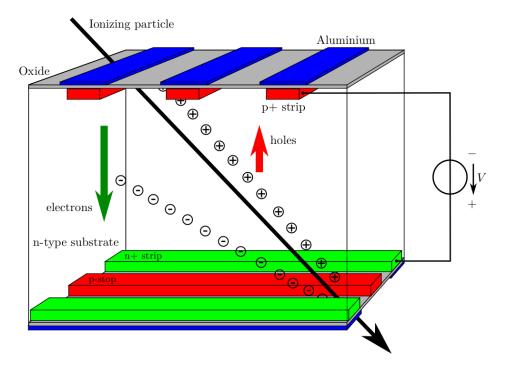


Figure 2.6: Sketch of a DSSD with a p-stop implant between each n+ strip [16]. Note: Sketch does not contain intermediate strips.

determine the position of the impinging particle the p+ and n+ implants are segmented into strips, see figure 2.6. On the p+ side each strip forms a pn-junction between the n-type bulk material. The reverse bias voltage increases the inter strip resistance. On the n+ side the strips are implemented in a n-type bulk material, therefore the n+ strips are not electrically isolated. In order to circumvent this problem a so call p-stop structure has been implemented. The p-stop structure is a highly doped p-type semiconductor that is located between the n+ strips. For more detailed description and other strategies to separate the n+ strips see the PhD thesis of Manfred Valentan [16]. Additionally so called intermediate strips have been implemented between two readout strips to increase the spatial resolution. The particle signal collected by the intermediate strip is capacitively read out by its neighbouring strip.

In order to reduce the capacitive load noise the Origami design [10] has been applied, where the readout chips are directly mounted on the n+ side of the sensor, figure 2.7. A 1 mm thick electrical and thermal isolator material separates the PCB from the sensitive area. A flexible PCB connects the strip on the side to the corresponding readout chip.

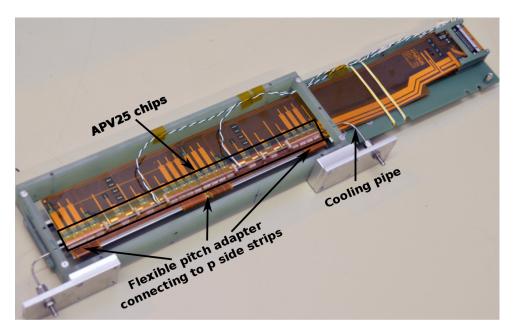


Figure 2.7: One of the Origami modules with rectangular DSSDs used in the DESY beam test.[10].

Since each chip dissipates about 350 mW, a cooling pipe is attached above the readout chips and connects to a 2 phase CO₂ cooling system.

2.1.4 Noise sources

The noise of each strip is an import benchmark for the signal quality generated by a particle. Each strip is read out by an integrating amplifier implemented in the APV25 chip [6]. The systematic fluctuations, that depend on the integration time $t_{\rm int}$, are denoted in equivalent noise charges (ENC) and consist of the following contributions [16]:

$$ENC^{2} = ENC_{C}^{2} + ENC_{P}^{2} + ENC_{S}^{2} + ENC_{J}^{2}$$
 (2.10)

The capacitive load noise ENC_C can be numerically approximated with ENC_C = $a+b\cdot C$. a and b are the fit parameters depending on the geometry of the design. C is the sum of all capacitive loads of a single strip including the readout and the inter strip coupling capacitances. ENC_P accounts for the thermal noise generated by the bias resistors. The contribution is proportional to $\sqrt{\frac{T\cdot t_{int}}{R_P}}$ with T denoting the temperature, t_{int} the integration time and R_P the parallel connected bias resistance. ENC_S describes the thermal fluctuations of resistors connected in serial and decreases with longer t_{int} . The majority of ENC_S is contributed by the aluminium layer connected to the readout chip. The contribution of the dark current ENC_J increases with t_{int} . The integration time of the APV25 chip is set at 50 ns in the so-called multi-peak mode.

2.2 Readout system

The DSSD designed for the Belle II experiment has 6×128 strips on the p-side and 6×128 (layer 4, 5 and 6) or 4×128 (layer 3) strips on the n-side. Each of the 128 strips is read

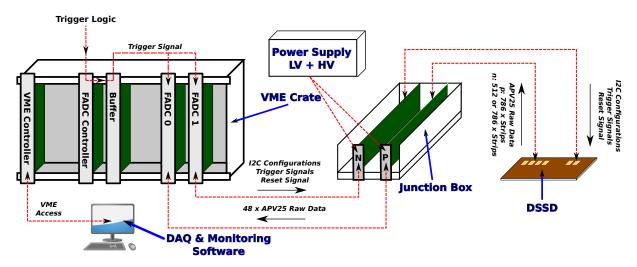


Figure 2.8: Readout chain of the SVD system. LV denotes low voltage applied to the APV25s and HV the high voltage, that supplies the sensor with the reversed bias for full depletion.

out by an APV25 chip. Upon receiving a trigger signal a buffered set of data is sent to the readout chain, figure 2.8. This system is also known as FADC system and consists of the following parts:

APV25

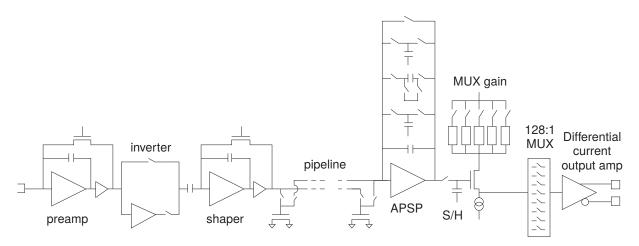


Figure 2.9: Block diagram of APV25 [7].

The APV25 chip, figure 2.9, is the first readout component and is directly mounted on the sensor. The chip has 128 readout channels. The first electric component of each channel consists of an integrating amplifier with an integration time of 50 ns. The polarity of the amplified signal can optionally be inverted. The CR-RC shaper turns the integrated charges into a pulse shape, where the amplitude is proportional to the collected charge. The processed signals are stored in a pipeline (actually a ring buffer) with a depth of 192 cells. Up to 32 of the cells can be marked for readout. The APV25 operates with 2 modes: In the deconvolution mode a switched capacitor filter performs a 3-weight deconvolution.

In peak mode, the only mode which can be used for the SVD system, the data consist of shaper pulse samples. Finally with an integrated multiplexer (MUX) the 128 channel data are merged into one line with a differential current output. The APV25 chip can be configured with I2C inputs. A dedicated trigger line performs the desired functions upon receiving 3 consecutive binary signals:

- [100] trigger signal: The APV25 reads the internal ring buffer at the position of the read pointer. Depending on the I2C configuration one or tree shaper pulse samples are read out. The address of the internal buffer is also decoded in a 8-bit word inside the output data, that can be used to determine if all APV25s are synchronized. A dedicated error flag inside the output data indicates if an error has occurred.
- [110] calibration request: The APV25 injects a defined amount of charge into the electrode connected to the pre-amplifier. The next calibration request inverts the polarity of the injection. The magnitude and timing are programmable with I2C commands. This function is primarily used to sample the pulse generated by the CR-RC shaper and to determine defects of the readout channel and connected strip.
- [101] reset: The reset signal resets the error flag and any pipeline pointer and relaunches them with the given latency. After sending a reset signal the APV25 needs 11 clock cycles to perform the reset and additionally the configured amount of latency to correctly set the pointers of the internal ring buffer. A trigger signal in this time period generates a latency error that raises an error flag.

For a more detailed description of the APV25 chip see [7] and [11].

Junction box

The junction box contains several junction boards, that form a bridge between the front-end electronics (APV25 and DSSD) and back-end electronics (9U VME crate). Additionally it connects the sensor and APV25 chips with the corresponding power supplies. Due to the different polarity of the bias voltages each board connects one side of at most 8 DSSDs. The junction board is introduced to break the cables directly connecting to the strip sensors. Additionally it contains two radiation hard DC/DC converters, one set for operation and one set as backup. The DC/DC converters provide the supply voltages (+1.25V and +2.5V) to the APV25 chips.

FADC controller and buffer board

The main task of the FADC controller is to distribute the trigger signal to the APV25s. The generated triggers are sent through each FADC to the trigger line of the front-end chips. In order to set a constant timing of each signal pattern, the FADC controller has an implemented signal sequencer, that can be represented as a two dimensional array. The first index indicates the type of signal, the second one the timing within 256 clock cycles. This implementation allows a constant pattern that is required by some of the configuration runs. Since there is only one FADC controller and several VME crates the signal patterns are distributed via with the buffer boards in each create.

FADC

The FADC board is the central control and data processing component of the SVD readout chain. Each board supports 48 APV25s and converts the analog inputs to digitial data. The data processing is done by a powerful FPGA (Altera Stratix-IV). The processed data are forwarded to the Finesse Transmitter Board (FTB), where the electrical signals are converted into optical ones. The optical data in turn is sent to the Belle II DAQ system and in parallel a duplicate of data is forwarded to the DATCON (data concentrator) system, which performs online tracking and calculates the regions of interest (ROI) for the pixel detector to reduce their data output. A sample of the main data stream is copied

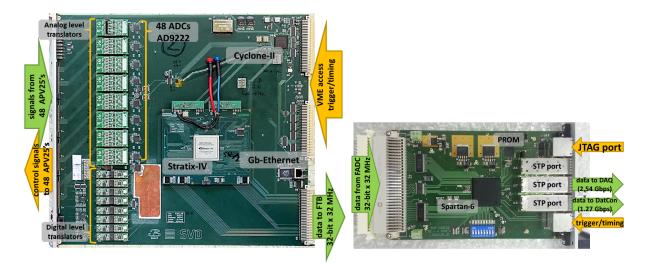


Figure 2.10: FADC and FTB boards. Note: The sizes of the depicted board are not in scale.

to a so called SPY FIFO on the FADC board, which is read out via VME bus (later: via Gigabit Ethernet) and used for online monitoring and standalone operations.

The following list shows the run modes of the FADC board, sorted by the degree of processing:

• Raw mode

The data consists of the raw output of the APV25 chip, see figure 2.11. In an idle state the APV25 chip periodically produces so called tick marks. Upon receiving a trigger signal the next tick mark is overwritten by the following logical signals: 3×1 header bits, 8 address bits indicating the read position of the internal buffer and 1 error bit with 1 representing no error. The next 128 analog data points consist of a sample of the shaping curve with integration time of 50 ns from each 128 strip. Due to the four-stage multiplexer of the APV25 output circuit, the strip data in the raw data frame are not consecutive and the ordering is described by the following equation:

$$i = 32 \cdot (j \text{ MOD } 4) + 8 \cdot \left\lfloor \frac{j}{4} \right\rfloor - 31 \cdot \left\lfloor \frac{j}{16} \right\rfloor$$
 (2.11)

with i representing the strip number and j the position in the raw output. MOD denotes the modulo operation. In multi peak mode three consecutive sets of shaper

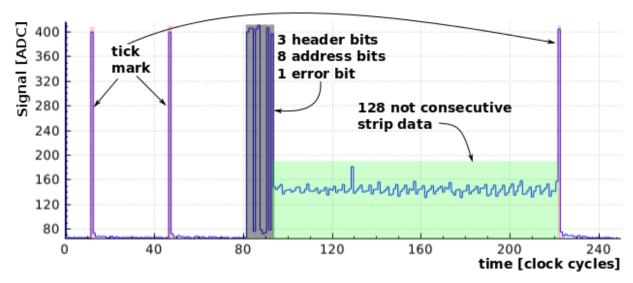


Figure 2.11: Raw APV25 output in single peak mode (see text for description). Note: All strip signals (green shaded area) are recorded at the same time.

curve samples are taken. By sending two consecutive triggers in that mode signal six frames can be generated, see figure 2.12. Since each frame contains only one

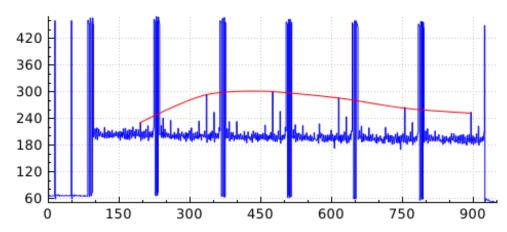


Figure 2.12: Raw mode data with six frames of the shaping curve (red line; the shaper pulse is stretched, since each frame comprises of the strip signals at the same clock cycle.). The peaks inside each 128 strip data indicate the signal level of the corresponding APV25 channels. The number of charges generated by an traversing particle is proportional to the maximum of the curve.

sample of the shaper pulse, at least three frames are needed to find the maximum that correlates to the collected charge.

• Transparent mode

The FADC performs a header detection (figure 2.11: gray shaded area) and reordering of the strip samples (figure 2.11: green shaded area). The output of each event consists of the extracted 128×number of sampled data points. Additional information is coded in the corresponding 32 bit header/trailer words.

• Zero suppressed mode

In addition to the transparent mode, signal correction and zero suppression, see section 3.2.2, are also performed. The output consists of the strip signals that are over a predefined threshold, that can be configured for each strip individually.

• Zero suppressed and hit time mode

This run type is not yet implemented. After signal correction and zero suppression has been performed, the FADC continues with hit time finding, the position of the maximum of the shaper pulse. Recent studies performed by R. Frühwirth indicate that a forward feed artificial neural network (ANN) yields a better convergence than traditional fitting algorithms using steepest decent methods. Furthermore the evaluation of ANN is constant in time and easier to implement into the firmware.

VME controller

All boards and APV25 chips are configured with dedicated VME addresses. The communication is performed by a VME controller, that can be accessed by a PC. A standalone software named TuxDAQ has been written to access the functionality of the hardware for configurations and reading the data buffered in the SPY FIFO. The data in turn are sent via a socket to the online monitoring tool called TuxOA for processing and determining parameters necessary for certain run types and run modes. The next chapter provides a brief overview of the two software systems.

Chapter 3

SVD control software and online monitoring

One of the requirements was to split online monitoring from the control software. To this end 2 standalone applications, TuxDAQ and TuxOA, have been developed. The main task of TuxDAQ is to apply the configuration required for each run type to each hardware component and to send the data, read out from the SPY FIFO, via a socket to TuxOA for online monitoring.

3.1 TuxDAQ

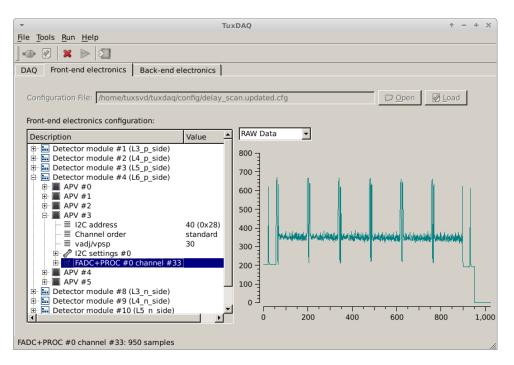


Figure 3.1: Screenshot of TuxDAQ.

The first version of TuxDAQ was written in C++ by Thomas Obermayer during his master thesis [13]. His code was designed for the SVD3 system, a precursor of the current

FADC system used for the Belle II experiment. At that time only 2 run types were implemented:

- Pedestal Run: The trigger signal is issued by TuxDAQ. The data containing empty events (without a particle beam) are used to calculate the pedestal and noise of each strip.
- Hardware Run: Trigger signals are generated by an external source.

The control flow of the system is based on Model-View-Control pattern (MVC), where each component has a dedicated task. The model provides data for the View object to display. The user input is interpreted by the control object. The control object is designed as a finite state machine (FSM) [13]. The control flow of the system delegated by the FSM can be summarized by the following figure 3.2. The run specific settings are applied



Figure 3.2: Control flow of TuxDAQ.

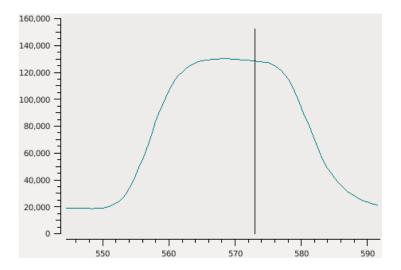
during the initialisation of the VME boards and the configuration of APV25 chips. After all configurations have successfully been set, the TuxDAQ starts the data acquisition. Depending on the run type additional configurations at certain number of events are set to scan for the properties of the system. During the configuration runs the whole set of data is sent to TuxOA for online processing. Only a fraction of the acquired data depending on the buffer size of the socket - is forwarded for monitoring. The functionalities at each step delegated by the control object are implemented in the model, which supplies the view with data for presentation. The model also encapsulates the communication of the hardware components mentioned in the previous chapter and represents the core of the application. The design heavily relies on mapping of each hardware component to a software object, therefore creating unnecessary complexity, that originates from the hardware layout.

In order to adapt to the latest FADC system the structure of the hardware and the access logic had to be modified. For a more detailed description of the changes, see appendix A.1. In the latest TuxDAQ software following run types have been (re)implemented:

3.1.1 ADC delay scan

The ADC delay scan determines the optimal delay for each ADC sample clock. The delay configuration depends strongly on the length of the connected cables as well as on the clock frequency of the APV25 chip. An optimal delay value is determined by sampling the tick mark of the APV25 output. At an operation frequency of 32 MHz the delay scan ranges from 0 to 64 with 0.5 ns step size. In order to suppress random noise, 300 events are taken at each step to yield the mean height of the sampled tick mark. The resulting curve is shown in figure 3.3. The optimized delay value (figure 3.3: black line) is located at the left of FWHM point plus 60% of its width. In the current FADC system a maximum of six APV25s are connected to one ADC chip. Thus a truncated mean of all chips of one

Figure 3.3: Tick mark sampled with different delay configurations of a single APV25 chip (green line). The vertical axis shows the sum of the signal over 300 events in units of ADC counts and the horizontal axis the delay in arbitrary units. The black line marks the computed delay setting.



converter is applied as a delay setting. The deformation of the scanned tick mark shows the influence of dispersions and reflections in long cables. In order to compensate for this effect a FIR filter is applied. The needed configurations and the operations applied on each set of data are discussed in the following section.

3.1.2 FIR filter

In the cables, the frequency response is not constant. This signal components with a higher frequency are more damped compared the ones at lower frequencies. This effect causes the initial signal to be distorted, see figure 3.3. Additional deformations are induced by small reflexions, depending on the length of the cable.

The most significant impact can be seen in strip signals following the error bit. A noticeable part of the error bit contaminates the following signals, that creates reoccurring peaks in the noise map of the APV25. The affected strips are usually: 0, 32, 64, 96.

In order to suppress this effect a finite impulse response (FIR) filter has been implemented in the firmware of FADC board. The FIR filter run determines the 8 coefficients c_i needed for the signal correction. The FADC in turn applies the constants described in the following equation: $s_n = \sum_{i=0}^8 c_i s_{n-i}$, with s_n representing the current signal and s_{n-i} the previous signals.

The distorted output \mathbf{S}' can be expressed as a transformation \mathbf{H} of the input signals \mathbf{S} , $\mathbf{S}' = \mathbf{H} \cdot \mathbf{S}$. Assuming $S_0 = 1$ and $S_{i\neq 0} = 0$, \mathbf{H} can be simplified to a triangular matrix.

$$\mathbf{H} = \begin{pmatrix} S_0' & 0 & 0 & \cdots \\ S_1' & S_0' & 0 & \cdots \\ \vdots & \vdots & \ddots & \cdots \\ S_n' & S_{n-1}' & \cdots & S_0' \end{pmatrix}.$$
 (3.1)

The coefficients of the FIR filter are the elements in the first column of \mathbf{H}^{-1} . In order to set the initial values of \mathbf{H} , the FIR filter run averages the tick mark and seven consecutive points over 1000 events. After the subtraction of the baseline, \mathbf{S}' can be represented by the sampled points and the filter coefficients are obtained by matrix inversion. The evaluated constants are in turn uploaded to the FADC boards.

3.1.3 Calibration

The main purpose of the calibration run is to find defect strips and to estimate the gain of each strip. Using the calibration request [110], a predefined charge, usually corresponding to a particle signal of about 22400 electrons, is injected into the preamplifier of the APV25. The shaper output is not directly accessible, but can be reconstructed from individual samples taken with different delays of the APV25 and a dedicated latency of the calibration module with a resolution of 1/8 of a clock cycle. Figure 3.4 shows the curve sampled with the calibration run. The maximum of the samples is proportional to the injected charge. Every 8th strip is scanned at the same time. A small fraction of

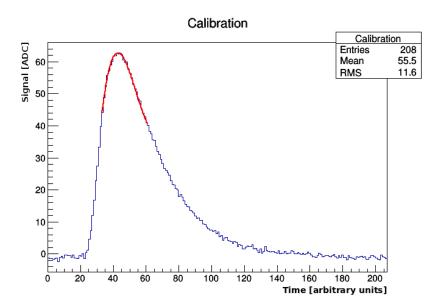


Figure 3.4: Shaper pulse sampled with a calibration run (blue line). The red line represents a fit with a polynomial of third order to estimate the maximum.

the injected charge is coupled to the adjacent strips and capacitively shared among its neighbours, see figure 3.5.

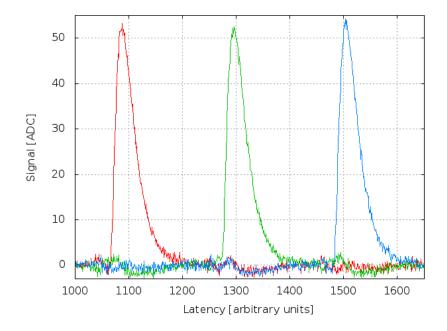


Figure 3.5: Shaper pulse of three neighbouring strips.

3.1.4 Sixlet calibration

The sixlet calibration run is similar to the calibration run. The main task of this run type is to provide a set of training data for the artificial neural network (ANN) for hit time estimations. To this end the generated shaper pulse is sampled with six frames of strip data at various timing and amplitude settings.

3.1.5 Runs with external triggers

The different run types mentioned in the previous subsections are configuration runs, that determine the system properties. Those run types are designed in such a way that an interaction with an external trigger is not permitted. The run types discussed in this subsection use different trigger sources and interactions with the main Belle II data stream.

- Local hardware run: The triggers are issued by an external source connected to the LEMO input of the FADC controller board. After receiving one trigger signal the following triggers are blocked until the software is ready to record the next event. This run type is used to test the system without the Belle II readout chain, e.g. with a source in the lab or in a standalone beam test.
- Hardware run: After resetting the resetting the trigger veto flag in the FADC controller, that blocks incoming triggers TuxDAQ only interacts with the so called SPY FIFO, where samples of the main Belle II data stream are buffered. The buffered data in turn are readout by TuxDAQ and forwarded to TuxOA via a socket for online monitoring.

The triggers are issued by the front-end timing switch (FTSW), which also distributes the clock and command signals issued by the Belle II DAQ. The acquired data are in turn forwarded by the FADC to the FTB, that convert the digital data into optical signals. At the next stage the data stream is forked to the COPPER system, a part of Belle II DAQ and to the DAQCON system, that calculates the ROIs for the pixel detectors. Finally a high level trigger (HLT) system decides if the data is going to be recorded.

The data sampled by both run types are also locally recorded by TuxDAQ for debugging and offline analysis.

3.2 TuxOA

TuxOA is written in C++ and designed for a Linux system. Its main tasks are:

- to determine configuration parameters from the data acquired by TuxDAQ and
- to perform simple analysis for online monitoring.

The logic of analyser modules are based on HAT[8] and APVDAQ[7, 9], that were designed for the SVD3 system. The following subsections provides an overview of the software layout and the analysis of data.

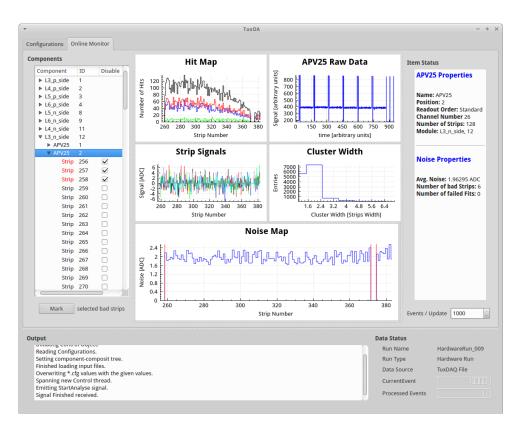


Figure 3.6: Screenshot of TuxOA.

3.2.1 Overview

The main task during the design was to keep the system as modular as possible. To this end the system is split into the following components each with a dedicated task:

- DataTransfer reads the input data either from a file or socket and converts them to a format readable by the analysers.
- AnalyserTask contains a list of analysers that perform the analysis of one side of a detector. After the configuration the created AnalyserTasks are moved to the corresponding thread object, that carries out the analysis upon receiving a start signal.
- ResultContainer provides the storage of the data analysed by each thread as well as the raw input data. The structure of the ResultContainer reflects the physical layout of each APV25 connected to one side of the sensor.
- QtView shows the analysed data stored in the ResultContainer for the user. It provides a graphical user interface written in Qt4 for user defined configurations and run control.
- Configure stores the configuration of the run. Additionally it creates the structure of the ResultContainer, ie. which APV25 chip is connected to the sensor.
- Control defines the communication between each component and delegates their functionalities.

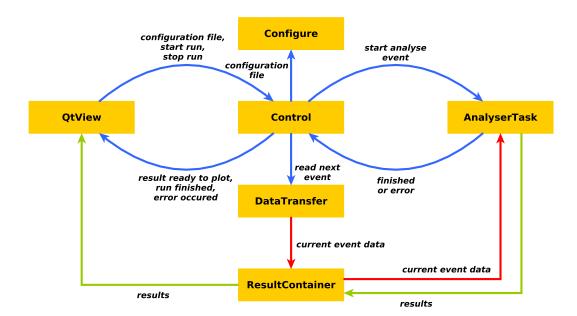


Figure 3.7 shows an overview of the communications between each component. After each

Figure 3.7: Interactions of each component of TuxOA. The blue line represents the functions delegated by the Control object. The red and green lines mark input/output of raw data and results respectively.

component has been initiated, the application proceeds with the following steps: TuxOA waits until the next event can be read. Then the incoming raw data depending on the operation modes of the FADC is converted to a format that can be read by the analyser in the AnalyserTask object and in turn is stored in a dedicated queue. The control starts all threads that perform the analysis of the buffered data. After all data have been processed the control checks if an update has been requested. At each update only a part of the data is sent to the QtView object. Depending on the selected component (module, APV25 or strip) a set of predefined plots is displayed. The run continues by reading the next event. The results of each event are recorded in a Root file, that allows the sampling over a certain region of each sensor.

The scalability of the current system is strongly limited by the data layout in the memory that causes cache misses with increasing number of APV25s. In order to circumvent this effect the data structure has to be redesigned.

3.2.2 Signal corrections

Depending on the run mode signal corrections already have been applied by FADC to the data recorded by TuxDAQ. This type of processing is usually applied to the raw mode. The signal S of a certain strip i and event j consists of:

$$S_{i,j} = S_i^{\text{ped}} + S_j^{\text{cm}} + N_i + S_{i,j}^{\text{part}}$$
 (3.2)

with S_i^{ped} denoting the pedestal, S_j^{cm} the common mode, N_i the uncorrelated noise and $S_{i,j}^{\text{part}}$ the particle signal. In order to calculate the pedestal and noise of each strip an

random trigger run with usually more than 5000 events is taken with one frame of strip data. The applied signal corrections are listed in the following:

Pedestal

The first few events recorded by a software run are taken to calculate the pedestal of each strip. The pedestal represents the mean signal height. Usually 1000 events are used to sample the mean value. Figure 3.8 shows the pedestal values of the L3 p-side sensor with 6 APV25s. The slope of the pedestals within 128 strips is caused by an internal supply

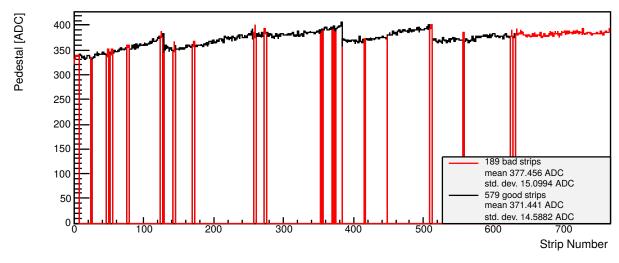


Figure 3.8: Pedestal of L3 p-side with 6 APV25 chips. The red bars mark defect strips. The last APV25 chip (from strip number 640 to 756) was disconnected from the sensor and thus fully labelled as defect.

voltage drop across the chip. After the evaluation of the pedestals, the pedestal values are subtracted from the strip signals are subtracted with the pedestal value to yield the common mode and noise of each strip.

Common mode

The common mode is the common fluctuation of 128 strips within an APV25 chip around their pedestal value. In order to compensate for this effect the strips are usually divided into 4 sections, each containing 32 consecutive strips. The common mode is the truncated mean value of each section. The truncation cuts off 25% of the highest and 25% of the lowest signals to avoid a bias by particle hits, while the remaining 50% are used for the mean evaluation.

An example of common mode corrected data is shown in figure 3.9. The RMS of common mode is usually smaller on the p-side than on the n-side of the sensor, since the way in which the APV25 chip is operated on the p-side (inverter between preamplifier and shaper is turned on) already performs a common mode correction internally as a side effect.

The current implementation of common mode correction only accounts for constant shifts of the signals caused by the coupling of the strips to the sensor and to the externally

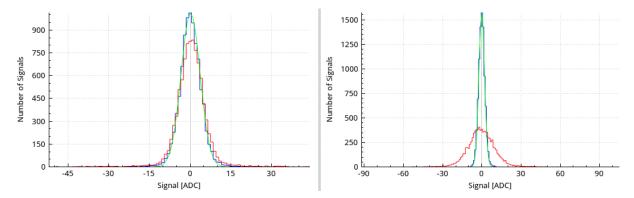


Figure 3.9: Signal distributions of pedestal subtracted data (red) and of common mode corrected signals (blue). The green line shows a fit with a normal distribution. Plots are generated with the pedestal run number 10 taken at DESY and sensor L5 p-side (left) and n-side (right). Due to the effective APV25-internal common mode correction on the p-side, there is hardly any difference seen on the left plot, while a significant amount of common mode is present on the n-side.

induced noise. The first few strips at the edges of the DSSD couple to a different capacitive network compared to the centre strips. By applying the correction over 32 strips it shows a decreasing noise towards the centre strips. Additionally those strips are more prone to externally induced noise. The resulting pedestal subtracted signal distribution shows either multiple peaks or an elongated tail on both sides of the distribution. The amplitude of the secondary peaks decrease towards the centre strips. The number of affected strips at the edges usually ranges from 8 to 10 strips.

Noise

The noise of each strip is the standard deviation of the Gaussian distributed signals after pedestal subtraction and common mode correction. In order to yield better convergence the fit with the normal distribution is performed within the FWHM. Strips with a noise value greater than $2.5\times$ the mean noise of the corresponding APV25 are marked as bad. Those strips are excluded from further evaluations. Figure 3.10 shows the noise map of the L4 sensor.

3.2.3 Clustering

A cluster consists of several consecutive strips, that detect the signal generated by an impinging particle. The data usually consists of 6 frames to distinguish uncorrelated noise from a particle signal. In order to find a cluster the following signal to noise (SNR) ratio thresholds are applied:

- 1. **Seed threshold**: A strip's SNR exceeding this threshold is marked as a seed strip and triggers the cluster search in its vicinity. The default value is 5.
- 2. **Neighbour threshold**: The strips neighbouring the seed strip are added to the cluster, if their SNR exceeds the neighbour threshold that is usually set to 3.

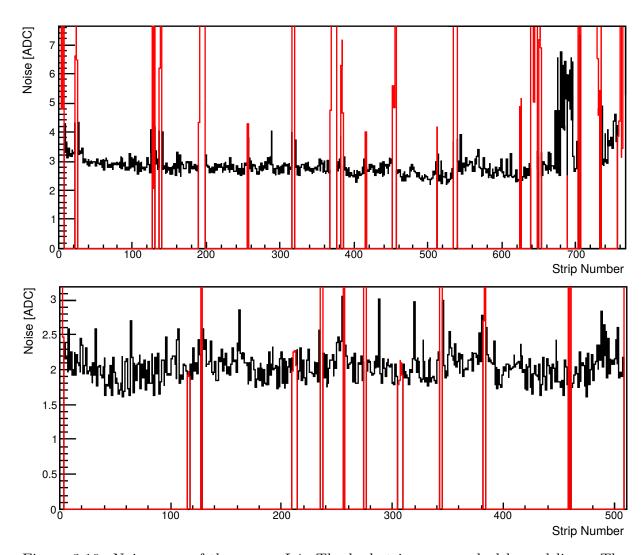


Figure 3.10: Noise map of the sensor L4. The bad strips are marked by red lines. The upper plot shows the noise values of the p-side strips and the lower one the n-side. The elevation at strip number 680 is caused by a defect sensor region that has not been automatically detected by TuxOA.

- 3. Cluster threshold: The SNR of the cluster $SNR_{cl} = \frac{\sum S_i}{\sqrt{\sum N_i^2}}$ has to be greater than 5, otherwise the found cluster is rejected. S denotes the signal of the strip i and N_i the corresponding noise.
- 4. **Hit length**: In order to distinguish random noise, that exceeds at least one of the first 2 thresholds, at least 3 consecutive strip signals have to exceed the neighbour threshold.

At the beam test the incident angle is usually perpendicular. The 5-3-5 SNR thresholds with a hit length of 3 yield reliable results. With increasing angles a part of the particle signal might be cut off by the neighbour threshold. In order to circumvent this effect the neighbour threshold may need to be reduced. To yield better estimation of the signals generated by an incident particle, clusters adjacent to bad strips are discarded in the lab and beam test analysis.

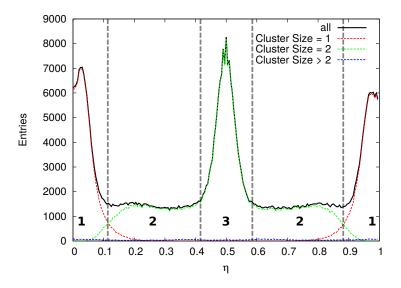
3.2.4 Position of the particle

The position of the particle can be determined by the centre of the charge gravity (COG):

$$x_{\text{COG}} = \frac{\sum_{i} \mathbf{x}_{i} \cdot \mathbf{S}_{i}}{\sum_{i} \mathbf{S}_{i}} = \mathbf{x}_{0} + \mathbf{p} \cdot \frac{\sum_{i} i \cdot \mathbf{S}_{i}}{\sum_{i} \mathbf{S}_{i}} = \mathbf{x}_{0} + p \cdot \eta,$$
(3.3)

with x_i representing the position of the i-th strip of the cluster, S_i the corresponding strip signal and p the distance between 2 readout strips. η shows the particle position weighted with the corresponding signal in units of inter strip distances. The applied bias voltage creates a strong electric field that forces the created charge carrier cloud to drift towards the strips. At narrow incident angles the majority of charges are collected by only one or two strips, thus affecting COG. The non uniform position distribution can be demonstrated by sampling the decimal places of x_{COG} in units of inter strip distance, as shown in figure 3.11. The resulting histogram shows 3 distinct regions. Region 1 is

Figure 3.11: Histogram of inter strip positions with an intermediate strip, where the incident angle is nearly perpendicular. The black line shows the distribution of all cluster sizes. The dotted line represents the different contributions depending on the cluster size. This plot is generated with the data of sensor L3 n-side taken at the lab of HEPHY using Sr⁹⁰ as a particle source.



dominated by clusters with one strip (red line). To account for capacitive coupling between the strips and particle signals that are below the neighbour threshold, neighbouring strip are added to the η calculation, if their signals at the peaking time are positive. This region does not yield any position information. Assuming a uniform distribution the error of the position becomes $\frac{P}{\sqrt{12}}$. However the positions of the peaks show the interplay of the particle signals lost by applying the neighbour threshold and capacitive coupling between strips. The width is proportional to the inverse of the signal to noise ratio. The difference of the amplitude roughly scales with the angle of the sensor plane and the incident beam. Region 2 is dominated by clusters containing 2 strips, where charge sharing occurs. The peak at $\eta=0.5$ in region 3 is caused by an intermediate strip, where the majority of the particle signal is collected by the intermediate strip and capacitively read out by its neighbouring readout strips.

Overall the non uniform charge sharing introduces a systematic shift of the particle positions in region 2 for narrow incident angles. In order to compensate for this discrepancy the η correction can be applied. The sampled histogram, figure 3.11, represents the measured probability density function $f(\eta)$. The distribution $F(\eta)$ is determined by the integral of $f(\eta)$, figure 3.12. The applied correction for region 2 reads:

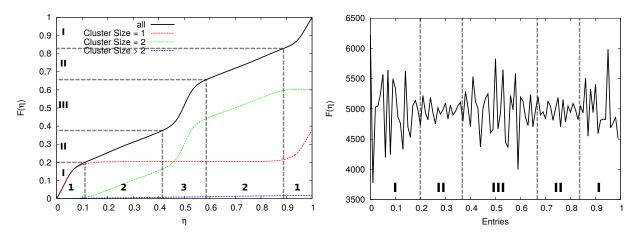


Figure 3.12: η correction. Left: The distribution function $F(\eta)$, black line. Right: Corrected inter strip positions.

$$\mathbf{x}_{\eta} = \mathbf{x}_0 + p \cdot \mathbf{F}(\eta) \quad \text{with} \quad \mathbf{F}(\eta) = \frac{1}{N} \int_0^{\eta} \mathbf{f}(\eta') \, d\eta'$$
 (3.4)

The resulting inter strip distribution is shown in figure 3.12. For incident angles close to 0° the η correction improves the resolution considerably. With increasing angles the charge sharing becomes more linear and the 3 peaks less pronounced. In this case both η correction and COG approaches the same resolution $\sigma_{\rm x} \sim \frac{p}{\rm SNR}$ with the SNR denoting the signal to noise ratio.

Chapter 4

Beam test at DESY

In January 2014 an integration test of BELLE II DAQ, PXD and SVD was performed at DESY (Hamburg) with an electron beam at a momentum of 2 to 6 $\frac{\text{GeV}}{\text{c}}$ with a typical rate of a few kHz/cm². The beam passes through a solenoid magnet, where the field strength reaches up to 1 T. The setup at DESY was the first beam test involving the SVD and the PXD detectors. The main task was to perform an integration test of the two sub-detector systems, that form the vertex detector VXD, and the BELLE II DAQ.

4.1 Setup

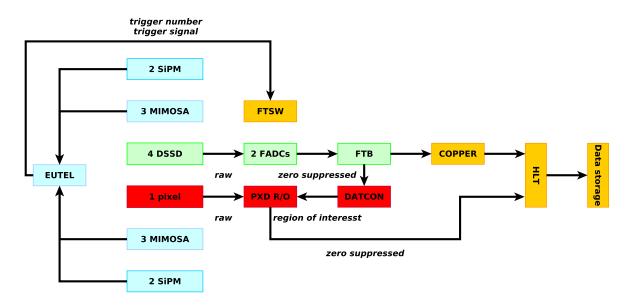


Figure 4.1: Overview of the readout chain at DESY. The orange boxes show the components of BELLE II DAQ, the green boxes the SVD and the red boxes the PXD system. The 3 MIMOSA detectors are independently read out by EUTEL system.

Figure 4.2 shows the beam test setup. Inside the solenoid magnet and parallel to its magnetic field lines, one plane of the pixel detector and four DSSDs were installed in a black box, where the layers had the same distances as in the future BELLE II detector.

The black box is attached onto a telescope composed of 3 MIMOSA pixel detectors on each side of the VXD detector. Figure 4.2 shows the alignment of the mentioned sensors with a fitted track. The telescope system is controlled and read out by the EUTEL system

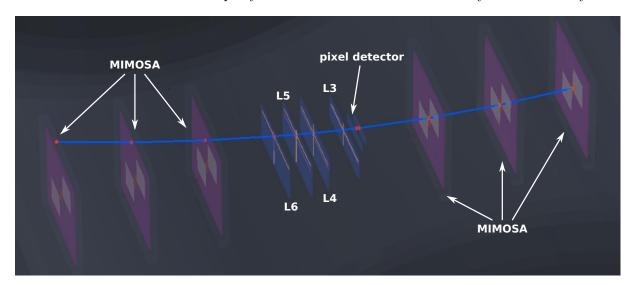


Figure 4.2: Alignment of all sensors. The n-side of all DSSDs was facing the pixel detector. The blue line shows a fitted track. The figure is adapted from [3].

which is not a part of the BELLE II setup. The trigger inputs are generated by three silicon photomultiplier (SiPM) with two of them mounted on each end of the telescope. One of the SiPM was defect and had to be masked out in the trigger logic unit provided by the EUTEL system. The trigger signal is obtained from a configurable coincidence of the scintillator outputs and sent to the front-end timing switch (FTSW), that in turn distributes the signal to the VXD.

Upon receiving the trigger, both systems, SVD and PXD, read out the data from their front-end buffers, perform signal correction and zero suppression. The event captured by the FADC system is forwarded to the corresponding FTB that in turn distributes the data among the COPPER and the DATCON systems. The main task of COPPER is to collect the data of the SVD and to forward them to the readout PCs that process the event to yield a high level trigger (HLT). Depending on its result the event taken by PXD and SVD is stored on the disk for offline analysis. The second parallel data stream of the FTBs is processed by DATCON which performs a fast track finding to approximate the particle positions on the pixel detector by extrapolation. The signals in the vicinity of those positions are read out and forwarded to the offline storage. The EUTEL system runs independently from the BELLE II setup. The data recorded by the BELLE II DAQ are synchronized by the trigger number generated by the EUTEL.

The SVD readout chain, figure 4.3, consists of four rectangular DSSDs, two junction boards, two FADCs and an FADC Controller. In this setup the sensors are arranged with the same spacing as it will be used in the Belle II experiment for the SVD layers 3 to 6. Hence it represents a fraction of the barrel part of the Belle II SVD. The geometry is given in table 4.1. The four DSSD modules are early prototypes of the future SVD system and have already been used for previous beam and irradiation tests. Thus, a few hotspots were known. Each side of the sensor is connected to one of the junction boards, that in turn forward the data to the corresponding FADCs. The FTB system is attached

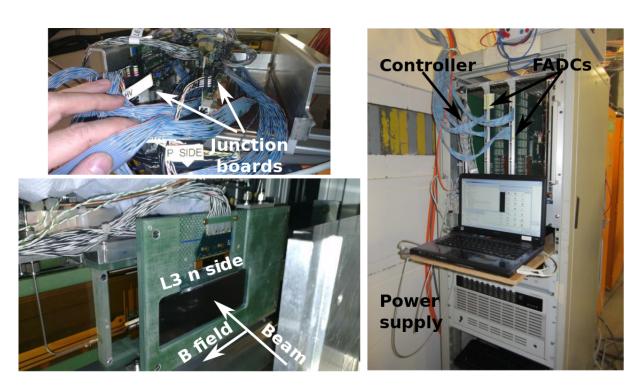


Figure 4.3: SVD readout chain.

layer	sensor	sensitive	$\# \ \mathbf{APV25}$	$\mathbf{pitch} \; [\mu \mathrm{m}]$
	name	$area [mm^2]$	(n/p-side)	(n/p-side)
3	L3	122.8×38.4	6 / 6	160 / 50
4	L4	122.8×57.6	4 / 6	240 / 75
5	L5	122.8×57.6	4 / 6	240 / 75
6	L6	122.8×57.6	4 / 6	240 / 75

Table 4.1: Geometry of rectangular sensors.

to the back-side of the FADCs and only works with zero suppressed data. To this end all the runs with the beam were taken with zero suppression containing six frames of strip data and using a signal threshold of $5 \times \text{strip}$ noise.

During the beam test, the following run modes were used to record data:

- Pedestal run: In this mode the data are generated with triggers issued by the software. This run type is usually performed with 1 frame of strip data and without the beam to evaluate the pedestal and the noise of each strip. Each run usually contains 10000 events. While 1000 events are used to evaluate the pedestals, the remaining events are used to calculate the noise levels.
- Calibration run: For this run type a built-in circuit of the APV25 chip is used to inject a defined amount of charge into each amplifier input of the chip. For each channel the output signal of the APV25 chip is sampled. The resulting waveform is used to determine the gain of each strip. Moreover, waveform, timing and amplitude of the sampled signals are used to identify defect or noisy strips.
- Hardware run: The hardware run is designed to record data of beam particle hits. The FADC boards are operated in zero suppressed mode, the trigger signal for data taking is obtained from the FTSW and all the data are sent to the DAQ system via the FTB boards and the Copper system. TuxDAQ only samples a fraction of the data buffered in the SPY FIFO. In this case the data format has to be in zero suppressed mode in order to avoid buffer overflow of the FTB boards and to provide suitable data to the DATCON system. Usually a SNR threshold of 5 was applied during data taking in zero suppression mode.

4.2 System properties

4.2.1 Defect strips

During the beam test pedestal, and calibration runs were frequently performed to determine the properties of the sensors with different external configurations and to find bad strips associated with the defects of the DSSDs. Defects of detector strips - opens, shorts or pinholes - typically widen the signal distribution of the affected channels and thus result in higher noise levels. By comparing the noise to the average of the APV25 chip the mentioned defects can easily be detected. Additional bad strips can be found by comparing the amplitude of their calibration pulses to the mean value within the APV25 chip.

Other sensor defects can affect more than one strip. A fraction of the noise is coupled to the adjacent strips, see figure 4.4. The resulting noise of the neighbouring strips decreases with the distance and usually impacts up to two adjacent strips on each side. The effects of the induced noise on the neighbouring strips can be seen in the signal correlation plots, shown in figure 4.5. The signals distributed along the diagonals show the impact of the defect strip. With increasing distances the correlation becomes more circular. A cut along the vertical (x = 0) and horizontal axis (y = 0) of the signal correlation yields similar noise levels compared to the average within the APV25 chip, indicated by the black circle in figure 4.5. While the signal correlations of strips adjacent to the defect one are positive, the correlations between the defect strip and its neighbours show negative values.

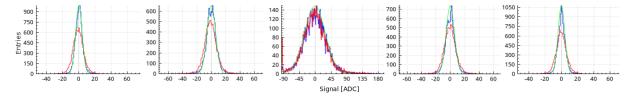


Figure 4.4: Signal distribution of a defect strip (centre) and its adjacent neighbours. The plots show a defect region from sensor L4 (p-side) ranging from strip number 21 (left) to 25 (right). The red line shows the pedestal subtracted data and the blue line the data after common mode correction. The green line represents a Gaussian fit.

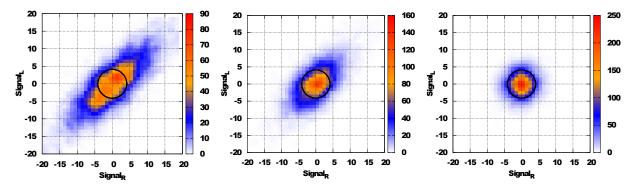


Figure 4.5: Signal correlations of strips adjacent to the defect strip 24. Left: strip 23 and 25. Centre: strip 22 and 26. Right: strip 21 and 27. The radius of the black circle represents the RMS = $\sqrt{\frac{1}{N}\sum_{i}(S_L^2 + S_R^2)} = 4.12$ ADC of the right plot.

4.2.2 Systematically induced noise

At the beam test we have experienced several noise problems, discussed in the following section 4.2.3. In order to distinguish the systematic noise from the externally induced one at DESY, the clustering algorithm with lowered thresholds, see section 3.2.3, has been applied to the data taken with the software run in the lab of HEPHY. The used configurations are recorded in the table 4.2. The noise values used for the clustering algorithm has been evaluated with a common mode correction (CMC) with 32 strips. In order to keep the shape of the noisy events, the CMC for the cluster finding has been set to 128 strips. By setting the maximum cluster width (CLW) to 3 strips, region affected by the external disturbances can be mapped.

The resulting hit maps with different CLWs are shown in figure 4.6. The L3 sensor shows a nominal behaviour, where the clusters containing 2 strips (red line) are evenly spread over the whole sensor. The accumulation of clusters with CLW = 3 only occurs at the edges of the DSSD, caused by the coupling of the border strips to a different capacitive network compared to the center strips. The number of strip signals over 1 SNR threshold including all cluster sizes yield an expected count of about 1580 out of 10000 events. The remaining sensors from layer 4 to 6 show a distinct behaviour at certain regions of the cluster map containing strip clusters with a CLW = 2, 3. The accumulations at the borders of the common mode section with 128 strips, most visible on the fourth APV25 chip on the p side, indicate a more complex common mode structure throughout the chip. Further more the reoccurring peaks of clusters with CLW = 3 at roughly the same

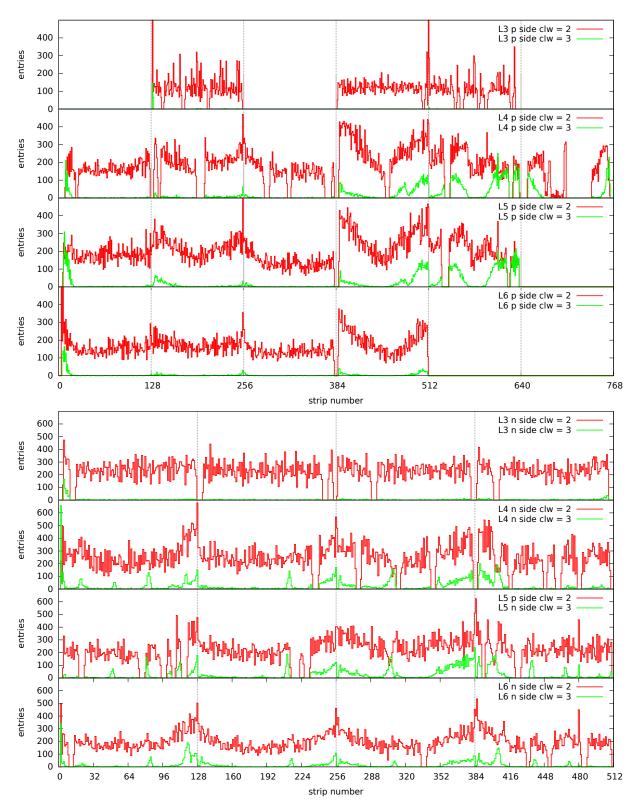


Figure 4.6: Areas affected by noise. The red line marks clusters containing 2 strips and the green line clusters containing 3 strips. The gaps indicate the defect strips and disconnected APV25s. The vertical gray lines show the borders of each APV25 chip. Each plot is generated with 10000 events containing 1 frame of strip data. The data is taken at the lab of HEPHY and the configurations of the evaluation are described in the text. Note: The strip number of L3 n side has been shifted by -128 to fit the results into the plot.

39

configuration	value	
pedestal and noise		
number of events used to evaluate pedestal	1000	
number of events used to evaluate noise	9000	
common mode section	32	
noise strip cut	$1.5 \times \text{mean noise}$	
clustering		
common mode section	128 strips	
seed threshold	1 SNR	
neighbour threshold	1 SNR	
cluster threshold	1 SNR	
max cluster size	3 strips	

Table 4.2: Configuration used to map the regions with enhanced signal correlations and the level of induced noise.

position suggests a systematically induced noise. By applying a CMC with 32 strips the mentioned accumulation becomes less noticeable, however the peaks of the cluster with CLW = 3, that are not located at the borders of the CMC sections, still remain. Most of those regions can be found on the n side. The affected strips usually have an asymmetric signal distribution with a slightly elongated tail towards greater signals.

Figure 4.7 shows an example of the induced noise signal with 6 frames of strip signals at the same event, which causes the additional peaks. Except for the L3 sensor the noisy signals occur on each APV25 at the same event and usually at the same data frame. The

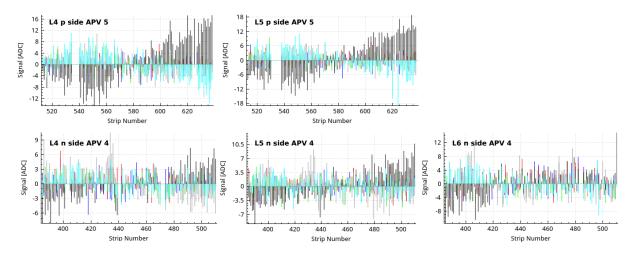


Figure 4.7: Strip signals at the same event after pedestal subtraction and common mode correction with 128 strips. The plots are generated with 6 frames of strip data with the black line representing the 4th frame and the cyan line the 5th frame. The data are taken at the lab of HEPHY after the beam test.

most probable noise signal (figure 4.8) of clusters with CLW = 3 yields \sim 18 ADC on the p side and \sim 12 ADC on the n side. The second peak in figure 4.8 is caused by the strips

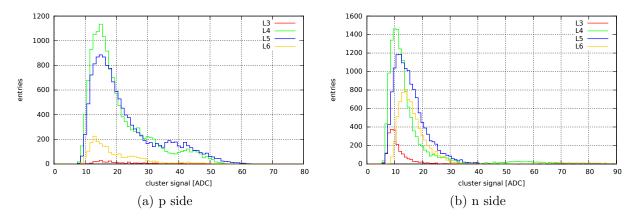


Figure 4.8: Signal distribution of the induced noise. Only clusters containing 3 strips are taken into account.

located at the edges of the sensor.

The remaining accumulations of clusters containing 3 strips are usually caused by defect strips or a common mode border adjacent to the maximum of the induced signal, see figure 4.6 and 4.7, strip number 540 on the p side of L4 and L5 sensors. Overall about 1% to 2% of the sampled events contain the induced noise. The number of falsely identified clusters introduced by this effect is significantly reduced by applying a minimum hit length of requirement of 3 consecutive sampled and a CMC with 32 strips.

4.2.3 Externally induced noise

After the installation of the PXD sensor we have encountered several noise problems, that caused the base line of each frame and the strip data to oscillate. Most of the impact was suppressed by applying a better grounding scheme except for the L3 sensor with its n side facing the pixel detector. Applying the same configurations as listed in tab. 4.2 to determine the systematic noise allows to identify the regions on the DSSD, which were affected by the externally induced noise during the measurements at DESY (see figure 4.9). The effects of the externally induced noise can be identified as peaks at each CMC section size (at each 128 strips). The n side of the L3 sensor shows the greatest impact, where the number of the noisy events accounts up to 10% out of 10000 events. Its most probable noise signal of the clusters with a CLW = 3 is about \sim 18 ADC, comparable to the systematic noise sampled with L4, L5 and L6 at the lab of HEPHY, see figures 4.10 and 4.8 respectively. By setting the section size to 32 strips, the most probable 3 strip cluster signal is reduced to ~ 4 ADC. The remaining sensors yield a slightly more frequent noise and an increase of most probable signals of ~ 1 to ~ 2 ADC. However the externally induced signals on the L3 sensor does not show any time correlation with the systematic noise on the L4 to L6 sensors.

Furthermore the higher amplitude and the more frequent occurrence of the externally induced noise widened the strip signal distributions on the L3 n side at the edges of each common mode section, figure 4.11. The remaining sensors show a slightly enhanced strip noise compared to the data taken at HEPHY.

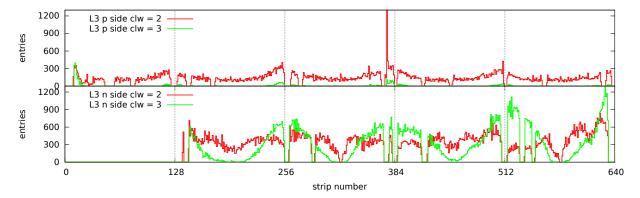


Figure 4.9: Areas affected by the external noise. The plot is generated with the same configurations and color scheme as figure 4.6. The SNR thresholds are generated with the data taken at the lab of HEPHY using a common mode section of 32 strips. The pedestal values were sampled with the first 5000 events of the same run.

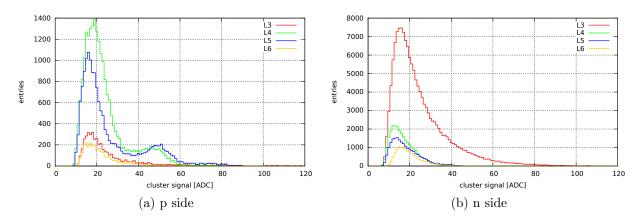


Figure 4.10: Signal distribution of the induced noise. Only clusters containing 3 strips are taken into account yielding a most probable signal of \sim 9 ADC per strip on the p side and \sim 4 ADC on n side.

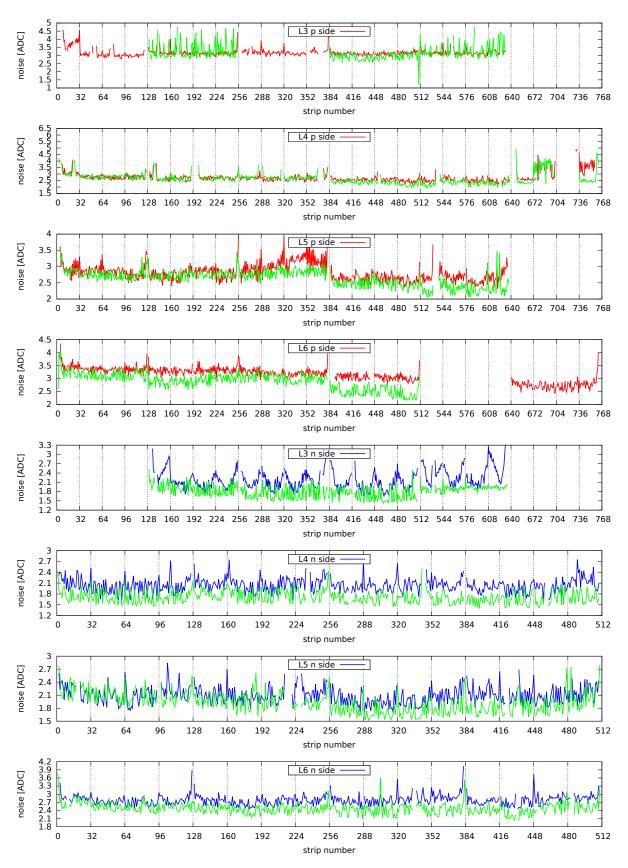


Figure 4.11: Strip noise of the sensors used at the beam test. The data are taken at DESY at 15° C. The red and blue lines represent the noise of the p and n side of each sensor respectively. The vertical gray lines mark the applied common mode sections of 32 strips. The green line represents the noise values taken at HEPHY at room temperature. 43

4.3 Results

The default configurations, applied to evaluate the data, are shown in table 4.3. Due to a

pedestal and noise			
number of events used to evaluate the pedestal	1000 events		
number of events used to sample the signal distribution	4000 - 9000 events		
common mode section	32 strips		
noisy strip cut	$1.5 \times \text{mean noise}$		
clustering			
seed threshold	5 SNR		
neighbour threshold	3 SNR		
cluster threshold	5 SNR		
hit length	3		

Table 4.3: Configurations

miscommunication with the firmware developer, the FADC board was only able to perform a common mode correction (CMC) with 128 strips, while the uploaded SNR thresholds for the clustering algorithm were obtained with a software CMC using 32 strips.

Typical beam profiles are depicted in figure 4.12. The higher rate of noisy events on the L3 n side mostly affects clusters comprising of more than 2 strips, while clusters with CLW = 1 and 2 are less contaminated. The remaining sensors hardly show any impact. The elevated 1 strip cluster counts at L4 p-side of last APV25 are caused by a negative signal correlation between each neighbouring strip, discussed in the previous section 4.2.1.

Overall only a fraction of the recorded data is affected by the noise. By applying the default configurations most of the noise signals are suppressed within the results of clusters containing 1 or 2 strips. The impact of the induced noise on hits with CLW > 2 is higher, because their most probable SNR is about 2 to 3 and thus in the same range as the applied neighbour cut. The following subsections present the results using the default configurations yielded from the data taken at DESY.

4.3.1 Signal distributions

Since the induced noise does not show any correlation with the trigger signal, only a fraction of the recorded data has been contaminated. For uncontaminated events the common mode correction with 128 strips applied by the FADC boards yield about the same value compared to the results with a section size with 32 strips. Figure 4.13 shows the resulting signal distributions. Due to defect strips, which were not automatically detected by TuxOA, there is a smaller peak at about 15 to 25 ADC. The greater cluster signal on the L3 sensor is caused by a greater strip gain. For hits (events) with CLW = 2 a non-negligible fraction of the signal is capacitively read out from the intermediate strip. The interplay of different inter strip distances, the SNR thresholds and the signal loss due to capacitive readout causes the difference between the most probable signal of clusters with CLW = 1 and CLW = 2, respectively. The most probable signal of cluster with a CLW > 2 yields twice the amount of the ones with CLW = 1 and CLW = 2, indicating 2

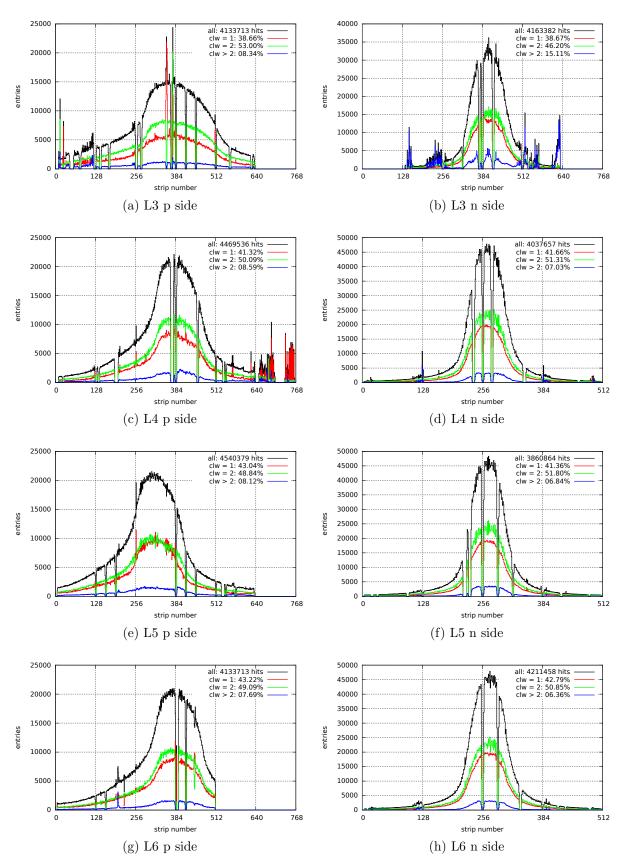


Figure 4.12: Hit map at 15°C in both vertical (p-side) and horizontal (n-side) directions. The black line shows the cumulative sum of all hits, the red line the hits with CLW = 1, the green line the hits with CLW=2 and the blue line the hits with CLW>2. 45

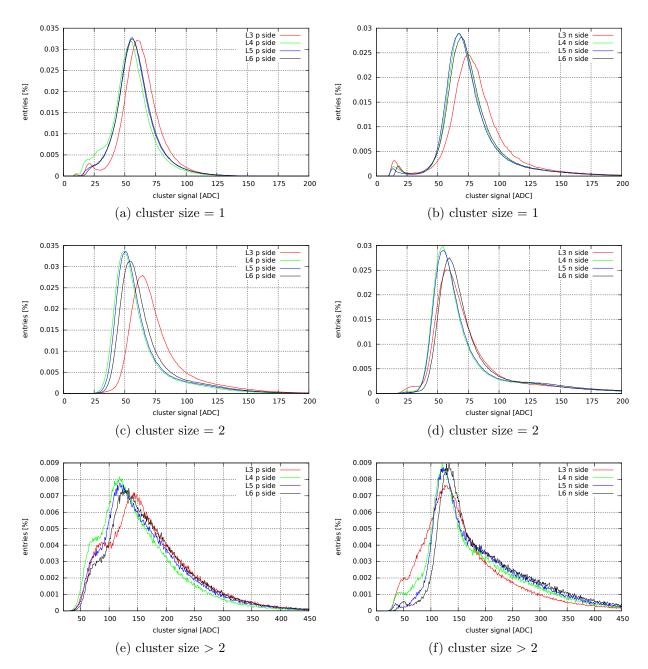


Figure 4.13: Cluster signal distribution on the p side (a, c, e) and the n side (b, d, f) at 15°C. The vertical axis shows the entries of each bin normalised to the total number of hits. The corresponding beam profile is shown in figure 4.12 and the noise values in 4.11.

adjacent particle hits, that were merged during the clustering procedure. With only a few kHZ/cm² 2 adjacent hits are quite unlikely. However the beam passed through a massive solenoid magnet, that might have caused a small fraction of beam particles to shower, increasing the chance for adjacent hits. Additionally smaller peaks at the expected cluster signal can be observed (figures 4.13e and 4.13f).

Overall most of the induced signals are suppressed by applying the default clustering configurations, see table 4.3. By splitting the evaluation into different cluster sizes it becomes obvious, that the noise events are all included in the events with a cluster width of three or more strips. For L4, 5 and 6 only about 7% to 8% and for L3 about 15% of all events are affected by the fake hits from induced noise. Additionally the oscillating noise values of the L3 n side, figure 4.11 blue line, might affect the clustering efficiency at the contaminated regions. Due to a more frequently induced signal, a small fraction of shaper pulses sampled with 6 frames is distorted, thus deteriorating a precise hit time finding.

4.3.2 Temperature dependence of strip noise and gain of each strip

The various temperature scans were performed at -10, 0 and 15°C, while at 15°C a different set of APV25 chip settings were applied. The different chip setting influence the amplification of the strip signals. Figure 4.14 shows the mean noise values of each hybrid at the mentioned temperature. Overall the mean strip noise shows no significant im-

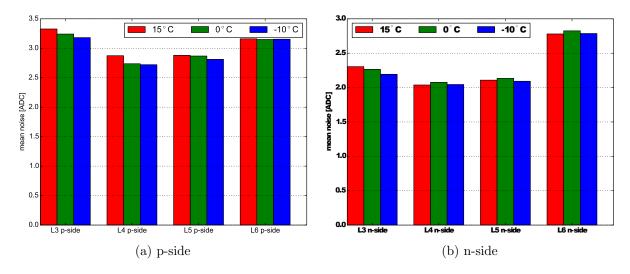


Figure 4.14: Mean noise of each hybrid at different temperatures.

provement over a range of 25°C. In order to determine the gain of each strip, calibration runs were performed at the same temperature, where a defined charge is injected into the preamplifier of the APV25. Figure 4.15 shows the resulting mean calibration signal of each hybrid. The different ADC counts between 15 and 0°C indicate the impact of the different chip settings (different gains), while the 0 and -10°C with the same chip configuration only yield a small improvement. In order to eliminate the influence of the strip gains, SNR of the calibration pulses (figure 4.16) was evaluated. The mean SNR

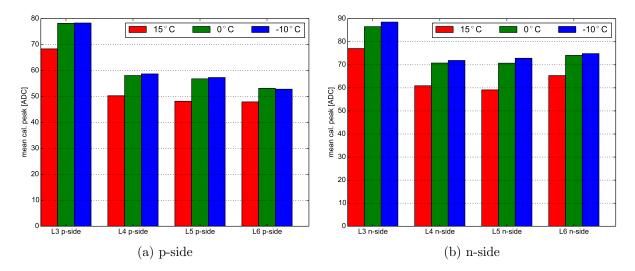


Figure 4.15: Mean peak value of the calibration pulses at different temperature.

values yield an improvement of about 15% over a temperature range of 25°C. The smaller difference at 0 and -10°C of each sensor indicates, that the SNR values starts to saturate.

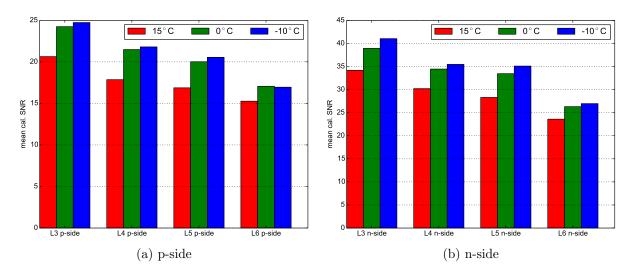


Figure 4.16: Mean SNR of the calibration pulses at different temperature.

4.3.3 Temperature dependency of SNR

Figures 4.18 and 4.19 show the SNR of both p side and n side of each sensor. At 15°C a run with about 1.5 million event are used for the evaluation, while at 0 and -10°C four smaller runs containing about 10000 events are used to calculate the SNR values. The smaller peaks at a SNR of \sim 7 are caused by defect strips that have not been automatically detected by TuxOA. The different most probable SNR values between each sensor are caused by different geometries. Due to the evaluation of SNR = $\frac{\sum_i S_i}{\sqrt{\sum_i N_i^2}}$, the resulting

values for 1 strip clusters are about $\sqrt{2}$ times greater than the SNR of 2 strip clusters. The most probable SNR values after appling a fit with a Landau Gauss convolution are shown in figure 4.17. The comparison between sampled values at -10° and 15° Celsius

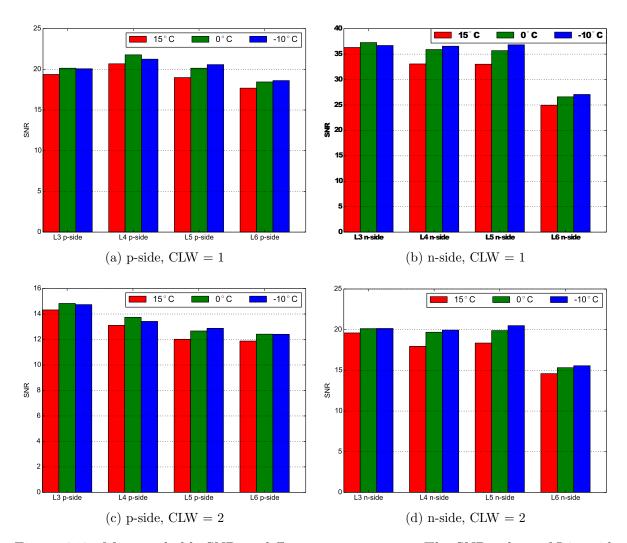


Figure 4.17: Most probable SNR at different temperatures. The SNR values of L3 n-side are evaluated with the externally induced noise. For 0 and -10°C the mean SNR values of four independent runs are plotted.

indicates a better SNR at lower temperature. Depending on the sensor the improvement compared to 15°C is between 8% and 10%. However the small difference between 0° and -10° Celsius suggests that the temperature dependent SNR values start to saturate. A similar behaviour is also observed with the SNR of calibration pulses (figure 4.16). The impact of the externally induced noise on the L3 n side might have widened the SNR distribution, while a significant contribution originates from the applied strip noise, see figure 4.11.

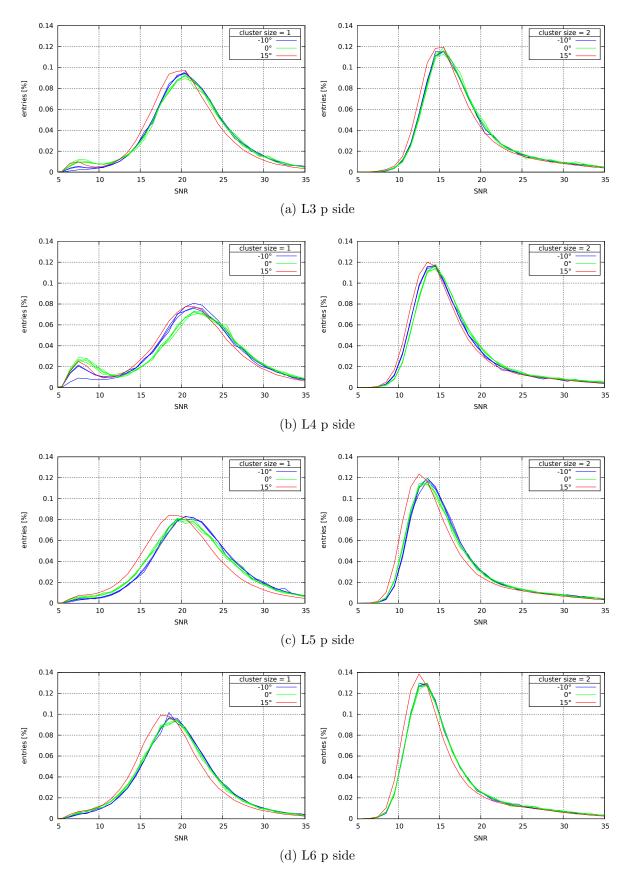


Figure 4.18: SNR distributions at different temperatures. The plots show the distributions sampled with the p-side of each sensor. Several run has been evaluated at 0 and -10°C.

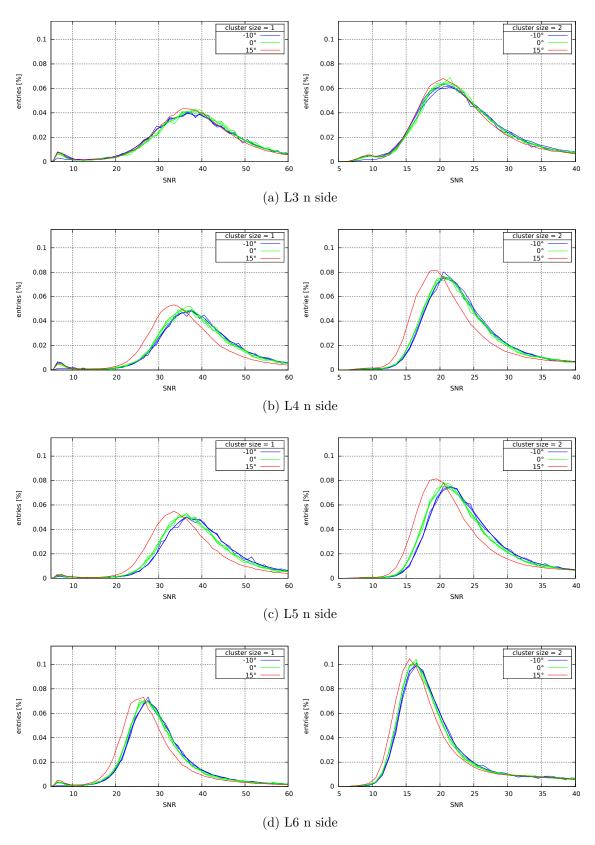


Figure 4.19: SNR distributions at different temperatures. The plots show the distributions sampled with the n-side of each sensor. Several run has been evaluated at 0 and -10°C.

Chapter 5

Conclusion and outlook

One of the major tasks of this thesis was to finish the development of TuxDAQ and to update the communication with the latest FADC system as well as to design TuxOA. First versions of both applications were successfully tested at the DESY beam test.

The DESY beam test was the first integration test of the Belle II VXD aiming to examine the communications between of the PXD, SVD and the Belle II DAQ. The integration test also provided insights into the interactions between SVD and its environment. A better grounding scheme was applied during the beam test, that suppressed most of the externally induced noise. However a noticeable disturbance was still visible in the strip noise on the n-side of the L3 DSSD, while the remaining sensors showed comparable noise levels to the ones measured at HEPHY. The induced noise indicates possible crosstalk between PXD and SVD. The following standalone beam test at CERN in November 2014 showed similar noise levels of the L3 sensor with the lab results (figure 5.1).

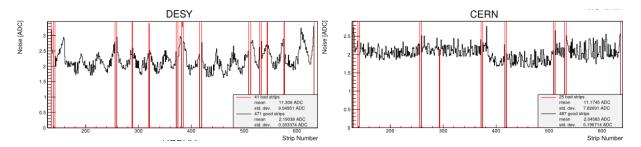


Figure 5.1: Noise map of the L3 sensor n-side taken at DESY and CERN.

Four DSSD modules, similarly arranged as in the future Belle II experiment, were tested in a beam at DESY. The sensors have been tested at -10°, 0° and 15°C. While the mean strip noise of each sensor did not indicate any significant change, the particle signals increased at lower temperature. Comparing -10° to 15°C the SNR increases by about 8% to 10%, while the comparison between -10° and 0° suggests, that the SNR values starts to saturate. The obtained SNR values are in good agreement with the previous measurements [16].

In order to determine the source of the noise problems and the sensitive frequency range of the SVD readout system, several test was performed with a fully functional layer 5 ladder at ITA (Zaragoza, Spain). During the measurements a defined amount of noise at different frequencies were injected into cables carries the supply voltage and transmitting data. In order to prevent crosstalks with the PXD system, an emission test on the pixel detectors has been planned.

TuxDAQ and TuxOA are currently modified for the integration into the SVD slow control system, that monitors several environmental sensors (temperature, humidity, radiation, etc.), the power supply, the state of the hardware components and a low level data quality. The slow control system is implemented with the so called Experimental Physics and Industrial Control System (EPICS) framework. A dedicated gateway interprets the incoming requests from the global Belle II DAQ. The first iteration of the slow control system will be tested at the next combined DESY beam test in April 2016.

Appendices

Appendix A

TuxDAQ

A.1 Overview of the changes

The following classes/structures were changed to adapt to the latest hardware:

Hardware structure - software mapping

The relations between each hardware component was changed to deprecate unnecessary classes and to simplify the relations between classes. Figure A.1 shows the changed relations between each object. The following objects became deprecated due to the latest hardware design: SCChannel (slow control channel), REBO (repeater board), Mambo (mother board).

The SCChannel, that monitors the temperature, voltage and currents of the DC/DC converter, had to be reimplemented. Considering vast differences of the data acquisition rate (in a magnitude of at about 10² to 10³) compared to the SPY FIFO readout, the monitoring can be performed in a separate thread with an update rate of one second matching the hardware constrains.

Due to the different communication pattern of the latest FADCs compared to the SVD3 system, the functionalities of the DAQChannels were deprecated. Currently the DAQChannels is used for data storage. Additionally it houses the configurations saved in the APV25 and I2CConfig object. The DetectorModule is used to map the DAQChannels to the connected sensor. Overall the DAQChannel, APV25 and I2C objects can be merged into a single configuration object, however is would entail a redesign of the whole application, that was not possible due to time constrains.

Controller and FADC

The FadcVME class was recoded with the latest VME addresses and its access pattern. Overall, the function calls are roughly the same compared to the old design. The new FADC Controller board introduced an additional FSM, the so called 'SPY state', to synchronise the SPY FIFO readout. The implemented FSM consists of the following states:

• IDLE: Initial state of the controller.

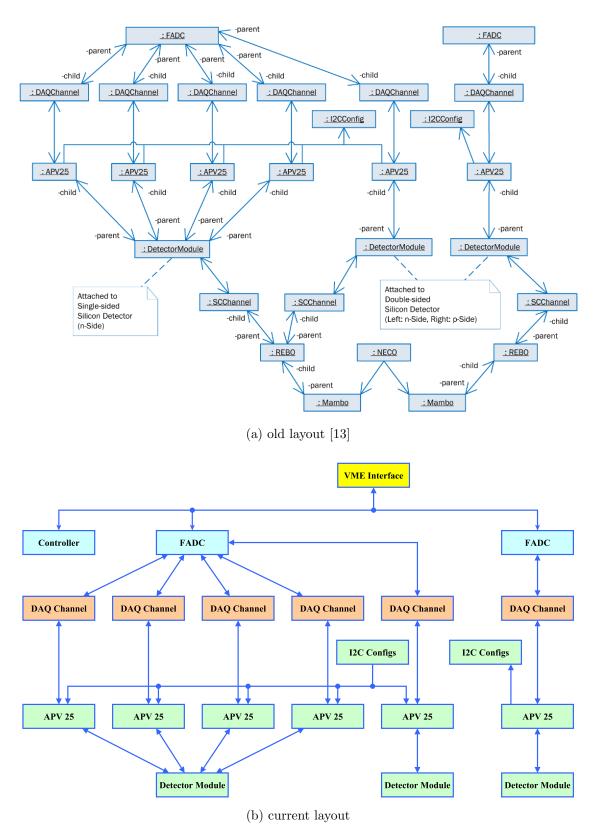


Figure A.1: Relations between each software object mapping the hardware components. Both examples show the same configuration comprising of a single sided detector and a double sided detector. The Neco (new controller) object in fig (a) represents the Controller object in (b). The boxes represents classes and the arrows pointers.

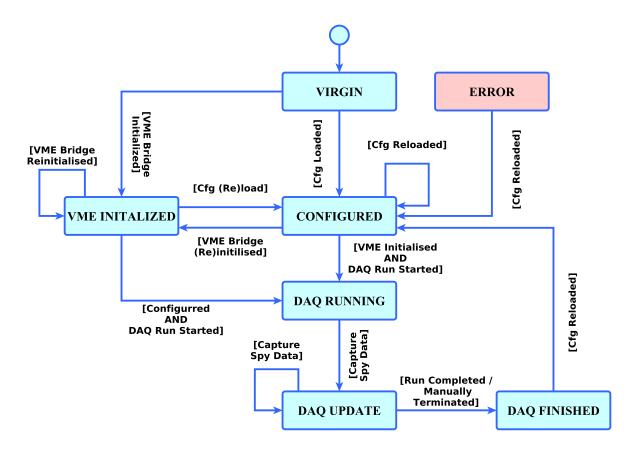


Figure A.2: TuxDAQ FSM.

- WAITING TRG: The transition of 'waiting for trigger' state is only accessible with the IDLE state and triggered by sending a 'SPY NOW' signal issued by Tux-DAQ.
- TRG DETECTED: 'TRG DETECTED' indicates that the controller has forwarded the trigger signal to each APV25 chip. After reading the SPY FIFO Tux-DAQ has to send a 'CLEAR SPY STATE' signal to reset the FSM to IDLE.

DAQControl

The DAQControl class is the central control system delegating the functionalities of the hardware and is designed as a finite state machine (FSM), figure A.2. Only the states 'Configured' and 'DAQ Update' were changed to adapt to the latest hardware. Due to legacy design the event loop of 'DAQ Update' is driven by a timer, that executes the data acquisition corresponding to the run type, figure A.3. The additional tasks performed by the different configuration runs are listed in the table A.1. The control flow of each run type has been refactored into the corresponding functions.

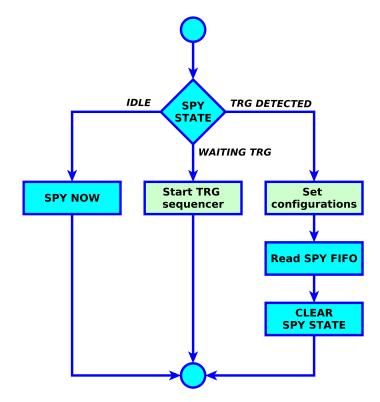


Figure A.3: Tasks performed at each step of the event loop. The blue boxes shows the steps taken during a hardware run. The green boxes are additional tasks performed during a configuration run.

run type	TRG sequencer	configurations		
software run	software trigger			
calibration run	calibration request	APV25 latency		
ADC delay scan	soft reset + software trigger	Delay25 latency		
FIR filter run	soft reset + software trigger			
sixlet calibration run	calibration request	APV25 latency		

Table A.1: Enabled TRG sequencer and settings performed at each step of the configuration runs corresponding to the green boxes in figure A.3. The configurations are incremented depending on an internal event counter.

Appendix B

TuxOA

B.1 ROOT file

For each side of the sensor a separate ROOT file is created, that logs the results yielded for each event. The data structure of each entry is listed in table B.1. TuxRoot was

branch name	data type	description
EventNumber	$UShort_t$	event number
NumberOfHits	$UShort_t$	number of clusters
Occupancy	Double_t	number of strips detecting the particle signal
SubEventHit	$UChar_t[NumberOfHits]$	frame containing the maximum signal
FirstStrip	UShort_t[NumberOfHits]	first strip of the cluster
SeedStrip	$UShort_t[NumberOfHits]$	seed strip
ClusterWidth	$UShort_t[NumberOfHits]$	number of strip of the current cluster
ClusterSignal	$Double_t[NumberOfHits]$	sum of the cluster strip signals at SubEventHit
ClusterNoise	$Double_t[NumberOfHits]$	sum of the corresponding strip noise
SignalToNoise	$Double_t[NumberOfHits]$	signal to noise ratio
Eta	$Double_t[NumberOfHits]$	decimal placed of COG used for the η correction.

Table B.1: Data structure of an event recorded in the ROOT file. The data type is defined in rtypes.h.

created to generate few summary plots of the recorded data, see figure B.1.

Desy 2014 - L4 n-side 009 - Cluster Results

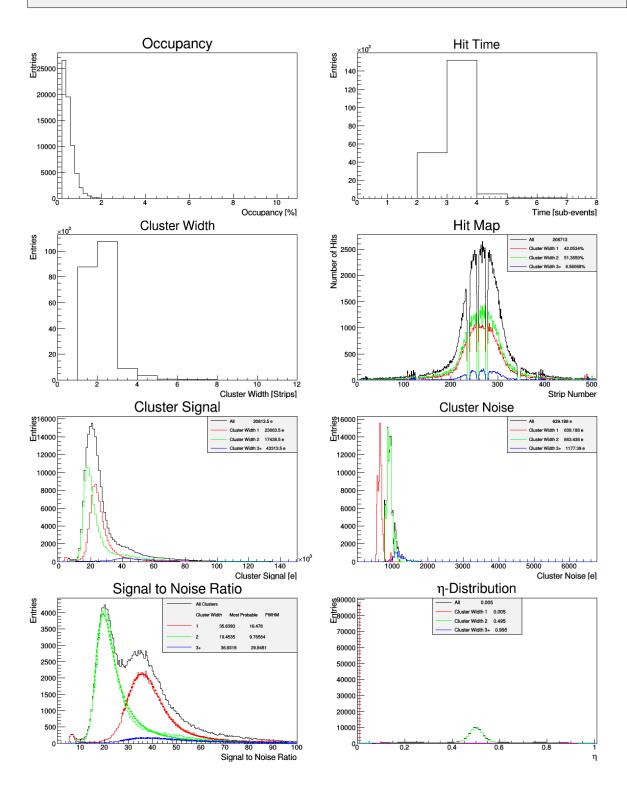


Figure B.1: Example of the plots generated by TuxRoot. The η distribution is distorted, since the data was taken with zero suppression.

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