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D I S S E R T A T I O N

Advanced PNP PIN Phototransistors in Submicrometer CMOS

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„Das schönste Glück des denkenden Menschen ist,
das Erforschliche erforscht zu haben und
das Unerforschliche zu verehren.“

Johann Wolfgang von Goethe

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I wish to thank my parents and my brother, Dimitrinka, Petko and Daniel Kostov for their support and patience.

Last but not least, I would like to express my gratitude to my girlfriend Anda for her support.

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Plamen Kostov

Abstract

Introduction: The aim of this work was to develop and investigate new kinds of phototransistors. These phototransistors should have the possibility to be integrated in a standard CMOS process. A further requirement was the improvement of their responsivity and bandwidth, especially for deep penetrating light, i.e. the light in the near infrared range.

Methodology: The phototransistors have been fabricated in three different sub-micrometer CMOS processes: $0.18\,\mu m$, $0.35\,\mu m$, and $0.6\,\mu m$. In each process a p-substrate silicon wafer together with a thick low doped p-epitaxial layer on top of it was used for the implementation of the phototransistors. The limitation to this kind of wafers together with the CMOS process without standard burried collector (SBC) technology restricts reasonable phototransistor types to PNP PIN phototransistors. The key point for achieving these requirements is to reduce the base-collector and base-emitter capacitances and to reduce the base transit time of the charge carriers. A reduction of the base-collector capacitance is achieved by implementing a thick low doped p epitaxial layer in the collector. Furthermore, this leads to an increase of the drift current part and to a reduction of the diffusion current part of the photogenerated charges for deeper penetrating light resulting in a reduced transit time and in an increased bandwidth. At the base-emitter junction a reduction of the capacitance is achieved by reducing the emitter size. However, reducing the emitter size will also lead to a reduction of the responsivity of the device due to an increased recombination probability of the charges in the base. The recombination probability can be reduced by means of a lower doping concentration in the base. Reducing the doping concentration of the

base leads to an expansion of both space charge regions closer to each other in the base region and thus to a thinner effective base and to a reduced base transit time. By this means on one side the recombination probability of the charges in the base is reduced and on the other side the bandwidth of the phototransistor is increased. The reduction of the base doping concentration in a standard CMOS process is achieved by interrupted n-wells which diffuse into each other during the high-temperature processing steps. A variation of the gaps between the n-wells leads to a variation of the resulting base doping concentration and thus to a variation of the gain and the bandwidth of the phototransistor.

Results: Several phototransistors were implemented in different sizes and different layouts of the base and the emitter areas in the three mentioned processes. Depending on their layout and the process these devices achieve maximum responsivity-bandwidth products of 238.4 A/W·MHz, 251.8 A/W·MHz and 177.8 A/W·MHz for the wavelengths of 410 nm, 675 nm, and 850 nm, respectively. Additional measurements including further DC and AC responsivities, bandwidths, rise and fall times, dark currents, current gains, output characteristics, spectral responsivities and noise analysis were performed. Furthermore, the expansion of the space-charge regions and the electric fields in them were simulated for several devices at different collector-emitter voltages.

Conclusion: PNP PIN phototransistors with different layouts were built and investigated in standard CMOS processes. The possibility to change their design of the base and emitter opens the opportunity to adapt the key parameters of the phototransistors (e.g. their responsivity and bandwidth) to respective requirements. Furthermore, the monolithic and cheap integration of the phototransistors in silicon offers a possibility for light detection, especially if higher responsivities are required. These phototransistors are well suited for applications like opto-couplers, light barriers, closed photonic sensors (e.g. shear sensors), etc.

Kurzfassung

Einleitung: Das Ziel dieser Arbeit war die Entwicklung und Untersuchung neuer Phototransistoren. Eine zusätzliche Anforderung war die Verbesserung der Empfindlichkeit und der Bandbreite vor allem für tief eindringendes Licht (z.B. infrarotes Licht in Silizium).

Methodik: Die Phototransistoren wurden in drei unterschiedlichen CMOS Prozessen hergestellt: $0.18\,\mu m$, $0.35\,\mu m$ und $0.6\,\mu m$. Als Ausgangsmaterial wurde in jedem Prozess ein p-Substrat Siliziumwafer mit einer dicken, niedrig dotierten, epitaxisch aufgewachsenen p-Schicht verwendet. Die Beschränkung auf den p-Substrat Wafer sowie das Fehlen von vergrabenen Kollektoren führte zur Beschränkung der Entwicklung und Untersuchung auf PNP PIN Phototransistoren. Die Kernpunkte zum Erzielen dieser Anforderungen sind einerseits die Reduktion der Basis-Kollektor- sowie der Basis-Emitter-Kapazität und andererseits die Reduktion der Transitzeit der Ladungsträger durch die Basis. Die Reduktion der Basis-Kollektor Kapazität wird durch die niedrig dotierte p-Epitaxieschicht erfüllt. Dies führt außerdem zu einer dicken Basis-Kollektor Raumladungszone und damit zu einer Erhöhung des Driftanteils und Verringerung des Diffusionsanteils vom photogenerierten Strom für tief eindringendes Licht und dadurch zur Verkürzung der Transitzeit photogenerierter Ladungsträger. Eine Verringerung der Basis-Emitter Sperrschicht Kapazität wird durch eine Verkleinerung der Emitterfläche bewerkstelligt. Diese Verkleinerung führt jedoch auch zur Verringerung der Fotoempfindlichkeit des Phototransistors da sich die Wahrscheinlich für Rekombination der Ladungsträger in der Basis erhöht. Um dem entgegen zu wirken kann die Dotierung der Basis verringert werden. Eine Verringerung der

Basisdotierung führt zu einer Ausweitung beider Raumladungszonen in die Basis hinein. Daraus folgt einerseits die Reduktion der Rekombinationswahrscheinlichkeit der Ladungsträger in der Basis und andererseits die Verkürzung der Basistransitzeit. Eine Möglichkeit eine Verringerung der Basisdotierung in einem herkömmlichen CMOS Prozess zu realisieren ist die Verwendung von n-Wannen Streifen, welche während der Herstellung wegen den Hochtemperaturschritten ineinander verfließen. Die Variierung des Abstands zwischen den einzelnen n-Wannen Streifen führt zu einer unterschiedlichen resultierenden Basisdotierung und damit auch zu unterschiedlichen Eigenschaften des Phototransistors.

Ergebnisse: Verschiedene Phototransistoren mit unterschiedlichen Größen und unterschiedlichen Layouts der Basis und des Emitters wurden in den oben genannten Prozessen hergestellt. Abhängig von dem Layout der Basis und des Emitters, erzielen die Phototransistoren maximale Empfindlichkeitsbandbreitenprodukte von bis zu $238.4\,\text{A/W}\cdot\text{MHz}$, $251.8\,\text{A/W}\cdot\text{MHz}$ und $177.8\,\text{A/W}\cdot\text{MHz}$ für die Wellenlängen $410\,\text{nm}$, $675\,\text{nm}$ und $850\,\text{nm}$. In weiteren Messungen wurden zusätzliche DC und AC Empfindlichkeiten, Bandbreiten, Anstiegs- und Abfallzeiten, Dunkelströme, Stromverstärkungen, Ausgangskennlinienfelder, spektrale Empfindlichkeiten sowie Rauschen erfasst. Mittels Simulationen wurden die Ausweitungen der Raumladungszonen sowie das vorhandene elektrische Feld in ihnen für verschiedene Kollektor-Emitter Spannungen simuliert.

Schlussfolgerung: PNP PIN Phototransistoren mit unterschiedlichen Layouts wurden in herkömmlichen CMOS Prozessen hergestellt und untersucht. Die Möglichkeit das Layout der Basis und des Emitters zu variieren, öffnet Wege zur optimalen Anpassung der Phototransistoren für entsprechende Anforderungen. Außerdem bietet die monolithische und billige Herstellung der Phototransistoren in Silizium neben den integrierten Photodioden eine weitere Möglichkeit zur Lichtdetektion, besonders wenn höhere Empfindlichkeiten gefragt sind. Durch diese Eigenschaften eigenen sich die präsentierten Phototransistoren besonders gut für Anwendungen in Optokopplern, Lichtschranken, geschlossenen optischen Systemen (z.B. Scherkraftsensoren), usw.

Contents

Introduction

1 Motivation

In recent decades photonics became an important and indispensable part of nowadays technology. In a variety of today's applications photonics can be found, e.g. in data-communications, image sensors, chemical sensors, switches, waveguides, etc. For almost all of these applications the photonic system is based on two parts. On one side a light source is needed for the generation and emission of photons. Such photon emitting devices are typically light bulbs, LEDs (Light Emitting Diodes), LASERs (Light Amplification by Stimulated Emission of Radiation), etc. However, there are also natural light sources, e.g. background radiation from the sun. On the other side a sensor for the detection of the incident photons is needed. Some of the most commonly used detectors are photodiodes, avalanche photodiodes or phototransistors.

Nowadays, most photon emitting devices and photo sensors are realized in semiconductors. One main advantage of semiconductors is the relatively small area needed for the integration and thus the high compactness of the device. LEDs as well as the semiconductor based LASERs are typically implemented in direct semiconductors due to the energy properties of the band structures of the used crystal. The emission of a photon in a direct semiconductor does not require an additional momentum of a phonon, as it would be the case with an indirect semiconductor. Photodetectors however can be implemented in direct and indirect semiconductors. Silicon offers a cheap, clean, and an easy possibility for integration of photodetectors. Furthermore a high amount of the following readout

circuitry can be integrated in silicon, which leads to the possibility of a monolithic integration of the photodetector together with the readout circuitry. Such combinations are called opto-electronic integrated circuits (OEICs). OEICs offer many advantages over detectors wirebonded to integrated circuits: reduced chip area due to a monolithic integration, reduced parasitics (inductivity and capacity) due to eliminated bond wires and bond pads, cheaper fabrication, etc.

In silicon based CMOS processes photodiodes and phototransistors are the most commonly implemented photodetectors. Even though photodiodes can offer high bandwidths, they do not have an inherent current amplification like phototransistors. Phototransistors can have a high current amplification, however at a reduced bandwidth, which nevertheless may be sufficiently high for numerous applications. Common CMOS integrated phototransistors as those presented in [1–21] typically achieve bandwidths in the kHz range. Some publications even do not present bandwidths. However, the quantity of applications could be increased when it would be possible to increase the bandwidth of the phototransistor at same or higher responsivities.

The aim of this work was to develop and investigate new kinds of CMOS integrated phototransistors with the goal to increase the devices' bandwidth.

2 Outline of the Thesis

This PhD thesis deals with the development, investigation and characterization of CMOS integrated PNP phototransistors. The phototransistors were built in three different CMOS technologies: $0.18\,\mu m$, $0.35\,\mu m$, and $0.6\,\mu m$. Their structures and characteristics were presented in 14 peer-reviewed publications (ten conference papers and four journal papers).

This thesis is structured as a cumulative work. It consists of an introduction chapter, eight publications (each as a separate chapter) and a concluding chapter. In the **Introduction** a detailed description of the physical and optical properties of semiconductors is given. The following eight publications are enumerated with

capital letters: **Publications A**, **B**, **C**, **D**, and **E** present phototransistors built in the 0.18 µm CMOS process. **Publication F** reports on one phototransistor implemented in the 0.35 µm CMOS process. The characterization and design of phototransistors built in the 0.6 µm CMOS process are presented in **Publications G** and **H**. In the **Comparison and Conlusion** the implemented phototransistors are compared to each other and the best results are presented. Furthermore a comparison with other phototransistors from the literature is given.

3 Theory and Basics

Nowadays most photodetectors are typically built from semiconductors. Different semiconductor materials can be used for the detection of photons.

3.1 Semiconductor Materials

Semiconductor materials are characterized with a bandgap energy (E_g) of less than 6 eV between the valence band and the conduction band. They can be either element crystals or compound semiconductors. Element semiconductors are typically from the IV$^{\text{th}}$ group of the periodic system. The most used semiconductors from group IV are silicon (Si) and germanium (Ge). Compound semiconductors are combinations of minimum two materials from two groups of the periodic system. Typical group combinations used for compound semiconductors are IV-IV (e.g. SiGe), III-V (e.g. GaAs, InP, GaAlAs) and II-VI (e.g. ZnSe, ZnS). Each semiconductor has its own specific characteristic. The most important characteristic for light detection is the bandgap energy E_g of the semiconductor and whether it is a direct or an indirect semiconductor.

3.2 Theory on the Optical Absorption and Carrier Generation

The main principle of the photodetection is based on the inner photoeffect which describes the photon absorption and the generation of carriers within a semiconductor. Each photon can be characterized by its wavelength λ_{ph} or energy E_{ph},

respectively. The photon energy is indirectly proportional to the wavelength of the photon [22]:

$$E_{ph} = \frac{hc}{\lambda_{ph}} = h\nu, \tag{1}$$

where h is the Plank constant and c is the speed of light in vacuum.

The photon energy is transferred to an electron when they interact with each other. Depending on the photon energy three absorption processes can occur (Fig. 1) [23]. First, for intrinsic absorption the photon energy is larger than the bandgap energy of the semiconductor. In this case an electron-hole pair is generated and the electron is lifted from the valence band into the conduction band. Second, in the extrinsic absorption an electron is lifted from the valence band to a trap or from a trap to the conduction band, respectively. In the third case the photon energy is absorbed by a free electron in the conduction band, which is lifted within the conduction band to a higher energy level. However, only the first process can be used for the current transportation and the detection of the photon irradiation. This leads to a maximum detectable wavelength, the so called fundamental wavelength λ_{E_g}. Photons with wavelengths higher than λ_{E_g} do not have enough energy to lifted an electron from the valance band to the conduction band. For silicon, which has a bandgap energy of $1.1\,\text{eV}$, the cut-off wavelength equals $1125\,\text{nm}$. The probability for the interaction of photons with silicon increases for higher photon energies and is thus depending on the differential energy ΔE between energy of
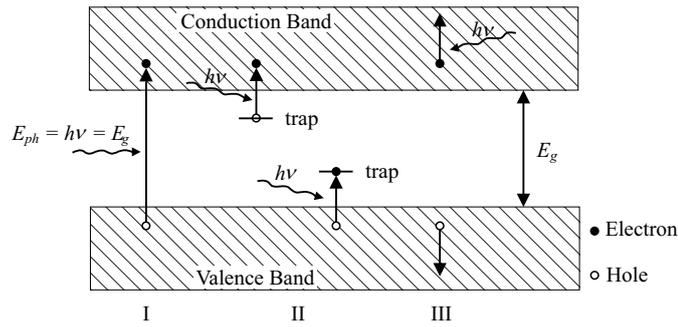
Figure 1: *Absorption processes in a semiconductor. (I. Intrinsic absorption, II. Extrinsic absorption, III. Absorption by free carriers) [23]*

the photon and the energy of semiconductor's bandgap:

$$\Delta E = E_{ph} - E_g. \tag{2}$$

The interacting probability between photons and the semiconductor is defined by the absorption coefficient α. Thus the absorption coefficient α is depending on the wavelength of the photons and the interacting material. Fig. 2 depicts the absorption coefficient over the wavelength for different semiconductors. The decrease of the optical light power within the semiconductor and thus the decrease of the density of photons within the semiconductor can be described by Beer-Lambert's law [22]:

$$P_{opt}(z) = P_{opt}(0)\mathrm{e}^{-\alpha z}, \tag{3}$$

where P_{opt} is the total incident light power and $P_{opt}(z)$ the remaining light power in the depth z of the semiconductor. After (3) an $1/e$ penetration depth depending on the wavelength of the photons and on the semiconductor can be introduced. The pentration depth is indirectly proportional to the absorption coefficient α. Fig. 3 shows the photogeneration density dependence on the wavelength for silicon [22].
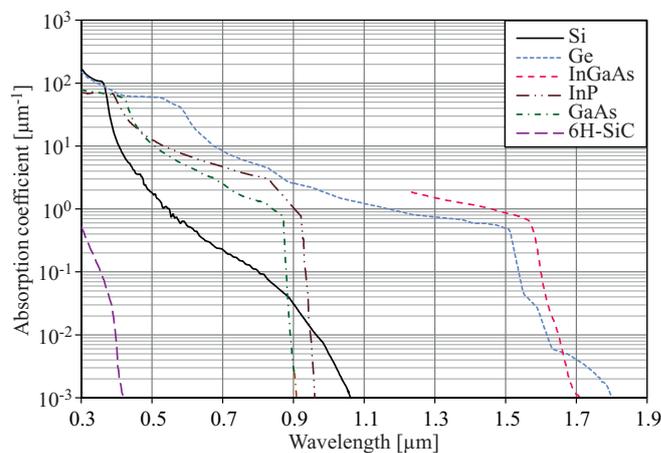
Figure 2: *Absorption coefficient α over wavelength for different semiconductors [24].*

3.3 Quantum Efficiency, Generation Rate and Responsivity

A portion of the incident photons are reflected at the surface of the semiconductor. These leads to the importance of the definition of an optical quantum efficiency η_o [22]:

$$\eta_o = \frac{\text{Amount of absorbed photons in the semiconductor}}{\text{Amount of incident photons}}. \tag{4}$$

However, only some of the photogenerated charges contribute to the photocurrent. The reduced quantum efficiency, known as the internal quantum efficiency η_i only takes into account the photocurrent loss due to carrier recombination:

$$\eta_i = \frac{\text{Amount of generated charges contributing to the photocurrent}}{\text{Amount of absorbed photons in the semiconductor}}. \tag{5}$$

Finally the external quantum efficiency η is defined by:

$$\eta = \frac{\text{Amount of generated charges contributing to the photocurrent}}{\text{Amount of incident photons}}$$

$$= \eta_o \eta_i = \frac{I_{PH}/q}{P_{opt}(0)/h\nu}. \tag{6}$$

In (6) I_{PH} is the photogenerated current and q is the elementary charge.
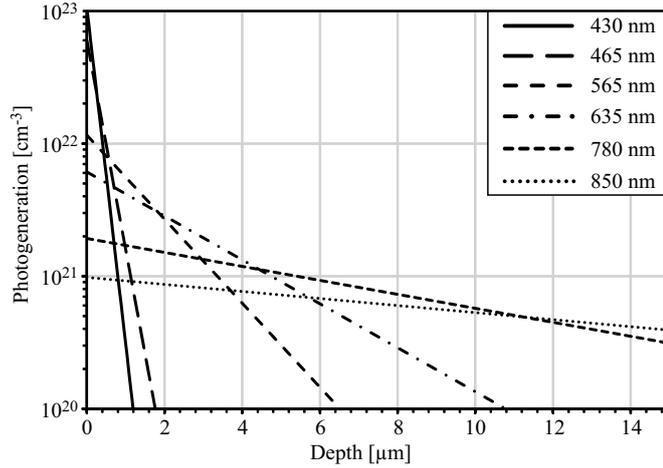
Figure 3: *Photogenerated carriers in silicon depending on the wavelength [22].*

With the external quantum efficiency η a generation rate G for the electron-hole pair generation in the semiconductor can be defined as

$$G = \eta P_{opt} \frac{\lambda}{hc} \tag{7}$$

leading to the photocurrent I_{PH} in a photodetector:

$$I_{PH} = qG = q\eta P_{opt} \frac{\lambda}{hc}, \tag{8}$$

Dividing (8) by P_{opt} leads to the maximum achievable responsivity R of a photodetector:

$$R = \frac{I_{PH}}{P_{opt}} = q\eta \frac{\lambda}{hc}. \tag{9}$$

Assuming that each photon will generate an electron-hole pair that contributes to the photocurrent then η would equal 1. In this case the responsivity R would increase proportionally with the wavelength λ. However, in practice the quantum efficiency η is limited by several factors as surface reflection or recombination of carriers in the field free region. The maximum responsivity is achieved for the wavelengths with the lowest reflectivity and an optimal penetration depth. The theoretical curve and the real curves of the responsivity over the wavelength of photodetectors in different semiconductors are presented in Fig. 4 [25].

3.4 Electrical Characteristics of Semiconductors

Within **Publication A**, **C**, and **D** simulations of the thickness of the space-charge regions and the electric field strength in the space-charge regions of several phototransistor are presented. For such simulations an amount of equations are needed. The most important and fundamental equations are described in the following.

3.4.1 Current Flow in Semiconductors

In semiconductors a charge carrier motion is present, which can be written as [26]:

$$\vec{i} = \varrho q \vec{v}, \tag{10}$$
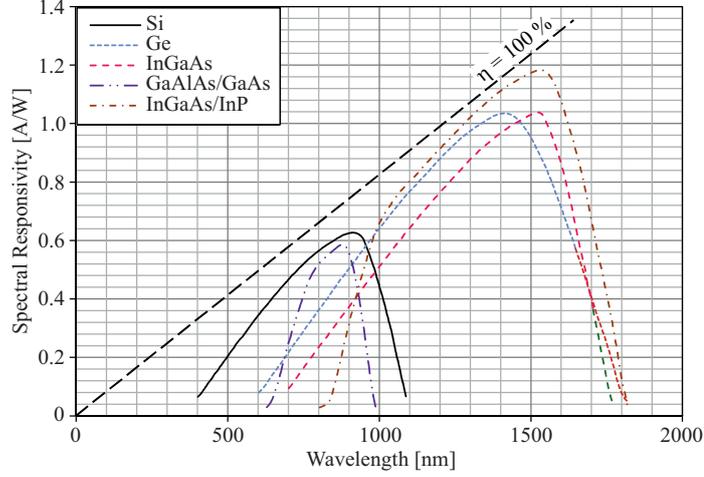
Figure 4: *Real photodetector responsivity R over wavelength for different semiconductors [25].*

where, $\vec{\boldsymbol{i}}$ is the total current density, ϱ is the density of charges, q is the elementary charge, and $\vec{\boldsymbol{v}}$ is the mean velocity. The bold symbols with the arrows represent vectors. If the motion is caused by an electric field then the resulting current is called a drift current $\vec{\boldsymbol{i}}_{Drift}$. If the motion is caused by a diffusion away of accumulated carriers than the resulting current is defined as a diffusion current $\vec{\boldsymbol{i}}_{Diff}$. Splitting (10) into an electron and hole based current leads to:

$$\vec{\boldsymbol{i}} = pq\vec{\boldsymbol{v}}_p - nq\vec{\boldsymbol{v}}_n, \tag{11}$$

where p and n are the densities of free holes and free electrons per volume, respectively. Consequently $\vec{\boldsymbol{v}}_p$ and $\vec{\boldsymbol{v}}_n$ are their mean velocities. The mean velocity is caused in the case of $\vec{\boldsymbol{i}}_{Drift}$ by an applied electric field and in the case of $\vec{\boldsymbol{i}}_{Diff}$ by the negative gradient of the accumulated charge carriers. In both cases the velocity is dependent on the mobility of the charge carriers [22, 26].

3.4.2   Mobility of Charge Carriers

The mobility μ of the charge carriers is a proportionality constant between the mean velocity of the charge carriers and the applied electric field $\vec{\boldsymbol{E}}$. It is dependent

on the crystal lattice, on the applied force and the effective mass m^* of the charge carrier. The effective mass m^* is the model mass of a charge carrier under the influence of an electric field. For both, electrons and holes the effective mass is different due to different band characteristics of the valence and conduction band. This leads to a different mobility for electrons μ_n and holes μ_p [26]:

$$\mu_n = \frac{q}{m_n^*}\tau_{av} \quad \text{and} \quad \mu_p = \frac{q}{m_p^*}\tau_{av}, \tag{12}$$

where m_n^* and m_p^* is the effective mass of electrons and holes and τ_{av} is the avarage scattering time of a charge carrier on the crystal lattice and crystal impurities. The avarage scattering time is a constant which describes the decrease of the drift velocity and thus the decrease of the total current after removing the electric field. Furthermore, μ_n and μ_p depend on the semiconductor since the effective mass is material dependent. Both equations from (12) lead to different velocities for electrons and holes in an electric field:

$$\vec{v}_n = -\mu_n\vec{E} \quad \text{and} \quad \vec{v}_p = \mu_p\vec{E}. \tag{13}$$

Fig. 5 shows the corresponding drift velocity of the charge carriers over the electric field. As noticeable, the drift velocity saturates at higher electric fields, which is
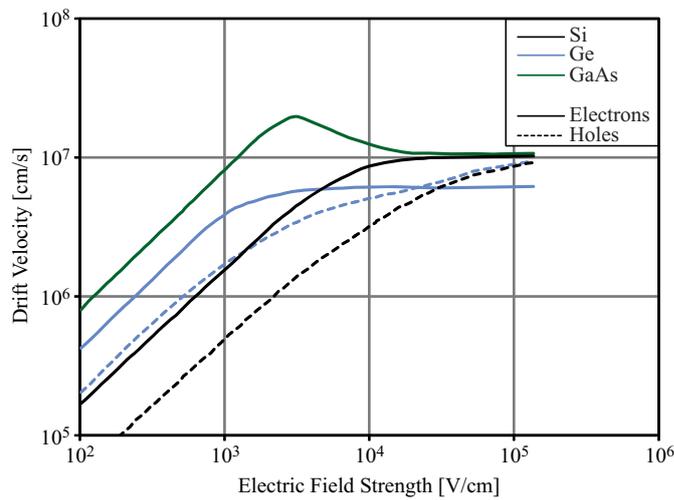
Figure 5: *Charge carrier drift velocity over electric field strength at 300 K for different semiconductor [26].*

caused by a decrease of the carrier mobility. This decrease arises due to a stronger scattering of the charges at the crystal lattice at higher electric fields [26].

3.4.3 Total Current Based on Drift and Diffusion Current

The transportation of electrical charge, and subsequently the current flow, takes place due to an applied force. Depending on this force the total current density is split in a drift current density $\vec{i}_{Drift}$ and a diffusion current density $\vec{i}_{Diff}$:

$$\vec{i} = \vec{i}_{Drift} + \vec{i}_{Diff}. \tag{14}$$

Drift Current Density

The drift current density is caused by an electrical field $\vec{E}$, which causes a charge movement. Inserting (13) into (11) leads to the total drift current in the semiconductor:

$$\vec{i}_{Drift} = q(p\mu_p + n\mu_n)\vec{E}. \tag{15}$$

The drift current is composed of an electron based current and a hole based current.

Diffusion Current Density

A spatial accumulation of charge carriers leads to a charge flow in the direction of a decreasing carrier concentration. Thus the flow is proportional to the negative gradient of the concentration. The energy for this movement is provided by the ambient temperature. This movement is described by the diffusion current density:

$$\vec{i}_{Diff} = q(D_n \, \vec{\nabla} n - D_p \, \vec{\nabla} p). \tag{16}$$

In (16) $\vec{\nabla}$ is the nabla operator and D_n and D_p are the diffusion constants for electrons and holes, respectively. The relation between these constants and the mobility is given by [27]:

$$D_n = \frac{kT}{q}\mu_n \quad and \quad D_p = \frac{kT}{q}\mu_p, \tag{17}$$

where k is the Boltzmann constant and T is the temperature. However, the diffusion current of minority charges drops down exponentially with the diffusion length L of the charge carriers:

$$L_n = \sqrt{D_n \tau_n} \quad and \quad L_p = \sqrt{D_p \tau_p},\tag{18}$$

where τ_n and τ_p are the lifetimes of the minority charge carriers in the p-doped and n-doped semiconductor, respectively [26–28].

3.4.4 Continuity Equations

The density of charge carriers in a considered volume can change only if charges flow away or flow into the volume or an imbalance between the generation and the recombination rate occurs. This process is described with the continuity equations, which can be derived from Gauss's theorem for a considered volume (Fig. 6) [26]:

$$\int_V \vec{\nabla} \cdot \vec{i} \, dV = \oint_{\partial V} \vec{i} \cdot d\vec{A},\tag{19}$$

$$\int_V (R - G) \, dV + \frac{\partial}{\partial t} \int_V p \, dV = -\frac{1}{q} \oint_{\partial V} \vec{i}_p \cdot d\vec{A},\tag{20}$$

$$\int_V (R - G) \, dV + \frac{\partial}{\partial t} \int_V n \, dV = \frac{1}{q} \oint_{\partial V} \vec{i}_n \cdot d\vec{A}.\tag{21}$$

Equation (20) and (21) are the continuity equations for holes and electrons for a considered volume. The first term of the left part is the difference between the recombination rate R and the generation rate G in the volume V. The second term of the left part gives the change of the number of the charge carriers in the volume. The right part of the equations shows the carrier flow through the boundary ∂V of the volume. The universal continuity equations for holes and electrons follow from (20) and (21):

$$\frac{1}{q} \vec{\nabla} \cdot \vec{i}_p + R - G = -\frac{\partial p}{\partial t},\tag{22}$$

$$-\frac{1}{q} \vec{\nabla} \cdot \vec{i}_n + R - G = -\frac{\partial n}{\partial t}.\tag{23}$$

4   Silicon Photodetectors

The seperation of the photogenerated charges of the following presented photodetectors is based on an inner electric field. The most commercially produced CMOS photodetectors using an inner electric field are photodiodes, avalanche photodiodes and phototransistors. Avalanche photodiodes and phototransistors have an inherent current amplification which leads to a higher quantum efficiency and thus to a higher responsivity compared to a photodiode. However, the current amplification mechanism of both detectors leads also to a higher output current noise compared to a photodiode. Regarding the frequency response behaviour the photodiodes achieve the highest bandwidths of the above mentioned three types of photodetectors. However, avalanche photodiodes and phototransistors do not require a further amplifier stage for the amplification of the detected signal.

The presented bipolar phototransistors in the following chapters are closely related to photodiodes and based on their functionality. Thus in the first part of this section an overview of photodiodes will be presented. The second part of this section gives a short introduction to avalanche photodiode to make the difference in the inherent current amplification between avalanche photodiodes and bipolar phototransistors more clearly. The last part introduces the theory on bipolar phototransistors.
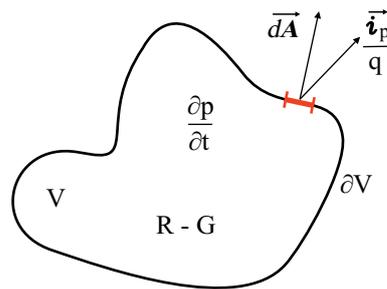
Figure 6: *Graphic representation of the continuity equation for holes [26].*

4.1 Photodiode

The connection of a p-type semiconductor with an n-type semiconductor forms a PN-diode. The difference in the carrier concentration in both semiconductor parts leads to a diffusion current flow of electrons into the p-type semiconductor and holes into the n-type semiconductor. This process builds up a space charge caused by the ionized acceptor and donor atoms in this region causing a formation of an electric field. Both, the diffusion of the charges and the electric field hold each other in equilibrium. The region where the electric field is present is called Space-Charge Region (SCR). Its width depends on the doping concentration of the n-type and the p-type semiconductor:

$$ w = l_p + l_n = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q} \left(V_D - V\right) \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}, \tag{24} $$

with

$$ V_D = \frac{kT}{q} \ln\frac{N_A N_D}{n_i^2}, \tag{25} $$

where l_p and l_n are the extensions of the SCR from the junction into the p-zone and n-zone, respectively, ε_0 is the permittivity in vacuum, ε_r is the relative permittivity of the semiconductor, V_D is the diffusion voltage, V is the applied voltage, N_A is the density of acceptors, N_D is the density of donors and n_i is the intrinsic charge carrier density of the semiconductor.

A thick SCR is desirable, since more photogenerated electron-hole pairs can be separated in the SCR by the electric field and will contribute to the total photocurrent. Photogenerated charges which are generated outside of the SCR will contribute only to the photocurrent if their diffusion lengths L_n and L_p are long enough to reach the SCR. Thus the probability for recombination increases the farther the charges are away from the SCR. Moreover, charges which are photogenerated close to the surface of the photodiode have a higher recombination probability due to traps caused by defects between the silicon surface and the silicon dioxide. Furthermore, it is desirable to reduce the diffusion current part and to increase the drift current part for achieving a faster response and a higher $-3\,\mathrm{dB}$ bandwidth. This can be achieved by increasing the thickness of the SCR by means of an applied reverse voltage. The resulting thicker SCR leads to a reduced

photodiode capacitance. Fig. 7 shows the transient behaviour and the frequency
response of the photocurrent for carrier drift and diffusion.

As presented in section 3.2 of the introduction chapter the penetration depth
of photons into semiconductor depends on their wavelength (see Fig. 3). Thus
the depth of the SCR from the top of the semiconductor should be adjusted to
optimize the quantum efficiency and the bandwidth of the photodetector. In a
CMOS process this optimization can be done by the use of different implemented
layers. E.g., if the wafer consists of a p-type substrate, than a highly doped and
thin n^+ layer can be implemented as a cathode. In this case the SCR would be
close to the surface, leading to an increased quantum efficiency for photons with
shorter wavelengths (e.g. 400 nm). Another possibility would be to use an n-well
instead of the n^+ layer. The n-well is lighter doped and thicker than the n^+ layer.
In this case the SCR would be thicker and deeper and optimized for wavelengths
in the range of 600 nm. To increase the quantum efficiency and the bandwidth of
the photodiode for deeper penetrating light (e.g. 850 nm) a lightly doped intrinsic
layer can be inserted between the anode and the cathode of the photodiode. This
structure is a so called PIN photodiode. Due to the low doping concentration of
the intrinsic layer, the SCR is spread over the whole intrinsic layer even for a small
applied reverse voltage. In Fig. 8 a comparison of the PN and the PIN photodiode
is shown. A 3D view of the PN and the PIN photodiode together with their SCRs
is depicted in Fig. 8a and 8b. The cathode is implemented as an n^+ layer. Fig. 8c
and 8d depicts the cross-section of the photodiodes. Their corresponding space
charge densities are shown in Fig. 8e and 8f. After the Poisson's equation these
space charge densities lead to the electric fields depicted in Fig. 8g and 8h:

$$\vec{\nabla} \cdot \vec{E} = \frac{\varrho}{\varepsilon_0 \varepsilon_r}, \tag{26}$$

and specially for the z-direction:

$$\frac{\partial}{\partial z} E(z) = \frac{q}{\varepsilon_0 \varepsilon_r} \left(N_D - N_A + p - n \right), \tag{27}$$

leading to:

$$E(z) = \frac{q}{\varepsilon_0 \varepsilon_r} \int (N_D - N_A + p - n) \, \mathrm{d}z. \tag{28}$$

The band bending, which is caused by the inner electric field in the SCR is depicted in Fig. 8i and 8j.

The electric field spreading within the PIN photodiode depends strongly on the applied voltage as well as on the doping concentration of the intrinsic layer. The lower the doping concentration of the intrinsic layer is the lower the applied voltage has to be for achieving a fully depleted intrinsic layer and a nearly constant electric field strength over the whole intrinsic layer. Fig. 9 depicts the electric field strength distribution over the depth of the photodiode for a PIN photodiode for
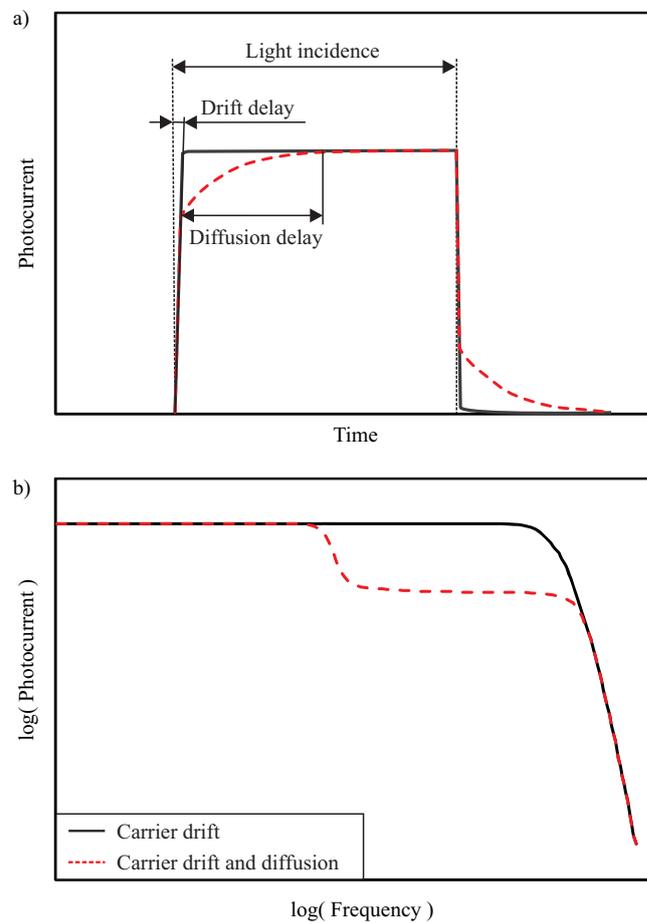
Figure 7: *Carrier drift and diffusion: a) transient behaviour, b) frequency response [22].*
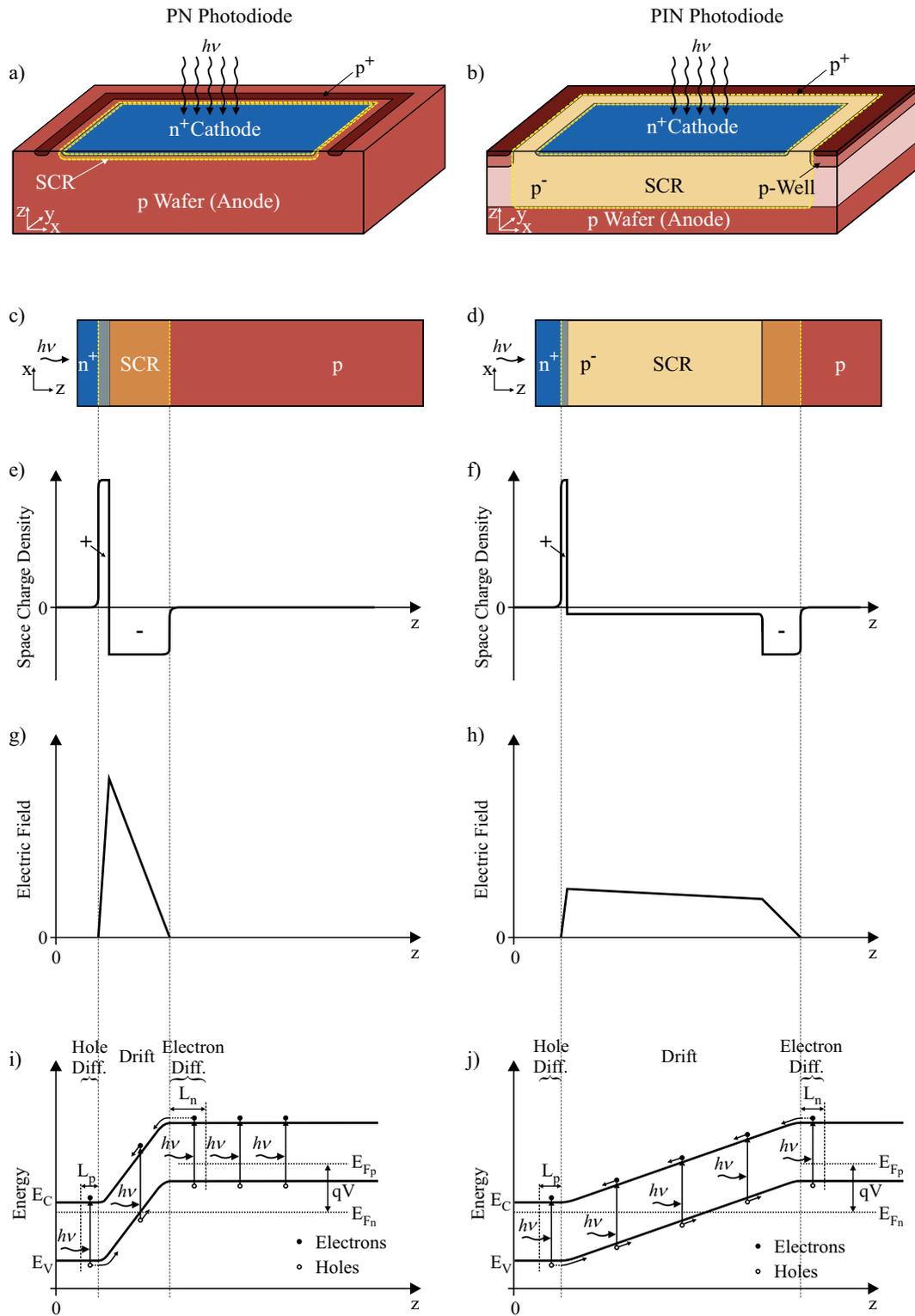
Figure 8: *Comparison PN and PIN photodiode at an applied reverse voltage V [23, 26].*

four different acceptor concentrations within the intrinsic layer. For this example the intrinsic layer is formed by a $15\,\mu m$ thick low doped p-epi layer on top of the p-substrate. The thermal budget of the production leads to a reduction of the depth of the effective low doped region to $\sim 10\,\mu m$. The strong dependence of the electric field strength on the doping concentration is noticeable. For a small applied photodiode voltage the doping concentration of the intrinsic layer has to be as low as possible for a fully depleted intrinsic layer with a nearly constant electric field within it.

4.2 Avalanche Photodiode

Compared to PN or PIN photodiodes, avalanche photodiodes (APDs) have an inherent current amplification and can achieve high quantum efficiencies. In an APD photogenerated electrons with sufficiently high energies can ionize atoms of the crystal. In this case the kinetic energies of the electrons have to be larger than the ionization energy of the atoms. The ionisation of the atoms leads to the generation of further electron-hole pairs. These electron-hole pairs are separated by the electric field in the SCR and can ionize further atoms. The whole process leads to a multiplication of the primary photogenerated electron-hole pair. However, for achieving the avalanche process the electric field in the SCR has to be very strong,
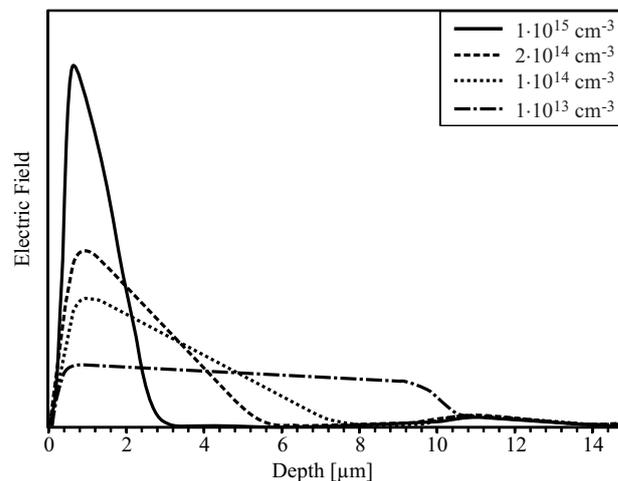
Figure 9: *Electric field spreading over the depth for different acceptor concentrations of the intrinsic p-layer in a PIN photodiode [22].*

which requires a high applied reverse voltage. Typically the voltage is around or beyond the breakdown voltage of the photodiode [23, 29].

The multiplication factor for the current amplification in an APD is composed of two multiplication factors based on the atom ionizations due to holes and electrons, respectively. Both multiplication factors differ from each other due to different ionization coefficients of holes and electrons, respectively. The ionization coefficients correspond to the impact ionization per unit length. Fig. 10 shows the ionization coefficients for holes α_p and electrons α_n in silicon and germanium.

The multiplication factors for holes M_p and electrons M_n in an APD equal [23]:

$$M_p = \frac{\left(1 - \frac{\alpha_n}{\alpha_p}\right) e^{\alpha_p w \left(1 - \frac{\alpha_n}{\alpha_p}\right)}}{1 - \frac{\alpha_n}{\alpha_p} e^{\alpha_p w \left(1 - \frac{\alpha_n}{\alpha_p}\right)}}, \tag{29}$$

$$M_n = \frac{\left(1 - \frac{\alpha_p}{\alpha_n}\right) e^{\alpha_n w \left(1 - \frac{\alpha_p}{\alpha_n}\right)}}{1 - \frac{\alpha_p}{\alpha_n} e^{\alpha_n w \left(1 - \frac{\alpha_p}{\alpha_n}\right)}}, \tag{30}$$

where w is the width of the SCR.

However, the carrier multiplication occurs only in the avalanche region of the APD where the electric field is highest. The electric field is highest in the area
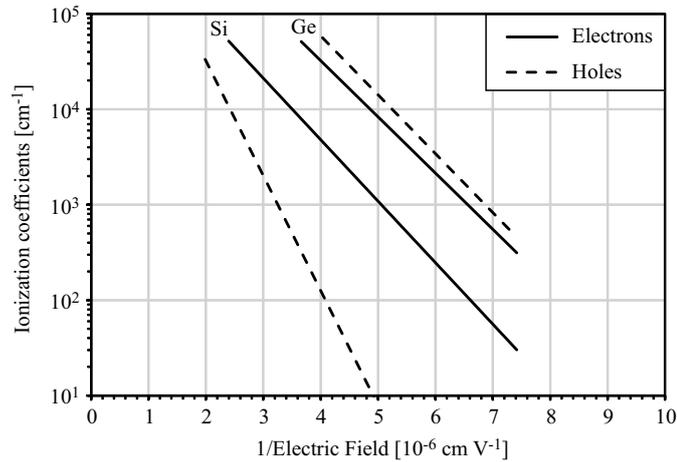
Figure 10: *Ionization coefficients in silicon and germanium as a function of the inverse of the electric field [29].*

of the PN junction. Fig. 11 shows two APD structures together with their space charge densities, electrical field and band bending for an applied reverse voltage. The sufficient electric field strength for avalanching E_A and the corresponding avalanche region are marked.

Furthermore the ionization coefficients α_p and α_n and the multiplication factor M are directly associated to the bandwidth $f_{-3\,\mathrm{dB}}$ of the APD [23]:

$$f_{-3\,\mathrm{dB}} = \frac{1}{2\pi M N \tau_{av} \frac{\alpha_p}{\alpha_n}}, \tag{31}$$

where τ_{av} is the mean transit time for carriers and N is a empirical value which depends on the ionisation coefficients and the electric field inside the SCR and takes values between 1/3 and 2 [23].

4.3 Bipolar Phototransistor

A further photodetector with an inherent current amplification is the phototransistor. Compared to avalanche photodiodes phototransistors do not need high voltages for their amplification, which is a major advantage especially in CMOS processes. Furthermore the noise performance of phototransistors is better than that of avalanche photodiodes [28].

Depending on the wafer material PNP and NPN bipolar phototransistors can be implemented in standard CMOS processes without additional masks. For a PNP phototransistor an n-well is implanted in the p-substrate. The p-substrate acts as the collector and the n-well acts as the base, respectively. A highly doped source/drain p-layer is implanted in the n-well acting as the emitter of the phototransistor. Since the collector is formed by the substrate material, it has to be at the lowest possible potential. This limits the operation of the phototransistor to an emitter follower configuration. Fig. 12a shows a 3D depiction of such a phototransistor.

In a phototransistor the base-collector diode acts as a photodiode. The photocur-
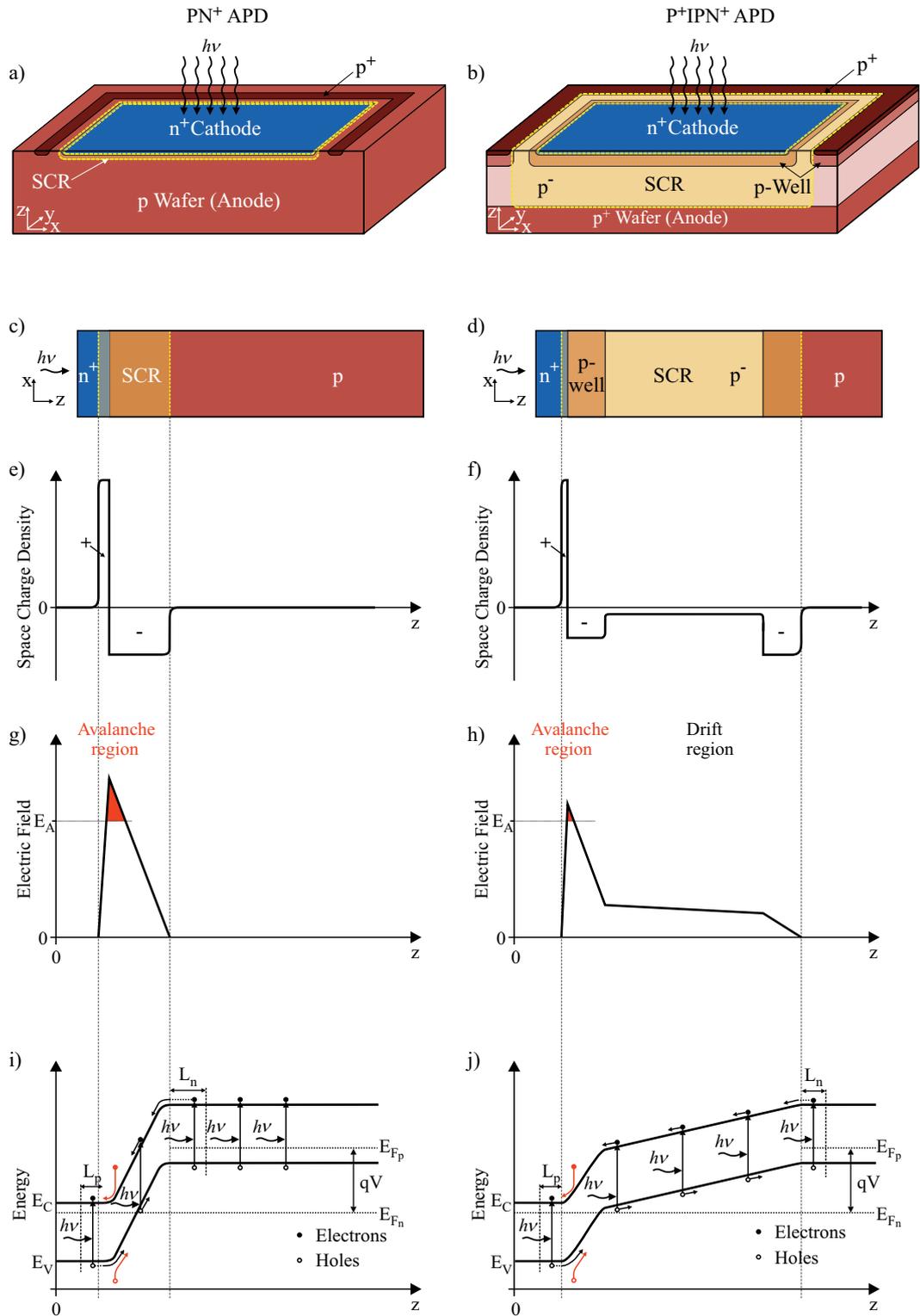
Figure 11: *Comparison of PN^+ and P^+IPN^+ APD structures at an applied high reverse voltage V [23, 26].*

rent injected into the base is multiplied by the current gain of the inherent transistor. In detail, a photogenerated electron-hole pair in the base-collector junction is split by the electric field. Thereby, in a PNP phototransistor the electron is swept towards the base and the hole towards the collector. The electron accumulation in the base makes the base potential more negative. Reaching the forward voltage of the base-emitter diode leads to a starting injection of holes from the emitter through the base towards the collector. As for a common bipolar transistor, it is important that the injected minority carriers in the base have a longer diffusion length than the effective base width. The effective base width w_B is the distance between both space-charge regions in the base (Fig. 12b). Furthermore, the ratio between the doping concentration of the emitter and the Gummel number of the transistor is important for the current gain. The Gummel number of the transistor corresponds to the integrated base doping concentration $N_{A/D}$ over the effective base width w_B. The value of this ratio should be as large as possible. A high ratio would lead to an improved hole injection efficiency in the base and thus to an increased current gain in a PNP phototransistor. These two main aspects are described in the current gain β of the phototransistor [23]:

$$\beta_{PNP} = \frac{D_p L_n N_A}{D_n w_B N_D} + 1 \qquad \text{for a PNP phototransistor,} \qquad (32)$$

$$\beta_{NPN} = \frac{D_n L_p N_D}{D_p w_B N_A} + 1 \qquad \text{for an NPN phototransistor.} \qquad (33)$$

In (32) D_p and D_n are the diffusion constants of the holes and electrons in the base and emitter, N_A and N_D are the acceptor and donor concentration in the emitter and the base, respectively, L_n is the diffusion length of electrons in the emitter and w_B is the effective base width.

The frequency response of a phototransistor is limited due to the capacitance of both SCRs and the base transit time τ_B. The total time τ_T, which an electron needs to reach the emitter from the collector is [29]:

$$\tau_T = \frac{C_{BE}}{g_m} + \frac{C_{BC}}{g_m} + \tau_B, \qquad (34)$$

where, C_{BE} and C_{BC} are the space-charge region capacitances of the base-emitter and base-collector diode. This leads to the f_{-3dB} bandwidth [23, 29]:

$$
\begin{aligned}
f_{-3dB} &= \frac{1}{2\pi\beta\tau_T} \\
&= \frac{1}{2\pi\beta\left(\frac{C_{BE}}{g_m} + \frac{C_{BC}}{g_m} + \tau_B\right)} \\
&= \frac{1}{2\pi\beta\left(\frac{kT}{qI_C}\left(C_{BE} + C_{BC}\right) + \tau_B\right)}.
\end{aligned}
\tag{35}
$$

In (35) I_C is the collector current of the phototransistor.

In both, photodiode and phototransistor, the responsivity and the frequency response can be improved by implementing a low doped intrinsic layer within the base-collector junction. This would lead to a PNP or NPN PIN phototransistor. In Fig. 12a the 3D view of such a PNP PIN phototransistor is presented. The responsivity increases since deeper photogenerated charge carriers are generated within the base-collector SCR and thus the probability for recombination is strongly reduced. On the other side, the bandwidth is improved since the spreading of the base-collector SCR would reduce the base-collector capacitance C_{BC}. According to (35), the C_{BC} reduction would improve the $-3\,\mathrm{dB}$ bandwidth f_{-3dB} of the phototransistor. In Fig. 12b, c, d, and e the cross section, the space-charge density, the electric field within the phototransistor, and the band structure for a PNP PIN phototransistor at an applied voltage are shown, respectively.

PNP PIN Phototransistor
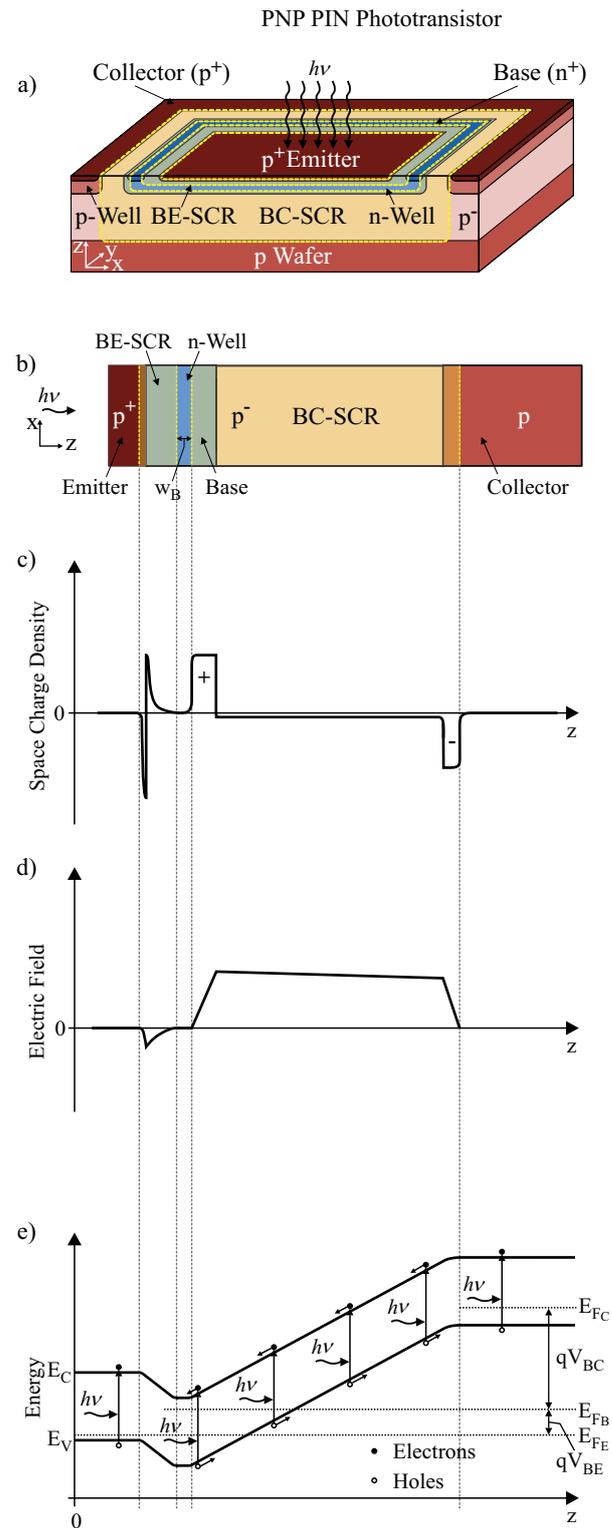
Figure 12: *PNP PIN phototransistor structure at an applied collector-emitter voltage [23, 26].*

References

[1] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[2] G. Castillo-Cabrera, J. Garcia-Lamont, M. A. Reyes-Barranca, J. Moreno-Cadenas, and A. Escobosa-Echavarria, "Optical characterization of integrated P+/N-Well/P-substrate and N-Well/P-substrate photo-device structures on CMOS technology," in *International Conference on Electrical Engineering Computing Science and Automatic Control (CCE)*, pp. 550–555, 2010.

[3] M. A. Abdallah, E. Dubaric, H.-E. Nilsson, C. Frojdh, and C. Petersson, "A Scintillator-coated Phototransistor Pixel Sensor with Dark Current Cancellation," in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, vol. 2, pp. 663–667, 2001.

[4] A. Tibuzzi, G.-F. D. Betta, C. Piemonte, C. D. Natale, A. D'Amico, and G. Soncini, "High gain bipolar junction phototransistors with finger-shaped emitter for improved optical gas sensing in the blue spectral region," *Sensors and Actuators A: Physical*, vol. 136, no. 2, pp. 588–596, 2007.

[5] Y. Huang and R. Hornsey, "Current-Mode CMOS Image Sensor Using Lateral Bipolar Phototransistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 12, pp. 2570–2573, 2003.

[6] R. Sandage and J. A. Connelly, "A 128×128 Imaging Array Using Lateral Bipolar Phototransistors in a Standard CMOS Process," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 6, pp. 641–644, 1998.

[7] R. Sandage and J. A. Connelly, "A Fingerprint Opto-Ddetector Using Lateral Bipolar Phototransistors in a Standard CMOS Process," in *International Electron Devices Meeting (IEDM)*, pp. 171–174, 1995.

[8] R. Sandage and J. A. Connelly, "Producing Phototransistors in a Standard Digital CMOS Technology," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp. 369–372, 1996.

[9] S. Espejo, A. Rodriguez-Vazquez, R. Dominguez-Castro, J. Huertas, and E. Sanchez-Sinencio, "Smart-Pixel Cellular Neural Networks in Analog Current-Mode CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 8, pp. 895–905, 1994.

[10] P. Chung-Yu Wu and C.-F. Chiu, "A New Structure of the 2-D Silicon Retina," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 890–897, 1995.

[11] A. Tibuzzi, G.-F. Dalla Betta, F. Ficorella, G. Soncini, C. Di Natale, and A. D'Amico, "Finger emitter/base bipolar junction phototransistors for optical gas sensing in the blue spectral region," in *IEEE Sensors Conference*, vol. 3, pp. 1581–1584, 2004.

[12] N. Tanaka, T. Ohmi, and Y. Nakamura, "A Novel Bipolar Imaging Device with Self-Noise-Reduction Capability," *IEEE Transactions on Electron Devices*, vol. 36, no. 1, pp. 31–38, 1989.

[13] G. Liang and W. Miller, "A Novel Photo BJT Array for Intelligent Imaging," in *Midwest Symposium on Circuits and Systems*, vol. 2, pp. 1056–1059, 1993.

[14] Y.-J. Kook, D.-Y. Chung, J.-H. Lee, C. H. Park, and H.-S. Min, "A new CMOS pixel with lateral and vertical BJT structure," in *IEEE Sensors Conference*, vol. 1, pp. 162–165, 2002.

[15] Y.-P. Lu, Y.-W. Chang, M.-Y. Lin, J.-S. Kao, Y.-T. Huang, and Y.-S. Yang, "CMOS Phototransistor Device: A total solution for Skin whitening Assays," in *IEEE International Conference on Nano/Molecular Medicine and Engineering (NANOMED)*, pp. 154–157, 2009.

[16] N. Jankovic and E. Jovanovic, "Variable-Gain Inversion Layer Emitter Phototransistor in CMOS Technology," in *IEEE International Semiconductor Conference (CAS)*, vol. 1, pp. 219–222, 2002.

[17] Y. Matsumoto, T. Hara, and Y. Kimura, "CMOS photo-transistor array detection system for visual light identification (ID)," in *IEEE International Conference on Networked Sensing Systems (INSS)*, pp. 99–102, 2008.

[18] A. Hu and V. P. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[19] A. Loaiza-Brito, R. Calzada, and L. Nino-de Rivera, "Foveal model of artificial retina with phototransistors in Darlington configuration in the high-resolution region," in *International Conference on Electrical and Electronics Engineering (ICEEE)*, pp. 174–177, 2005.

[20] J. Hurwitz, M. Panaghiston, K. Findlater, R. Henderson, T. Bailey, A. Holmes, and B. Paisley, "A 35 mm Film Format CMOS Image Sensor for Camera-Back Applications," in *IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 1, pp. 48–443, 2002.

[21] K. Kieschnick, H. Zimmermann, and P. Seegebrecht, "Silicon-based optical receivers in BiCMOS technology for advanced optoelectronic integrated circuits," *Materials Science in Semiconductor Processing*, vol. 3, no. 5-6, pp. 395–398, 2000.

[22] H. Zimmermann, *Integrated Silicon Optoelectronics*. Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[23] G. Winstel and C. Weyrich, *Optoelektronik II*. Berlin/Heidelberg, Germany: Springer-Verlag, 1986.

[24] E. Palik, *Handbook of Optical Constans of Solids*. San Diego, London: Academic Press, 1985.

[25] A. Ghazi, *Entwurf und Realisierung von Integrierten Photodetektoren und CMOS-Schaltkreisen für Optische Speichersysteme*. Wissenschaftsverlag Mainz, 2000.

[26] R. Müller, *Grundlagen der Halbleiter-Elektronik.* Berlin/Heidelberg, Germany: Springer-Verlag, seventh ed., 1995.

[27] A. Grove, *Physics and technology of semiconductor devices.* New York, USA: John Wiley, 1967.

[28] S. Sze and K. Ng, *Physics of Semiconductor Devices.* New York, USA: John Wiley & Sons, Inc., third ed., 2006.

[29] D. Decoster and J. Harari, *Optoelectronic Sensors.* Hoboken, London: Wiley-ISTE, 2009.

Publication A

PNP PIN Bipolar Phototransistors for High-Speed Applications Built in a 180 nm CMOS Process

Authored by P. Kostov, W. Gaberl, M. Hofbauer and H. Zimmermann

Abstract

This work reports on three speed optimized pnp bipolar phototransistors build in a standard 180 nm CMOS process using a special starting wafer. The starting wafer consists of a low doped p epitaxial layer on top of the p substrate. This low doped p epitaxial layer leads to a thick space-charge region between base and collector and thus to a high $-3\,$dB bandwidth at low collector-emitter voltages. For a further increase of the bandwidth the presented phototransistors were designed with small emitter areas resulting in a small base-emitter capacitance. The three presented phototransistors were implemented in sizes of $40 \times 40\,\mu\text{m}^2$ and

$100 \times 100\,\mu m^2$. Optical DC and AC measurements at 410 nm, 675 nm and 850 nm were done for phototransistor characterization. Due to the speed optimized design and the layer structure of the phototransistors, bandwidths up to 76.9 MHz and dynamic responsivities up to 2.89 A/W were achieved. Furthermore simulations of the electric field strength and space-charge regions were done.

1 Introduction

Photodiodes and phototransistors are the most commonly used photodetectors. By providing an additional gain, phototransistors are more suitable in some applications than photodiodes like for instance in low light scenarios. Nowadays photodetectors are built in silicon processes (these can also be standard CMOS or BiCMOS processes) or as III-V compound devices. Photodetectors integrated into standard silicon-based processes have several advantages over photodetectors realized in special silicon or III-V compound technologies. The main advantage of the implementation into a standard silicon process is the possibility for a cheap mass production of detector and circuitry together. The potential to combine the photodetector together with the readout circuitry to optoelectronic integrated circuits (OEICs) introduces further advantages of integrated solutions over wire-bonded solutions, due to the absence of bonding pads and bonding wires leading to less parasitic [1].

The physical property of silicon allows the material to be sensitive for wavelengths between 300 nm and 1100 nm. Light within this wavelength range will penetrate into the silicon and will be absorbed in it. Depending on the wavelength of the light, each photon can create one or more electron-hole pairs. A photon can create more than one electron-hole pair only if it is a high energy photon (corresponds to wavelengths below 375 nm) [2, 3]. However, the photon can also be absorbed by free carriers without generating an electron-hole pair (free carrier absorption) [4]. Nevertheless, if silicon photodetectors are used in the visible and near-infrared

range (400 nm - 900 nm), literature shows, that both mentioned effects can be neglected. Therefore for the visible light range the generation rate G of electron-hole pares in silicon can be simplified to [1]:

$$G(x, \lambda) = \Phi_0 \alpha(\lambda) e^{-\alpha(\lambda)x} \tag{1}$$

The generation rate G is dependent on the depth x from the semiconductor surface, on the wavelength λ, on the photon flux Φ_0 of the incident light and on the absorption coefficient α. The absorption coefficient α decreases strongly for increasing wavelength λ. To give two relevant examples: blue light (e.g. 430 nm) is absorbed in depths up to 0.2 μm while near infrared light (e.g. 850 nm) has a 1/e penetration depth of about 16.6 μm [1]. In a biased photodetector the electrical field separates the carriers. The wavelength dependent penetration depths lead to a wavelength dependent distribution of the total photocurrent into a drift and diffusion part, which further leads to wavelength dependent bandwidths and responsivities.

Photodiodes are the most common photodetectors. They can be implemented as a pn-junction or a pin-junction device. The difference between both structures is the additional low doped layer in the pin photodiode. In the junction region of the photodiode a space-charge region is formed. The space-charge region is thicker for the pin photodiode due to the additional low doped layer between the anode and cathode. For a vertical pin photodiode this will lead to a higher responsivity for deeper penetrating light and typically to a higher bandwidth since the drift current part is increased. PN photodiodes can be built in three different ways in a standard CMOS process using a p wafer: n-well/p-substrate, n$^+$/p-substrate and p$^+$/n-well. These diodes are characterized by a thin space-charge region and thus a small drift photocurrent, which leads to a relatively small bandwidth due to a large contribution of a diffusion current from photocharges generated below the space-charge region. However, by adding a thick intrinsic layer between the photodiode's anode and cathode, a thick space-charge region is formed and thus also a thick drift zone. A thicker drift zone leads to a larger fraction of drift current compared to diffusion current, which leads furthermore to higher bandwidths for

low bias voltages. The advantage of higher bandwidths in pin over pn photodiodes makes them the most commonly used detector for high speed optical applications, for example in optical receivers [5]. Such a vertical pin photodiode with a $-3\,\text{dB}$ bandwidth of $2.8\,\text{GHz}$ at $V_D = 20\,\text{V}$ and $0.2\,\text{A/W}$ for $850\,\text{nm}$ responsivity is presented in [6]. Another vertical pin photodiode with a responsivity of $0.135\,\text{A/W}$ for $850\,\text{nm}$ and a bandwidth of $1.6\,\text{GHz}$ at $V_D = 15.5\,\text{V}$ is presented in [7] Furthermore pin photodiodes can also be implemented as lateral devices. In [7] lateral pin photodiodes with responsivities up to $0.15\,\text{A/W}$ for $850\,\text{nm}$ and bandwidths up to $3.1\,\text{GHz}$ at $V_D = 15.5\,\text{V}$ are presented. For comparison the pn photodiodes presented in [8] reach a bandwidth of $80\,\text{MHz}$ at $V_D = 8\,\text{V}$ and responsivities of $0.215\,\text{A/W}$ and $0.15\,\text{A/W}$ for $650\,\text{nm}$. As can be seen on the presented values, photodiodes can achieve only small responsivities in the range of $600\,\text{nm}$ to $800\,\text{nm}$. This is due to a maximum quantum efficiency of $\eta = 1$. However, the maximum quantum efficiency cannot be reached in real devices due to reflection of the light at the surface as well as recombination of the photogenerated charges in the silicon.

Photodetectors with an inherent current amplification are introduced by avalanche photodiodes and phototransistors. Due to their inherent current amplification these photosensitive devices can improve the quantum efficiency limitation of photodiodes and reach values for η larger than 1.

Avalanche photodiodes achieve their inherent current amplification by an avalanche multiplication process. The drawback of this process is that voltages in the range of several tens of volts are needed to achieve sufficient electrical field strength for the inherent current amplification [9]. High voltages are a problem in integrated circuits and even more in modern low-voltage processes. However, new kinds of avalanche photodiodes, so called SPADs (single-photon avalanche photodiodes), can operate at smaller voltages than the standard avalanche photodiodes. In [10] two kinds of SPADs are presented with break-down voltages of $23.1\,\text{V}$ and $16.1\,\text{V}$, respectively. The very narrow bias voltage range for linear operation of APDs and SPADs is a further disadvantage of these kinds of photodetectors.

Phototransistors have the big advantage over APDs that they do not need high

voltages for their inherent current amplification. In BiCMOS, quite fast vertical npn phototransistors with responsivities of 2.7 A/W at 850 nm (due to the thin base-collector space-charge region) were reported [11]. Another BiCMOS SiGe phototransistor with a responsivity of 5.2 A/W at 850 nm is presented in [12]. In CMOS technology different types of phototransistors can be built, e.g. vertical bipolar phototransistors [13–18], lateral bipolar phototransistors [19], photo-MOSFETs [20], and so on. Vertical bipolar phototransistors with bandwidths up to 14 MHz and responsivities up to 98 A/W at 675 nm are presented in [13] and [14]. The CMOS lock-in amplifier presented in [15] uses pnp phototransistors with bandwidths of a few hundred kHz. Reference [16] describes a pnp phototransistor with a bandwidth of 7.8 MHz at 638 nm. In [17] a photodiode and a npn phototransistor in a 65 nm CMOS process are presented. The phototransistor achieves a responsivity of 0.34 A/W and a bandwidth of 150 kHz. This work describes extended results of the phototransistors presented in [18].

2   Working Principle

A vertical pnp phototransistor is formed in a CMOS process by implementing an n-well (base) in the p-substrate (collector) and a p^+-source/drain (emitter) in the n-well. Fig. 1a depicts the cross-section of a conventional pnp bipolar phototransistor. The pnp phototransistor can be used only in emitter-follower configuration since the substrate forms the collector. The phototransistor can be described as a photodiode (base-collector junction) and an internal bipolar junction transistor for the current amplification. Light with long wavelength penetrates deep into silicon and generates most charges in the base-collector space-charge region. There the charges are separated and electrons are swept into the base and holes into the collector. The electron accumulation in the base makes the potential of the base more negative, thus the forward bias voltage of the base-emitter diode increases and injection of holes from the emitter into the base becomes stronger. A large part of the injected holes can diffuse through the thin base and reach the base-collector space-charge region at the other end of the base area. This process leads to the amplification of the primary photocurrent. The inherent current amplification β is the relation between the collector current I_C and the primary

photocurrent I_{PH}. Further literature on conventional CMOS phototransistors can be found in [1, 21, 22].

3 Methodology

We present three speed optimized pnp PIN phototransistors with sizes of $40 \times 40\,\mu\text{m}^2$ and $100 \times 100\,\mu\text{m}^2$. The phototransistors are built in a $180\,\text{nm}$ CMOS process without any process modification and have been fabricated by LFoundry. For achieving high bandwidths a special wafer was used. This wafer consists of a p^+ substrate with a low doped ($5 \times 10^{13}\,\text{cm}^{-3}$) p epitaxial layer grown with a thickness of $15\,\mu\text{m}$ on it. A thick base-collector space-charge region is formed therefore even at low voltages due to the present low doped p epitaxial layer. The PIN structure of the base-collector diode has the same properties like the mentioned PIN photodiodes in section 1 and leads therefore to a fast separation of the photogenerated charges. As a consequence of the thick space-charge region the drift portion of the photocurrent for deep penetrating light rises and leads therefore to a higher responsivity compared to a conventional bipolar phototransistor like the one presented in [15].

The bandwidths and the responsivities of the phototransistors depend also on the layout properties of the base and emitter area. Eq. (2) shows the relationship between the $-3\,\text{dB}$ bandwidth of the phototransistor and the physical properties of the phototransistor [21]:

$$f_{-3dB} = \frac{1}{2\pi\beta(\tau_B + \frac{k_B T}{qI_E}(C_{BE} + C_{BC}))}, \tag{2}$$

where f_{-3dB} is the $-3\,\text{dB}$ bandwidth of the phototransistor, β is the forward current gain of the phototransistor, τ_B is the base transit time, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, I_E is the emitter current of the phototransistor, C_{BE} is the base-emitter capacitance and C_{BC} is the base-collector capacitance.

The $-3\,\text{dB}$ bandwidth depends on both space-charge region capacitances C_{BE} and

C_{BC}, current gain β, base transit time τ_B and the emitter current I_E. In case of large capacitance values the $-3\,\mathrm{dB}$ bandwidth is mainly dependent on both space-charge region capacitances C_{BE} and C_{BC}. For fast phototransistors a reduction of these capacitances is desired. In our presented phototransistors the capacitance C_{BC} is small compared to common phototransistors (e.g. Fig. 1a) due to the implemented thick low doped p epitaxial layer. Furthermore, a diminution of the capacitance C_{BE} is achieved by reducing the emitter area. Regarding the base doping two contrary effects have to be mentioned. On the one hand a reduction of the doping concentration in the base can lead to an increase of the bandwidth since both space-charge regions will reach deeper into the base leading to wider space-charge regions and thus smaller capacitances C_{BE} and C_{BC}. As a second consequence of larger space-charge region, the effective base width W becomes shorter leading to a reduced base transit time τ_B and thus also to an increased bandwidth. On the other hand, thicker space-charge regions will cause a reduction of the electric field strength inside the space-charge regions for the same potential conditions, leading to a slower device since the velocity of the charge carriers in the space-charge region will be reduced. This can be seen from the simulations in section 5.1. Furthermore the reduction of the base doping concentration leads to a higher inherent current gain β and thus to a higher collector and emitter current I_C and I_E. The higher emitter current will cause according Eq. (2) a higher bandwidth. Hence it follows that for phototransistors with generally small junction capacitances (e.g. optimized emitter layout, PIN structure) the frequency behavior of the device becomes more dependent on the other parameters like β, τ_B and I_E. A further increase of the bandwidth can be achieved by reducing the existing perimeter capacitance and further by reducing the size of the whole phototransistor. A reduction of the perimeter capacitance was achieved by adding a $3\,\mu\mathrm{m}$ gap with low doping between the n-well base and the p-well collector contact. However, the bandwidth of the PIN phototransistor is lower than the bandwidth of the PIN photodiode due to the both junction capacitances and the base transit time τ_B which is no issue in the photodiode.

As mentioned above, the bandwidth will increase when reducing the emitter area. On the other side, a smaller emitter area results in a smaller responsivity if the

whole device is illuminated. The reason for the smaller responsivity is the higher charge recombination probability due to a longer travel distance. Charges which are not generated directly under the emitter have to travel longer distances through the base to reach the base-emitter junction. These charges will contribute to the photocurrent only if their lifetimes are longer than the time they need to reach the base-emitter space-charge region. Regarding the responsivity the base doping concentration plays also a crucial role. For a smaller base doping concentration a thinner effective base width W is formed leading to a decreased travel distance of the generated charges through the base. This increases the probability for the charges to reach the base-emitter junction and thus also increases the inherent current amplification β. The inherent current amplification β is proportional to the emitter doping concentration N_E and the Gummel number N_G, which describes the doping concentration N_B of the base [22]:

$$N_G = \int_0^W N_B(x)\mathrm{d}x, \tag{3}$$

$$\beta \propto \frac{N_E}{N_G} \tag{4}$$

As a consequence we can say that for achieving high responsivities the photo-transistors should be designed with a large emitter over the whole photosensitive area together with a low doped base. Whereas for achieving higher bandwidths the phototransistors should be designed with very small emitter areas together with tendencially higher doped bases. It should be furthermore mentioned that by reducing the doping concentration of the base the probability for reach-through between collector and emitter increases, which should be avoided. However, the presented phototransistors are designed for high bandwidth applications and are implemented thus with small emitter areas. In the measurement section of this paper it can be seen that no reach-through arises for even high collector-emitter voltages.

4 Implemented Phototransistors

The three realized phototransistor versions (Fig. 1b, 1c and 1d) were built in $40 \times 40\,\mu m^2$ and $100 \times 100\,\mu m^2$ and have due to different layout designs of base and emitter different characteristics:

- $50_B Center_E$: This phototransistor was designed with a striped base. These n-well stripes have a width of $0.5\,\mu m$ and are separated by $0.5\,\mu m$ wide gaps between them. During the fabrication the n-well stripes will diffuse due to the thermal budget into one single layer with the half doping concentration of a base consisting of a full n-well. This is also the reason why this device is called $50_B Center_E$. The emitter of this device has the size of $0.74 \times 0.74\,\mu m^2$ and is placed in the center of the photosensitive area.

- $100_B Edge_E$: As can be seen from the name, this device consists of a full n-well base and an emitter at the edge of the photosensitive area. It has a slightly larger emitter area compared to the $50_B Center_E$ phototransistor due to the demands of the design rule specifications. The emitter area has a size of $2.18 \times 0.32\,\mu m^2$ and is formed by a p^+ drain/source implant. The idea for having the emitter at the edge of the photosensitive area is based on the idea of implementing an anti-reflection layer and an optical window etch on top of the photosensitive area and thus increasing the responsivity of the device. However, for a better comparison devices without an optical window edge were used.

- $100_B Quad_E$: This device has a similar layout as the device presented before. The difference between both phototransistors is that this device has four separate emitter areas. Each emitter area is placed in the center of each quadrant of the photosensitive area. All emitter areas are connected with minimum width metal lines on top of the phototransistor.

5 Results and Discussion

We characterized the presented phototransistors by optical DC and AC measurements. Optical DC measurements were done using a laser with $850\,nm$ wavelength

for the characterization of the phototransistors output characteristic and DC responsivity. Also, the spectral responsivity over the whole visible light spectrum was measured. Dynamic responsivity and bandwidth measurements of the phototransistors were done at 410 nm, 675 nm and 850 nm, respectively. The following equipment was used for the characterization of the phototransistors: the three mentioned laser sources, a monochromator for measuring the spectral responsivity, an optical attenuator and optical power meter for monitoring the light power, source-meter-units (SMU) for applying voltages and measuring current, an oscilloscope for measuring the AC responsivity and a vector network analyzer for measuring the frequency step response, respectively. All optical paths were calibrated with a fast optical reference photodiode. Furthermore the electric field strength and the space-charge regions of the phototransistors were simulated.
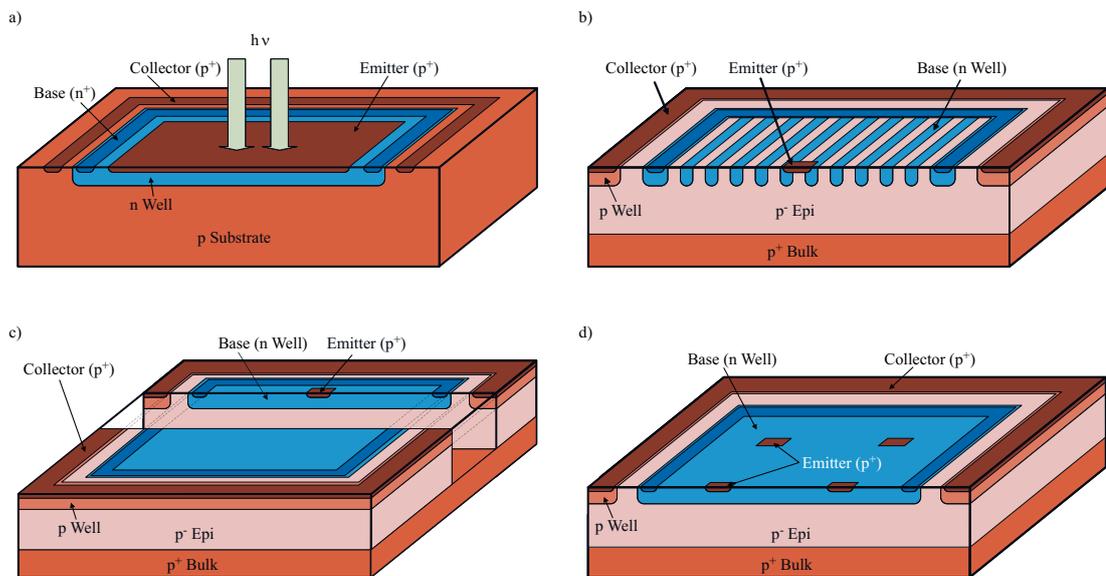
Figure 1: *3D depiction and cross section of the phototransistors: a) common pnp phototransistor integrated in CMOS technology, PIN PNP phototransistors: b) $50_B Center_E$, c) $100_B Edge_E$ and d) $100_B Quad_E$.*

5.1 Electric Field Strength and Space-Charge Region Simulation

Electric field strength and space-charge region simulations were done in order to make clear the variations between different collector-emitter voltages V_{CE} and different base doping concentrations. The phototransistor $50_B Center_E$ was simulated in dark light conditions at $V_{CE} = -2\,\mathrm{V}$, $-5\,\mathrm{V}$ and $-10\,\mathrm{V}$ always with floating base. Fig. 2 depicts the electric field strength in this phototransistor. In this figure the thick drift zone of the base-collector space-charge region and the strength of the electric field are noticeable. The peaks close to $Y = 0\,\mu\mathrm{m}$ are due to the contacts of collector, base and emitter of the phototransistor. For a better comparison of the electric field strength in the base-collector space-charge region for the three collector-emitter voltages the electric field strength was limited in the plot. Strong electric field strength peaks in the contact region are not shown to improve the scaling of the overall picture. The electric field strength in the base-emitter space-charge region reaches $35\,\mathrm{kV/cm}$. The borders of the space-charge regions for the $50_B Center_E$ phototransistor are depicted in Fig. 3. The phototransistor was simulated with a single n-well layer with the half doping concentration since the n-well stripes of this device will diffuse during the production into a single layer. Recognizable is the difference in the thickness of the base-collector space-charge region due to different collector-emitter voltages. In Fig. 4 the difference of the electric field between the $50_B Center_E$ and $100_B Edge_E$ phototransistor is depicted. Due to the lower doping concentration inside the base it is apparent that the $50_B Center_E$ phototransistor has wider space-charge regions but lower electric field strength compared to the $100_B Edge_E$ phototransistor. Thinner space-charge regions and thus higher electric field strengths in them will lead to a faster drift component. This can be seen in the bandwidth results section (section 5.3.2).

5.2 DC Characterization

The DC Characterization was split in two different measurement setups. First, the output characteristics were characterized and secondly the spectral responsivity was measured.
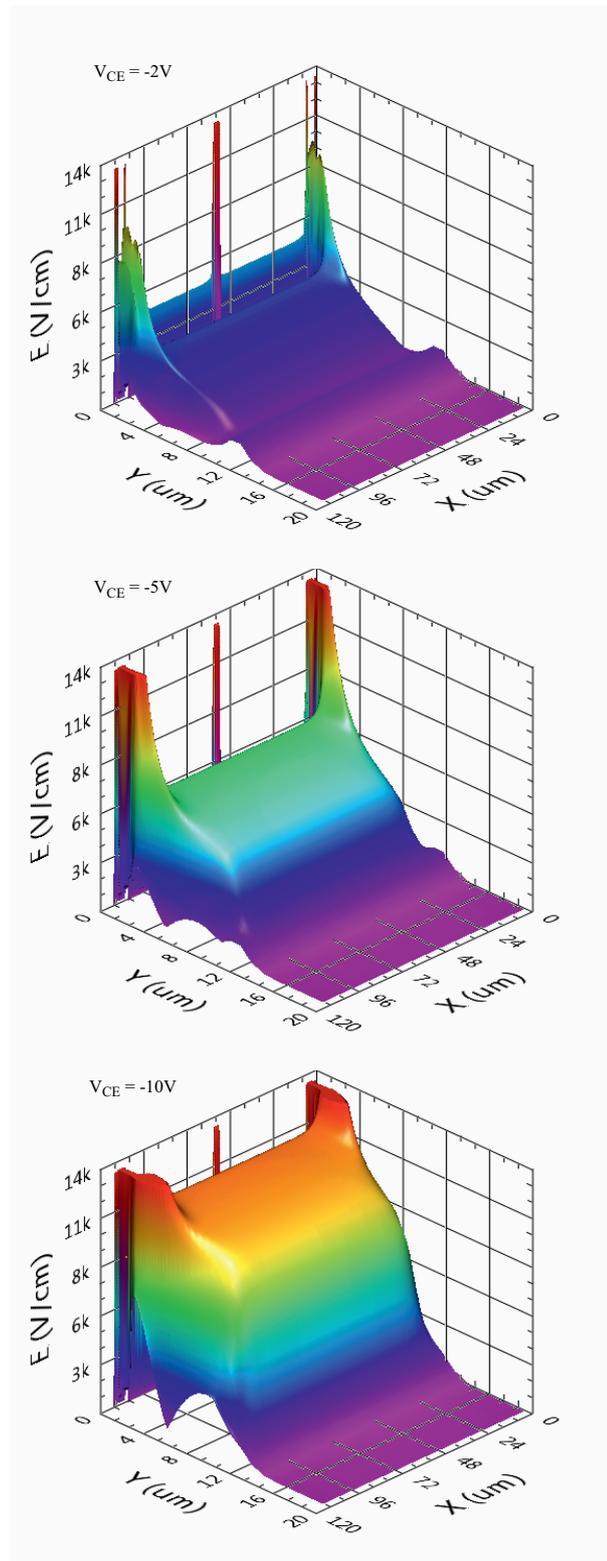
Figure 2: *Simulated electric field strength for the $50_B Center_E$ phototransistor at three different V_{CE} voltages.*
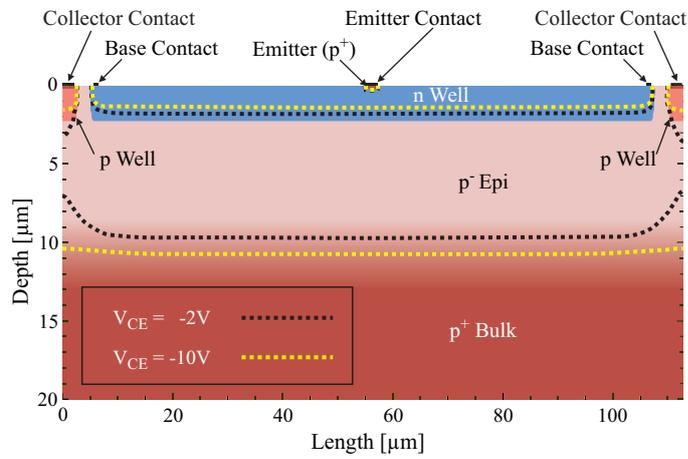
Figure 3: *Borders of the space-charge region at $V_{CE} = -2\,V$ and $-10\,V$ for the $50_B\,Center_E$ phototransistor.*
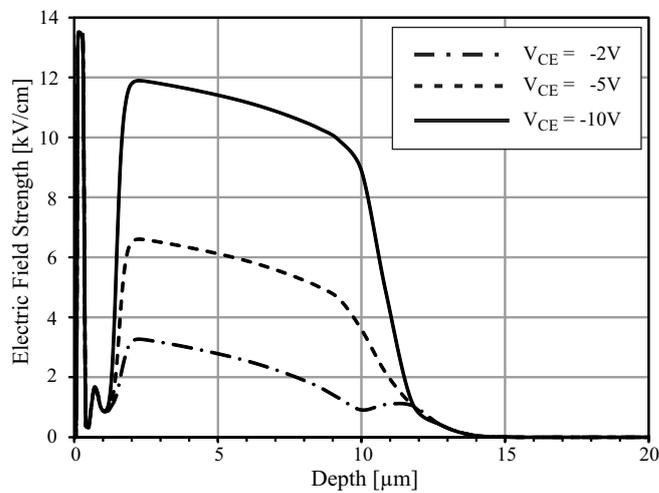
Figure 4: *Cross-section of the electric field strength at the center of the emitter of the $50_B\,Center_E$ and of the $100_B\,Edge_E$ phototransistor.*

5.2.1 I_C vs. V_{CE} Curve Family and Responsivity at 180 nm

For the characterization of the I_C vs. V_{CE} curve family (output characteristics) a light source with 850 nm wavelength was used. The operating point was changed by sweeping the collector-emitter voltage V_{CE} from 0 V to -13 V and the optical power between -37.7 dBm and -8.3 dBm. Thereby the light power was changed by an optical attenuator and monitored via an optical power meter. A source-meter-unit (SMU) was used on one hand to change the collector-emitter voltage and on the other hand to measure the collector current, respectively. The base contact was left floating. Fig. 5 depicts the output characteristics of the $100 \times 100 \, \mu m^2$ $50_B Center_E$ phototransistor. In this figure, it can be seen that for voltages V_{CE} up to -13 V no reach-through occurs. All other devices show an almost similar output characteristic like the depicted one.

The calculated DC responsivity for the $50_B Center_E$ and the $100_B Edge_E$ $100 \times 100 \, \mu m^2$ phototransistors at $V_{CE} = -10$ V is depicted in Fig. 6. The responsivity decreases for increasing optical light power due to a reduced gain in the phototransistor, which is caused by a change in the operating point as described in [13]. Thereby the higher optical light power induces a high collector current I_C which leads to a current density being larger than the critical current density $j_C \sim N_C$ (N_C is the collector doping concentration) given by the Kirk effect [23, 24] (also called base push out effect). Due to the doping concentration of $5 \times 10^{13} \, cm^{-3}$ in the collector layer (this is the thick p⁻ epitaxial layer) instead of usual collector doping levels above $10^{15} \, cm^{-3}$, the critical current density is reduced by about two orders of magnitude. Therefore, even at rather low collector currents, the current gain β reduces with increasing optical input power.

At weak optical light power the $50_B Center_E$ phototransistor shows a higher gain due to the lower doped base and thus a higher inherent current gain β. Phototransistor $100_B Quad_E$ has due to more emitter area a little bit higher responsivity as the $100_B Edge_E$ phototransistor. For all phototransistors the responsivity does not change much for different V_{CE}, since the collector current I_C is less dependent on different V_{CE} in the forward active region (see Fig. 5). In Tab. 1 the DC respon-
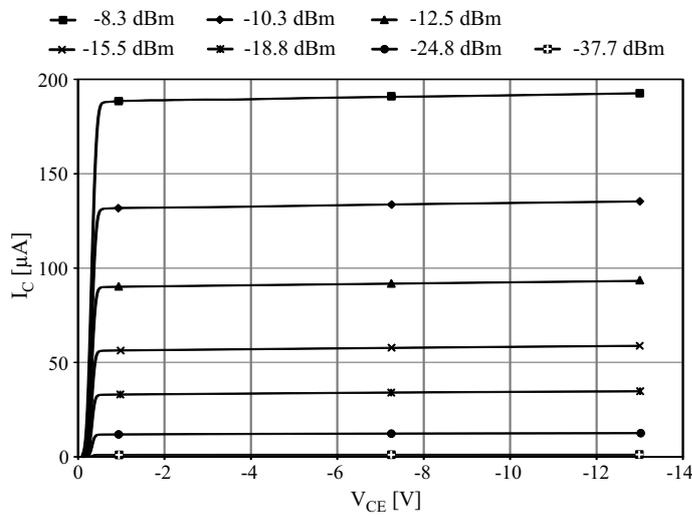
Figure 5: *Output characteristics of the $100 \times 100 \ \mu m^2 \ 50_B Center_E$ phototransistor at 850 nm for different optical power with floating base.*
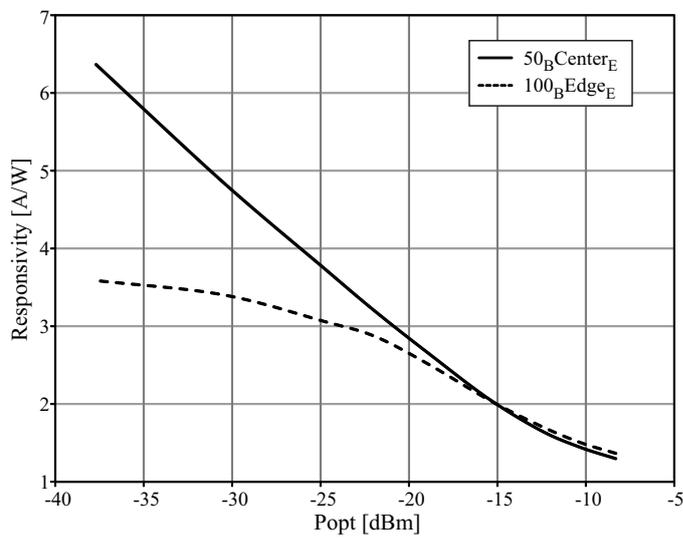
Figure 6: *DC responsivities of the $100 \times 100 \ \mu m^2 \ 50_B Center_E$ and $100_B Edge_E$ phototransistors at 850 nm at $V_{CE} = -10 \ V$.*

Table 1: *DC responsivity in A/W for the three $100 \times 100 \, \mu m^2$ phototransistors for three different collector-emitter voltages at 850 nm and an optical power of -37.7 dBm and -15.5 dBm.*

	$P_{opt}=-37.7$ dBm			$P_{opt}=-15.5$ dBm		
	$V_{CE}=-2$ V	$V_{CE}=-5$ V	$V_{CE}=-10$ V	$V_{CE}=-2$ V	$V_{CE}=-5$ V	$V_{CE}=-10$ V
$50_B Center_E$	6.12	6.23	6.37	2.01	2.03	2.07
$100_B Edge_E$	3.50	3.51	3.52	2.00	2.02	2.05
$100_B Quad_E$	3.57	3.57	3.59	2.63	2.65	2.68

sivities for the three $100 \times 100 \, \mu m^2$ phototransistors at different V_{CE} and different optical light power are shown.

5.2.2 Spectral Responsivity

The spectral responsivities of the phototransistors were measured by means of a monochromator. It was used to sweep the wavelength of the light from 400 nm to 900 nm. The optical light power of the monochromator changes thereby between -35.7 dBm and -26 dBm as depicted in Fig. 7a. The optical output power of the monochromator with attached optical fiber was measured with a calibrated reference photodiode. Then the fiber was adjusted to the phototransistors, whereby all light fell into their light sensitive area. A SMU was used to set the collector-emitter voltage and to measure the emitter current. The responsivity was then calculated from the measured emitter current and this incident light power. Fig. 7b shows the responsivity of the $50_B Center_E$ and the $100_B Edge_E$ $100 \times 100 \, \mu m^2$ phototransistors at $V_{CE} = -2$ V. The phototransistor $50_B Center_E$ shows a higher responsivity compared with the $100_B Edge_E$ phototransistor (compare with Fig. 6). A maximum responsivity is measured for all phototransistors in the red wavelength range. The oscillations, which can be seen in the spectral responsivity, are due to the influence of optical interference in the full oxide and passivation stack. They can be avoided by applying an optical window etch step together with an antireflection coating on top of the photosensitive area.
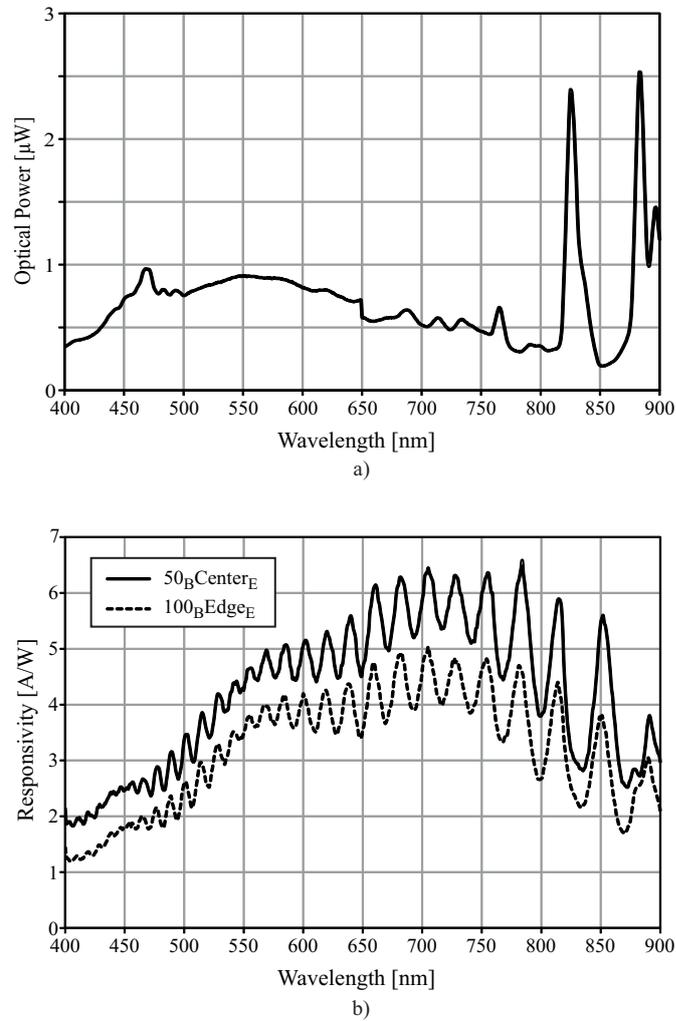
Figure 7: *Spectral measurements: a) emitted optical power of the monochromator and b) spectral responsivity of the $100 \times 100 \ \mu m^2$ $50_B Center_E$ and $100_B Edge_E$ phototransistors at $V_{CE} = -2 \ V$.*

5.3   AC Characterization: Responsivity and Bandwidth

AC responsivity measurements of the phototransistors were done at three different wavelengths: 410 nm, 675 nm and 850 nm. By using the same optical light power for the mentioned wavelengths different collector currents I_C will arise on the one hand due to different responsivities at each wavelength and on the other hand on different energy per photon for different light color. Therefore a comparison of the individual wavelengths would not be absolutely correct since the phototransistor would operate in various operating points for different wavelengths. For a better comparison, an alignment of the optical light power was applied to meet the same collector current I_C. Thus the mean optical light power at 410 nm was set to -12.7 dBm, at 675 nm it was set to -19.2 dBm and at 850 nm it was set to -15.8 dBm. Due to the used laser sources the extinction ratio was 2.00, 2.74 and 1.48 for 410 nm, 675 nm and 850 nm, respectively. During the AC characterization also different operating points were used for the phototransistors. Additionally the collector-emitter voltage V_{CE} was set to -2 V, -5 V and -10 V and the base current I_B was varied from floating condition (0 µA) to 1 µA, 2 µA, 5 µA and 10 µA. A bias-tee element together with an on-chip base-resistor was used to set the different operating points.

5.3.1   AC Responsivity

The dynamic responsivity was measured for the three mentioned wavelengths at a frequency of 630 kHz. The phototransistors were connected in emitter follower configuration and their output signal was capacitively coupled to the oscilloscope via a bias tee element. All phototransistors achieve rather small responsivities mainly due to the small emitter areas. These small emitter areas implicate a higher recombination probability of the charges inside the base area. This is caused by the fact that the charges have to travel longer distances to reach the emitter area. Only charges which are generated directly under the emitter have to pass only a short distance through the base to reach the base-emitter space-charge region. However, the phototransistors presented here are designed for achieving high bandwidths. In Tab. 2 the dynamic responsivities for the different phototransistors at different collector-emitter voltages V_{CE}, floating base and different wavelengths are

Table 2: *Dynamic responsivity in A/W for the three $100 \times 100 \ \mu m^2$ phototransistors for two different collector-emitter voltages at 410 nm (top), 675 nm (middle), 850 nm and floating base.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
$50_B Center_E$	0.45	0.48	1.93	1.95	1.34	1.36
$100_B Edge_E$	0.47	0.51	2.06	2.08	1.40	1.50
$100_B Quad_E$	0.71	0.74	2.81	2.89	2.20	2.34

presented. The highest responsivity of 2.89 A/W is achieved for the $100_B Quad_E$ phototransistor at $V_{CE} = -10$ V and 675 nm. By applying the above mentioned base currents the responsivity slightly decreases. This is caused by an arising base-push out effect and a reduced current gain β due to high base currents [23, 24]. Due to the demands of the design rule specifications the $100_B Edge_E$ phototransistor has a slightly larger emitter area which results also in a slightly higher responsivity compared to the $50_B Center_E$ phototransistor.

5.3.2 Bandwidth

The bandwidth characterization of the phototransistors was done by the means of a vector network analyzer (VNA). The phototransistors $50_B Center_E$ and $100_B Edge_E$ show nearly the same bandwidths. Phototransistor $100_B Quad_E$ achieves lower bandwidths due to more emitter area and thus a larger base-emitter capacitance C_{BE}. For the $50_B Center_E$ phototransistor the high bandwidth is mainly caused by the thin effective base width and thus short base transit time and furthermore smaller junction capacitances C_{BC} and C_{BE}. Regarding the $100_B Edge_E$ phototransistor, which is even slightly faster, the high bandwidth is dominated by the slightly higher electric field strength in the space-charge regions. These space-charge regions are slightly smaller due to the higher doped base area. Furthermore the small sized phototransistors show a higher bandwidth compared to the large sized ones. Here the smaller base-collector capacitance and a smaller perimeter capacitance are the main reasons. A higher bandwidth can be achieved by increasing the collector-emitter voltage V_{CE} and also by applying a base current I_B. The higher V_{CE} leads to wider space-charge regions, causing smaller

junction capacitances C_{BE} and C_{BC}, and consecutively to a thinner effective base width, causing a shorter base transit time. Furthermore the higher V_{CE} causes a stronger electric field strength inside the device (see Fig. 2). Fig. 8 shows the frequency response dependency on the size of the phototransistors as well as on the collector-emitter voltage V_{CE} at 850 nm for the $100_B Edge_E$ phototransistor. The -3 dB bandwidths are 12.0 MHz and 25.7 MHz for the $100 \times 100\,\mu m^2$ sized phototransistors and 14.2 MHz and 50.7 MHz for the $40 \times 40\,\mu m^2$ sized phototransistors at $V_{CE} = -2$ V and -10 V, respectively.

In Fig. 9 the bandwidths for the $100 \times 100\,\mu m^2$ $100_B Edge_E$ phototransistor at 850 nm and different operating points are depicted. The bandwidth increases with the base current until the collector current density reaches a maximum. At this point the largest homogeneous electric field exists in the base-collector space-charge region. By driving a higher collector current the charges cannot be carried completely by the electric field anymore [22]. Beyond the maxima in Fig. 9 the base push-out effect arises and leads to a spreading of the effective base into the collector [23, 24]. Thus the effective base width gets wider and the base transit time increases, leading according to Eq. (2) to a reduced bandwidth. However, it should be mentioned that the position of the maxima in Fig. 9 depend on the collector-emitter voltage V_{CE}. Hence an increase of V_{CE} leads also to an increase of the corresponding maximum collector current density and thus furthermore to an increase of the base current for the bandwidth maximum.

The difference in the bandwidth at different wavelengths for the $40 \times 40\,\mu m^2$ $100_B Edge_E$ phototransistor at $V_{CE} = -10$ V is shown in Fig. 10. The -3 dB bandwidths are 50.7 MHz at 850 nm, 76.9 MHz at 675 nm and 60.5 MHz at 410 nm for this phototransistor. In Tab. 3 the bandwidths for the three presented phototransistors at $V_{CE} = -2$ V and -10 V and floating base at the three different wavelengths are shown. The upper part of the table presents the results for the $40 \times 40\,\mu m^2$ and the lower one for the $100 \times 100\,\mu m^2$ devices. Noticeable is that phototransistor $100_B Quad_E$ shows a higher bandwidth for $V_{CE} = -2$ V compared to both other phototransistors. This is caused due to a shorter diffusion distance for the generated charges. Phototransistor $100_B Edge_E$ achieves the highest band-
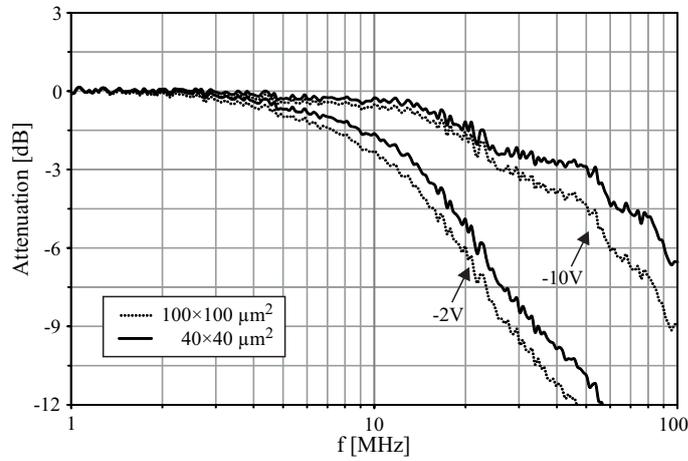
Figure 8: *Frequency response of the $40 \times 40 \ \mu m^2$ and $100 \times 100 \ \mu m^2$ $100_B Edge_E$ at 850 nm and floating base.*
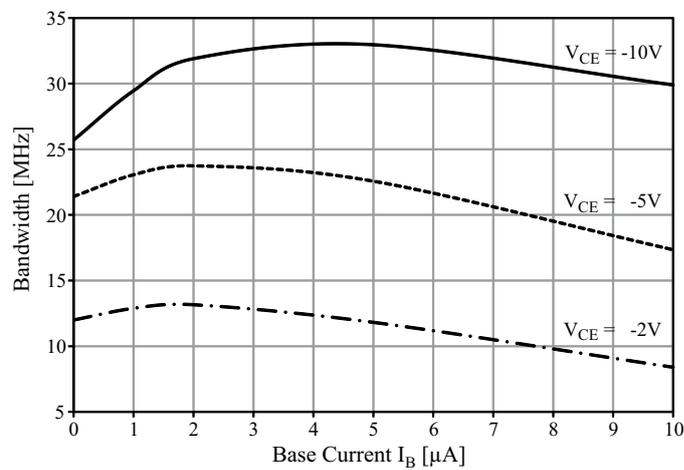
Figure 9: *Bandwidth dependence on base current at three different V_{CE} voltages for the $100 \times 100 \ \mu m^2$ $100_B Edge_E$ at 850 nm.*
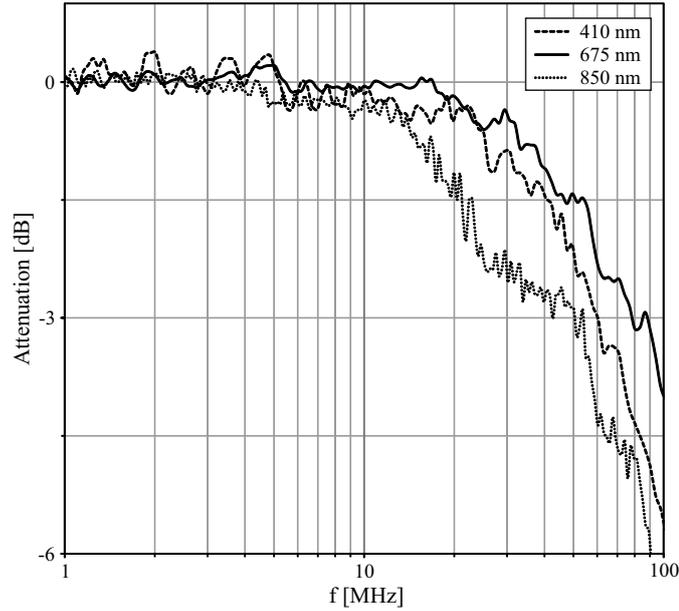
Figure 10: *Frequency response of the $40 \times 40\,\mu m^2$ $100_B Edge_E$ phototransistor at 410 nm, 675 nm, 850 nm and $V_{CE} = -10$ V.*

width due to stronger electric field strength in the space-charge regions (see Fig. 4). However, all devices achieve a maximal bandwidth at $675\,\mathrm{nm}$ due to an optimal light penetration depth. Thereby the main part of the charges is generated in the thick base-collector space-charge region and thus directly in the electric field zone.

6   Conclusion

In this work we present three types of speed-optimized pnp phototransistors built in a standard $180\,\mathrm{nm}$ CMOS process without modifications. Each type of phototransistor was fabricated with areas of $40 \times 40\,\mu\mathrm{m}^2$ and $100 \times 100\,\mu\mathrm{m}^2$. For achieving high bandwidths a PIN structure was used for the base-collector junction. Hence a special starting material was used consisting of the p^+ substrate and a low doped p^- epi layer grown on top of it. By this low doped epi layer a thick space-charge region is formed, which is necessary for a fast separation of the generated charges caused by deep penetrating light. Since the phototransistors were designed for high-speed applications a further bandwidth increase was achieved

Table 3: *Bandwidths in MHz of the three presented phototransistors at 410 nm, 675 nm, 850 nm as well as floating base and $V_{CE} = -2$ V and -10 V. The top table presents the values for the $40 \times 40\ \mu m^2$ phototransistors and the bottom table for the $100 \times 100\ \mu m^2$ phototransistors.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
$50_B Center_E$	10.7	57.5	9.6	67.0	12.8	50.0
$100_B Edge_E$	14.4	60.5	12.1	76.9	14.2	50.7
$100_B Quad_E$	20.2	54.2	18.8	60.3	18.6	31.6
$50_B Center_E$	9.8	36.5	9.1	54.0	10.5	25.1
$100_B Edge_E$	12.2	40.1	12.0	58.7	12.0	25.7
$100_B Quad_E$	16.6	34.0	16.1	51.6	15.8	21.4

Table 4: *Comparison of CMOS and BiCMOS phototransistors at 850 nm.*

Refs.	Technology	Device type	Dimension (μm^2)	Wavelength (nm)	P_{opt} (dBm)	Responsivity (A/W)	f_{-3dB} (MHz)	GBW (A/W MHz)
[11]	0.35 μm SiGe HBT BiCMOS	NPN	6×10	850	−17	2.7	2000	5400[a]
[12]	0.35 μm SiGe BiCMOS	PNP	21×25	850	−	5.2	−	−
[14]	0.6 μm CMOS	PNP	100×100	850	−21.2	1.8	14[b]	25.2
[15]	0.35 μm CMOS	PNP	35×35	−	−	−	< 1	−
[17]	65 nm CMOS	NPN	60×60	850	−	0.34	0.15	0.05
This work	0.18 μm CMOS	PNP	100×100 40×40	850	−15.8	1.5 1.44	25.7[b] 50.7[b]	38.6 73.0

[a] Small device illuminated with tapered fiber to get a 2.5 μm diameter optical spot.
[b] Fastest device for 850 nm.

by small emitter areas. This emitter area reduction leads also to a reduction of the base-emitter capacitance. However, the small emitter areas are disadvantageous for achieving high responsivities. Thus our phototransistors achieve only small dynamic responsivities up to 2.89 A/W as well as DC responsivities up to 6.44 A/W. Furthermore the phototransistors reach bandwidths up to 50.7 MHz at 850 nm, 76.9 MHz at 675 nm and 60.5 MHz at 410 nm at $V_{CE} = -10$ V and floating base conditions. These results are caused by the small capacitances and the high electric field strengths in the space-charge regions. Furthermore simulations of the electric field strengths and space-charge regions were done. Compared to the phototransistors described in [13] and [14], which were realized in 0.6 μm CMOS technology, the bandwidth is increased by more than a factor of 5. Therefore, these phototransistors are well suited for applications where a high-speed photodetector is needed with an inherent current amplification. A meaningful comparison of the presented phototransistors with other phototransistors is rather difficult since the device is strongly non-linear and its operating conditions are dependent on many factors (e.g. collector-emitter voltage, size of the device, optical light power, wavelength, additional base currents, etc.). However, the authors tried to give a comparison for 850 nm light, shown in Tab. 4. Possible applications for the presented phototransistors could be for example three dimensional cameras, fast opto-couplers and optical data receivers. Compared to an conventional PIN photodetector using an optimized PIN photodiode (with a responsivity of 0.4 A/W) the presented devices can be used to amplify the input signal up to a factor of 7.2, which equals an optical signal gain in the range of 8.6 dB.

Acknowledgements

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics.* Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] J. Geist and E. F. Zalewski, "The quantum yield of silicon in the visible," *Applied Physics Letters*, vol. 35, no. 7, pp. 503–505, 1979.

[3] O. Christensen, "Quantum efficiency of the internal photoelectric effect in silicon and germanium," *Journal of Applied Physics*, vol. 47, no. 2, pp. 689–695, 1976.

[4] D. Schroder, R. Thomas, and J. Swartz, "Free Carrier Absorption in Silicon," *IEEE Transactions on Electron Devices*, vol. 25, no. 2, pp. 254–261, 1978.

[5] R. Swoboda and H. Zimmermann, "11Gb/s Monolithically Integrated Silicon Optical Receiver for 850 nm Wavelength," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 904–911, 2006.

[6] J. Schaub, R. Li, S. Csutak, and J. Campbell, "High-Speed Monolithic Silicon Photoreceivers on High Resistivity and SOI Substrates," *Journal of Lightwave Technology*, vol. 19, no. 2, pp. 272–278, 2001.

[7] B. Ciftcioglu, L. Zhang, J. Zhang, J. Marciante, J. Zuegel, R. Sobolewski, and H. Wu, "Integrated Silicon PIN Photodiodes Using Deep N-Well in a Standard 0.18 μm CMOS Technology," *Journal of Lightwave Technology*, vol. 27, no. 15, pp. 3303–3313, 2009.

[8] M. Davidovic, G. Zach, K. Schneider-Hornstein, and H. Zimmermann, "TOF Range Finding Sensor in 90 nm CMOS Capable of Suppressing 180 klx Ambient Light," in *IEEE Sensors Conference*, pp. 2413–2416, 2010.

[9] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, pp. 1956–1976, 1996.

[10] L. Pancheri and D. Stoppa, "Low-noise Single Photon Avalanche Diodes in 0.15 μm CMOS Technology," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 179–182, 2011.

[11] T. Yin, A. Pappu, and A. Apsel, "Low-Cost, High-Efficiency, and High-Speed SiGe Phototransistors in Commercial BiCMOS," *IEEE Photonics Technology Letters*, vol. 18, no. 1, pp. 55–57, 2006.

[12] K.-S. Lai, J.-C. Huang, and K.-J. Hsu, "High-Responsivity Photodetector in Standard SiGe BiCMOS Technology," *IEEE Electron Device Letters*, vol. 28, no. 9, pp. 800–802, 2007.

[13] P. Kostov, K. Schneider-Hornstein, and H. Zimmermann, "Phototransistors for CMOS Optoelectronic Integrated Circuits," *Sensors and Actuators A: Physical*, vol. 172, no. 1, pp. 140–147, 2011.

[14] P. Kostov, W. Gaberl, and H. Zimmermann, "Visible and NIR integrated Phototransistors in CMOS technology," *Solid-State Electronics*, vol. 65-66, pp. 211–218, 2011.

[15] A. Hu and V. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[16] K. Kieschnick, H. Zimmermann, and P. Seegebrecht, "Silicon-based optical receivers in BiCMOS technology for advanced optoelectronic integrated circuits," *Materials Science in Semiconductor Processing*, vol. 3, no. 5-6, pp. 395–398, 2000.

[17] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[18] P. Kostov, W. Gaberl, and H. Zimmermann, "High-Speed PNP PIN Phototransistors in a 0.18 μm CMOS Process," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 187–190, 2011.

[19] R. Sandage and J. Connelly, "A Fingerprint Opto-Detector Using Lateral Bipolar Phototransistors in a Standard CMOS Process," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 171–174, 1995.

[20] W. Zhang, M. Chan, and P. Ko, "A Novel High-Gain CMOS Image Sensor Using Floating N-Well/Gate Tied PMOSFET," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1023–1025, 1998.

[21] G. Winstel and C. Weyrich, *Optoelektronik II.* Berlin/Heidelberg, Germany: Springer-Verlag, 1986.

[22] S. Sze and K. Ng, *Physics of Semiconductor Devices.* New York, USA: John Wiley & Sons, Inc., third ed., 2006.

[23] C. Kirk Jr., "A Theory of Transistor Cutoff Frequency (f_T) Falloff at High Current Densities," *IRE Transactions on Electron Devices*, vol. 9, no. 2, pp. 164–174, 1962.

[24] R. Whittier and D. Tremere, "Current Gain and Cutoff Frequency Falloff at High Currents," *IEEE Transactions on Electron Devices*, vol. 16, no. 1, pp. 39–57, 1969.

Publication B

High-Speed Bipolar Phototransistors in a 180 nm CMOS Process

Abstract

Several high-speed pnp phototransistors built in a standard 180 nm CMOS process are presented. The phototransistors were implemented in sizes of $40 \times 40\,\mu\text{m}^2$ and $100 \times 100\,\mu\text{m}^2$. Different base and emitter areas lead to different characteristics of the phototransistors. As starting material a p^+ wafer with a p^- epitaxial layer on top was used. The phototransistors were optically characterized at wavelengths of 410 nm, 675 nm and 850 nm. Bandwidths up to 92 MHz and dynamic responsivities up to 2.95 A/W were achieved. Evaluating the results, we can say that the presented phototransistors are well suited for high speed photosensitive optical applications where inherent amplification is needed. Further on, the standard silicon CMOS implementation opens the possibility for cheap integration of integrated

optoelectronic circuits. Possible applications for the presented phototransistors are low cost high speed image sensors, opto-couplers, etc.

Keywords: Phototransistor; CMOS; PIN

1 Introduction

During the last decades CMOS processes evolved to mature technologies, wherein a cheap implementation of integrated circuits is possible. Compared with III-V compound semiconductors, CMOS technologies have some major advantages like the possibility to combine silicon photodetectors together with the signal processing circuitry into an optoelectronic integrated circuit (OEIC). These single-chip devices exceed assemblies of wire bonded compound photodetectors and integrated circuits in many aspects. One advantage for example is the avoidance of the bond pads and bond wires between photodetector and read out circuitry. This for example leads to an excellent immunity against electromagnetic interference. Other advantages of CMOS OEICs over III-V solutions are the possibility for cheap mass production, easy handling, packaging, etc. [1].

Optical signals are converted into electrical signals by means of photodetectors. The most common photodetectors are photodiodes, phototransistors and avalanche photodiodes. However, Phototransistors as well as avalanche photodiodes have the advantage to increase the responsivity compared to simple photodiodes, due to their inherent current amplification.

Silicon photodetectors are able to detect wavelengths between $300\,\mathrm{nm}$ and to $1100\,\mathrm{nm}$ due to the physical properties of the material. Light in the mentioned wavelength range enters the silicon and is absorbed in it. The absorption of the photons leads to the generation of electron-hole pairs with a generation rate G [1]:

$$G(x, \lambda) = \Phi_0 \alpha(\lambda) e^{-\alpha(\lambda)x} \tag{1}$$

The generation rate G is dependent on the wavelength λ the depth x from the semiconductor surface, the photon flux Φ_0 of the incident light and the absorption

coefficient α. Light with short wavelength is absorbed near the semiconductor surface, while light in the near infrared region has a larger penetration depth and is therefore absorbed deep in the silicon. For example blue light with a wavelength of 430 nm generates electron-hole pairs in depths up to 0.2 µm while near infrared light with a wavelength of 850 nm has a $1/e$ penetration depth of about 16.6 µm [1]. Due to the wavelength dependent penetration depth of the light, the photodiodes and phototransistors will have also wavelength dependent bandwidths, since the distribution of the total photocurrent in drift and diffusion part is wavelength dependent. Compound photodetectors, for example InGaAs, InP, or GaAs have due to their material properties higher absorption coefficients α, which lead to small penetration depths in the range up to 1 µm from the surface. However, silicon photodetectors are preferable due to the above described advantages.

Photodiodes can be split in several subcategories. The PN photodiode can be mentioned as the most common photodetector. PN photodiodes consist of a simple p-n junction and are easily integrated into CMOS. This kind of photodiode can be implemented in three different ways. The n-well/p-substrate together with the n^+/p-substrate photodiodes can receive photons of the complete visible and the near infrared spectrum. However, the large $1/e$ penetration depth of near infrared light leads to long distances which charges have to travel in the field free diffusion region. Since the diffusion process is very slow, these kinds of PN diodes are characterized by a small bandwidth. However, the n-well/p-substrate structure has a higher bandwidth and a better responsivity compared to the n^+/p-substrate structure. This is mainly due to the deeper and lower doped n-well layer (compared to n^+), which results in a deeper and also thicker space-charge region. Thus, deep generated electrons have to travel shorter distances to reach the space-charge region, resulting in a higher bandwidth. As a third possibility, an isolated PN photodiode can be built. Thereby a p^+/n-well diode is implemented into the p wafer. Charges which are generated deep in the substrate do not contribute to the photocurrent due to the isolation of the PN diode from the substrate. However, charges generated in the active diode area are rapidly collected, which results in fast detectors, but with low responsivity. An n-well/p-substrate PN photodiode with a bandwidth of 1.6 MHz and a responsivity of 0.5 A/W at 780 nm for

a reverse bias voltage of $V_D = 5\,\text{V}$ is presented in [2]. In [3] an optical receiver using an n^+/p-substrate photodiode as well as an npn phototransistor built in a 65 nm CMOS process is presented. The paper states a photodiode responsivity of $0.03\,\text{A/W}$ and a bandwidth of $2.5\,\text{MHz}$ at 850 nm.

PIN photodiodes introduce some orders of magnitude higher bandwidth compared to standard PN photodiodes. They have an additional intrinsic layer between the cathode and anode. In CMOS technologies this low doped epitaxial layer is grown on top of the substrate material. This $10 - 15\,\mu\text{m}$ thick epi layer leads to a thick space-charge region between the anode and the cathode of the photodiode. By applying a relatively low reverse bias voltage a rather thick drift zone is formed, which results in a large amount of drift current and only a small fraction of diffusion current. As a consequence of the high drift current part, PIN photodiodes achieve very high bandwidths compared to PN diodes. Due to the advantages of PIN diodes over PN diodes, PIN diodes are the most commonly used detectors for high speed optical communication applications like optical receiver [3, 4], time-of-flight distance measurement applications [5–8], etc.

However, the responsivity of photodiodes cannot exceed the maximum limited by quantum efficiency $\eta = 1$. For example, for a wavelength of 850 nm the responsivity is limited to $0.65\,\text{A/W}$. A maximum quantum efficiency $\eta = 1$ cannot be reached in real devices due to reflection of the light at the detector surface as well as recombination of the photogenerated charges in the silicon. Thus in reality the achieved responsivities in reality are smaller and in the range of $0.2\,\text{A/W}$ for 410 nm, $0.55\,\text{A/W}$ for 675 nm and $0.35\,\text{A/W}$ for 850 nm.

Special kinds of photodetectors like avalanche photodiodes and phototransistors can improve the responsivity limitation of the PN and PIN photodiode by an inherent current amplification. By means of their internal amplification the can achieve quantum efficiencies $\eta > 1$. Due to this advantage e.g. the same light source can be used for longer transmission distances compared to PIN and PN photodiodes.

Avalanche photodiodes (APDs) achieve a high amplification of the photocurrent by an inherent avalanche multiplication process. However, the big drawback is the need for a high voltage supply of several tens of volts to achieve sufficient electrical field strength for avalanche amplification [9]. High voltages are a problem in integrated circuits and even more in modern low-voltage processes. However, single-photon avalanche photodiodes (SPADs) are a new kind of avalanche photodiodes, which can operate at smaller bias voltages compared to the described standard avalanche photodiodes. References [10–13] report single-photon avalanche photodiodes with breakdown voltages between 9.4 V and 23.1 V. Another disadvantage of SPADs and APDs is the very narrow bias voltage range for linear operation due to their strongly nonlinear behavior and thus the need for a complex control circuit.

The most important advantage of phototransistors over avalanche photodiodes is that they do not need high voltages for current amplification. Phototransistors can be built in different ways. Some examples for phototransistor implementations in CMOS technologies are vertical bipolar phototransistors [3, 14–20], lateral bipolar phototransistors [21] and photo-MOSFETs [22]. The 65 nm CMOS npn phototransistors described in [3] achieve a responsivity of 0.34 A/W and a bandwidth of 150 kHz at 850 nm light. Phototransistors with PIN structure show bandwidths up to 14 MHz and responsivities up to 76 A/W at 675 nm and 37.2 A/W at 850 nm [14]. In [15] a CMOS Lock-In Amplifier using standard CMOS pnp phototransistors with bandwidths of a few hundred kHz is described. Reference [16] and [17] report on npn phototransistors with responsivities of 0.25 A/W for the blue spectral range. Another pnp phototransistor with a current gain of 300 and a maximum bandwidth of 7.8 MHz at 638 nm is described in [18]. Some results of this work are presented in [19, 20].

2   Working Principle

The vertical bipolar pnp phototransistor is formed by the p-substrate, an n-well implant and a p^+ implant inside the n-well. A depiction of the cross-section of such a pnp phototransistor is shown in Fig. 1, wherein the base-collector junction acts as a PN photodiode. Since the collector is formed by the substrate, the pnp
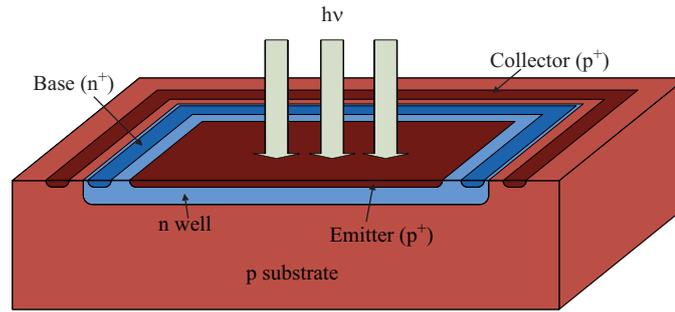
Figure 1: *Cross section of a common pnp phototransistor integrated in CMOS technology.*

phototransistor can only be used in emitter follower configuration. Two space-charge regions are present in the phototransistor, one between the base and the collector and another one between the base and the emitter. Charges generated by the incoming light are separated by the electrical field inside the space-charge regions. Assuming that the base is floating, the electrons are accumulated in the base and charge its potential more negative. The electron accumulation in the base leads to an increase of the base-emitter PN diode forward voltage, which implicates an injection of holes from the emitter into the base. A high portion of the injected holes diffuse through the base and reach the base the base-collector space-charge region. There they are swept into the collector by the electric field. The relation between the collector current I_C and the photocurrent I_{PH} is the inherent current amplification β of the phototransistor.

3 Methodology

In this work we introduce integrated vertical bipolar silicon phototransistors. The phototransistors were implemented in sizes of $40 \times 40 \, \mu m^2$ and $100 \times 100 \, \mu m^2$ in a 180 nm standard CMOS process without process modification. A special starting material was used to get a thick space-charge region at the base-collector junction. It consists of a 15 μm thick, low doped ($5 \times 10^{13} \, cm^{-3}$) epitaxial grown layer on top of the p-substrate. Due to this p⁻ epi layer a PIN structure is formed with the advantage of a thick drift zone and thus a large drift current part for deep penetrating light like 850 nm at low voltages. This characteristic leads to a fast

separation of the generated electron-hole pairs and furthermore to higher bandwidths compared to standard phototransistors. However, the bandwidth and also the responsivity of the phototransistors are also dependent on the size and design of the base and the emitter area. The characteristics of the phototransistors can be adjusted by changing the base and emitter designs.

3.1 Bandwidth and Photocurrent Amplification

For speed optimization all implemented phototransistors were built with small emitter areas. The reduction of the emitter size leads to a small base-emitter capacitance C_{BE} and thus to a higher $-3\,\mathrm{dB}$ bandwidth:

$$f_{-3dB} = \frac{1}{2\pi\beta(\tau_B + \frac{k_B T}{q I_E}(C_{BE} + C_{BC}))}, \tag{2}$$

where f_{-3dB} is the $-3\,\mathrm{dB}$ bandwidth of the phototransistor, β is the forward current gain of the phototransistor, τ_B is the base transit time, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, I_E is the emitter current of the phototransistor, C_{BE} is the base-emitter capacitance and C_{BC} is the base-collector capacitance [23].

On the other hand, the small emitter leads also to a reduced responsivity since the photogenerated charges have to travel longer distances to reach the emitter area which increases the probability for recombination. The base of the phototransistor is formed by a homogeneous n-well over the whole photosensitive area (Fig. 2a and Fig. 2b). For a further increase of the bandwidth the base-collector capacitance C_{BC} and thus the base-collector junction area should be reduced. This was done by implementing a second kind of base profile, where the base area was formed only by a small n-well under the emitter area as shown in Fig. 2c and Fig. 2d. A reduction of the perimeter capacitance leads also to a further increase of the bandwidth. Therefore a lateral $3\,\mu\mathrm{m}$ p^- epi layer gap was added between the n-well base and the p-well collector contact for the devices with a full n-well base. Applying a higher collector-emitter voltage V_{CE} will lead to thicker space-charge regions and thus to smaller base-collector and base-emitter capacitances. This furthermore

increases the $-3\,\mathrm{dB}$ bandwidth. Nevertheless, the bandwidth of phototransistors generally is lower than the bandwidth of PIN photodiodes. This is true on one hand because the phototransistor has two rather high junction capacitances C_{BE} and C_{BC} and on the other hand it is limited by the base transit time τ_B, which is no issue in a photodiode.

As mentioned before, the responsivity of the phototransistor will be small for a small emitter size due to a higher charge recombination probability. Charges which are not generated directly under the emitter will have to travel longer distances to reach the base-emitter junction. These charges will contribute to the photocurrent if their lifetime is longer than the time they need to reach the emitter. Otherwise they will recombine and get lost. The lifetime of the charge carriers is depending on the doping concentration of the base. Furthermore also the inherent current amplification of the phototransistor is depending on the doping concentration of the base. A small base doping concentration will lead to a small Gummel number and therefore to a high current amplification. The relation between base doping concentration N_B, Gummel number N_G and inherent current amplification β is shown in equations (3) and (4) [24]:

$$N_G = \int_0^W N_B(x)\,dx \tag{3}$$

$$\beta \propto \frac{N_E}{N_G} \tag{4}$$

where W is the effective width of the base and N_E the emitter doping concentration. The effective width W of the base is the distance between the borders of the base-emitter space-charge region and the base-collector space-charge region inside the base. However, if the effective base width gets too low a reach-through current between collector and emitter can occur. All our implemented phototransistors have a thick enough effective base width to prevent reach-through between the collector and emitter area even for high voltages. This is illustrated by the output characteristic measurements in the measurement results section. As a conclusion we can say that phototransistors for high responsivity should be designed with large emitters over the whole photosensitive area together with a low doped
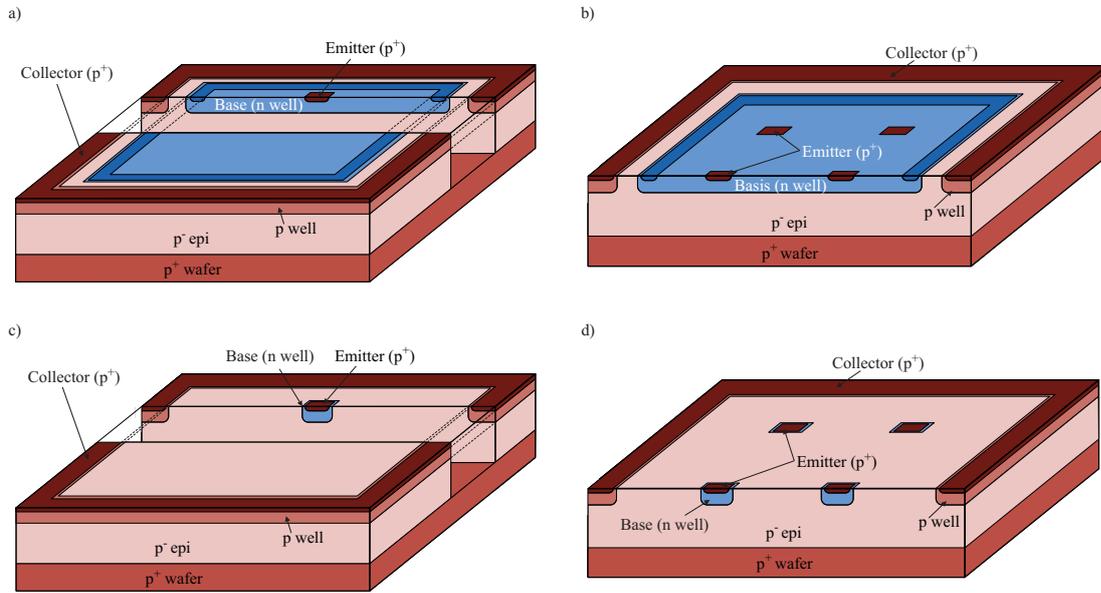
Figure 2: *3D depiction and cross section of the four presented phototransistors: (a) $PT_{EDGE}F_B$, (b) $PT_{QUAD}F_B$, (c) $PT_{EDGE}S_B$, (d) $PT_{QUAD}S_B$.*

base. However, our phototransistors are designed primary for higher bandwidth and therefor they have smaller emitters, with the tradeoff of a reduced responsivity.

3.2 Phototransistor Design

In this work we present four different kinds of phototransistors with different designs of base and emitter area:

- $PT_{EDGE}F_B$

- $PT_{QUAD}F_B$

- $PT_{EDGE}S_B$

- $PT_{QUAD}S_B$

Fig. 2 shows a depiction of the four phototransistors. All phototransistors have the same unique emitter area with a size of $2.18 \times 0.32\,\mathrm{\mu m}^2$. PT_{EDGE} phototransistors have their emitter area at the corner of the photosensitive area, wherein PT_{QUAD}

phototransistors have their emitter area in the center of each quadrant of the photosensitive area. The idea for heaving the emitter at the edge of the photosensitive area is based on the idea to have a flat photodetector surface without any contacts. Then it is possible to apply an ARC layer on top of the phototransistors which will lead to an increase of the responsivity by up to 3 dB. On the other hand, for achieving a higher responsivity the four emitter of the PT_{QUAD} were placed in the center of each quadrant of the phototransistor. As described in section 3.1., the small base (S_B) of the phototransistors was fabricated with the idea to reduce the base-collector capacitance C_{BC} and thus to increase the bandwidth compared to the phototransistors with a full base over the whole photosensitive area (F_B).

4   Measurement Results

The presented phototransistors were characterized by optical DC and AC measurements. The output characteristics and DC responsivity were measured by optical DC measurements at 850 nm. Furthermore the spectral responsivity was measured over the whole visible light range and near infrared range. Optical AC measurements were done for acquiring the responsivities, bandwidths and rise times of the phototransistors, respectively. The AC measurements were done at three different wavelengths: 410 nm, 675 nm and 850 nm.

4.1   Optical DC Measurements

4.1.1   Output Characteristics

The output characteristics of the devices were measured by applying an 850 nm light with different optical light power P_{opt} and varying the collector-emitter voltage V_{CE}. The optical light power P_{opt} was varied thereby from -37.7 dBm to -8.2 dBm. Fig. 3 depicts the output characteristics of the $100 \times 100 \, \mu m^2$ $PT_{QUAD}F_B$ phototransistor. As can be seen in Fig. 3 no reach-through occurs for V_{CE} voltages up to -13 V. The output characteristics of the other devices are similar to the presented one.
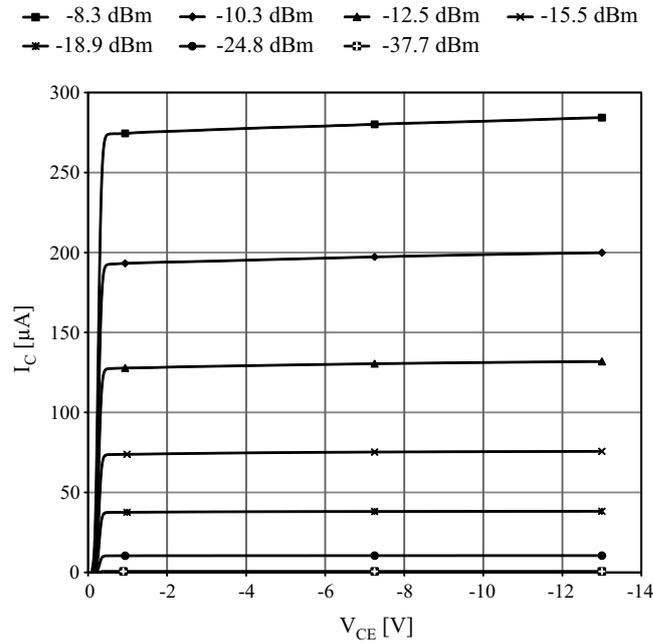
Figure 3: *Output characteristics of the 100 × 100 µm² $PT_{QUAD}F_B$ phototransistor at 850 nm for different optical powers.*

4.1.2 DC Responsivity

In Fig. 4 the calculated DC responsivity at $V_{CE} = -10\,\text{V}$ is depicted for the $100 \times 100\,\text{µm}^2$ $PT_{\text{QUAD}}F_B$ phototransistor. It can be seen, the responsivity decreases for increased optical light power. This is caused by a reduced gain in the phototransistor. The higher optical light power causes a change of the operating point and thus a different responsivity as described in [14]. As shown in Fig. 3 the collector current I_C has only a minor dependence on V_{CE} in the forward active region of the phototransistor. This leads to a nearly constant responsivity of the device over V_{CE}. Tab. 1 shows the DC responsivities of the $100 \times 100\,\text{µm}^2$ $PT_{\text{EDGE}}F_B$ and $PT_{\text{QUAD}}F_B$ phototransistors at $-2\,\text{V}$, $-5\,\text{V}$ and $-10\,\text{V}$ and an optical light power of $-15.5\,\text{dBm}$ and $-8.3\,\text{dBm}$.

4.1.3 Spectral Responsivity Measurements

Spectral responsivity measurements in the range from 400 nm to 900 nm were done using a monochromator. The used monochromator is based on a Spectral Prod-
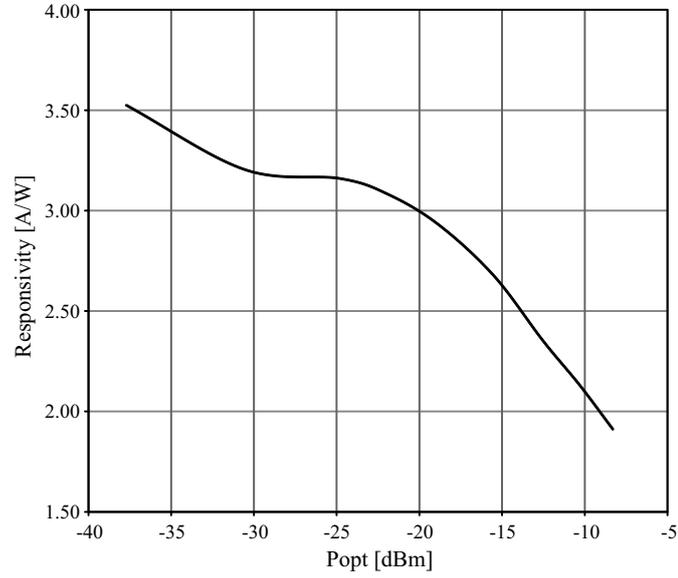
Figure 4: *DC responsivity of the $100 \times 100\,\mu m^2$ $PT_{QUAD}F_B$ phototransistor at 850 nm at $V_{CE} = -10\ V$.*

Table 1: *DC responsivity in A/W for the $100 \times 100\,\mu m^2$ $PT_{EDGE}F_B$ and $PT_{QUAD}F_B$ phototransistors for three different collector-emitter voltages at 850 nm and an optical power of -15.5 dBm and -8.3 dBm.*

	$P_{opt}{=}-15.5\,\mathrm{dBm}$			$P_{opt}{=}-8.3\,\mathrm{dBm}$		
	$V_{CE}{=}-2\,\mathrm{V}$	$V_{CE}{=}-5\,\mathrm{V}$	$V_{CE}{=}-10\,\mathrm{V}$	$V_{CE}{=}-2\,\mathrm{V}$	$V_{CE}{=}-5\,\mathrm{V}$	$V_{CE}{=}-10\,\mathrm{V}$
$\mathrm{PT_{EDGE}F_B}$	1.99	2.02	2.05	1.34	1.35	1.37
$\mathrm{PT_{QUAD}F_B}$	2.63	2.65	2.68	1.87	1.89	1.91

ucts Xenon Fiber Optic Lightsource ASB-XE-175, a Spectral Products Digikröm CM110 monochromator and optics for fiber coupling. Furthermore the device has a 50/50 splitter, which allows to monitor the actual output power in parallel to the measurement of the DUT (device under test). The optical power of the monochromator varied between $-35.7\,\mathrm{dBm}$ and $-26\,\mathrm{dBm}$ over the full spectrum (Fig. 5). Fig. 6 depicts the spectral responsivity of the $100 \times 100\,\mathrm{\mu m}^2$ phototransistors $\mathrm{PT_{EDGE}F_B}$ and $\mathrm{PT_{QUAD}F_B}$ measured at a collector-emitter voltage $V_{CE} = -2\,\mathrm{V}$. The phototransistor with the quad-emitter show a higher responsivity due to more emitter area and thus less recombination compared to the phototransistor with the edge emitter. A maximal responsivity is measured in the red wavelength range. Furthermore Fig. 6 shows oscillations in the spectral responsivity, which are caused by several oxide layers and one passivation layer. The oxide stack structure can be compared with a Fabry-Perot interferometer, which leads to reflection as well as to transmission dependent on the wavelength. The free spectral range $\Delta\lambda$, which describes the frequency spacing between the responsivity maxima, can be described with the following equation [25]:

$$\Delta\lambda = \frac{\lambda_0^2}{2nd \cos\theta} \tag{5}$$

Here λ_0 is the free-space wavelength, n is the refraction index of the layer, d is the thickness of the layer and θ is the angle of incidence. By applying an ARC layer together with an optical window etch step the oxide stack can be removed and described effects can be eliminated. Nevertheless, the diagrams are deviated slightly due to the varying operating point (mean optical power) at different wavelengths.

4.2 Optical AC Measurements

The optical AC measurements were done by using modulated light at $410\,\mathrm{nm}$, $675\,\mathrm{nm}$ and $850\,\mathrm{nm}$. For achieving the same collector current I_C, the measurements were done at different optical power for each wavelength. The results at $410\,\mathrm{nm}$ were acquired using a laser with an optical light power of $-12.7\,\mathrm{dBm}$ and an extinction ratio of 2. For $675\,\mathrm{nm}$ and $850\,\mathrm{nm}$ the light power was $-19.2\,\mathrm{dBm}$ and $-15.8\,\mathrm{dBm}$ and the extinction ratio of the laser was 2.74 and 1.48, respectively. Furthermore measurements were taken at different collector-emitter voltages V_{CE}.
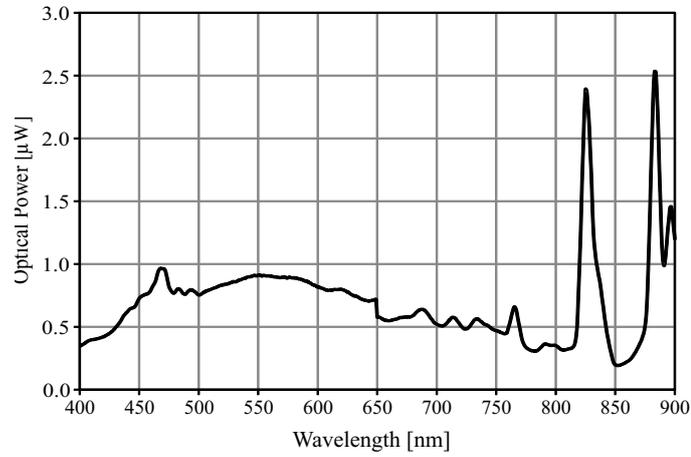
Figure 5: *Emitted optical power of the monochromator used for spectral responsivity measurements.*
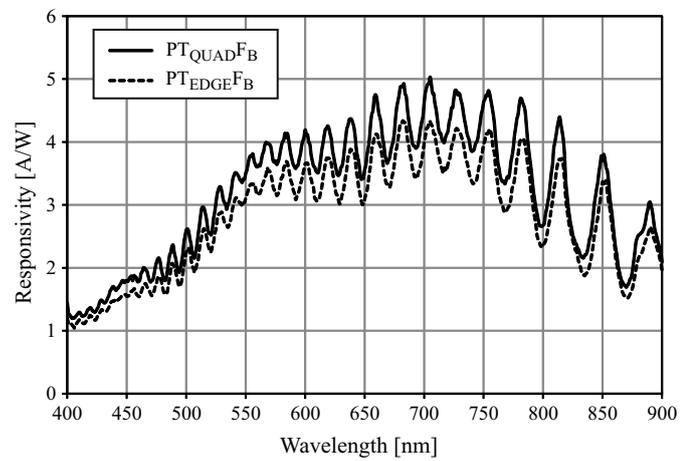
Figure 6: *Spectral responsivity of the $100 \times 100\,\mu m^2$ $PT_{EDGE}F_B$ and $PT_{QUAD}F_B$ phototransistors.*

Table 2: *Dynamic responsivity in A/W for the four 40 × 40 μm² phototransistors for two different collector-emitter voltages at 410 nm, 675 nm and 850 nm.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
PT$_{EDGE}$S$_B$	0.48	0.51	2.05	2.18	1.11	1.28
PT$_{EDGE}$F$_B$	0.64	0.67	1.94	1.97	1.40	1.44
PT$_{QUAD}$S$_B$	0.67	0.72	2.73	2.95	1.70	1.78
PT$_{QUAD}$F$_B$	0.86	0.87	2.47	2.63	2.12	2.18

4.2.1 AC Responsivity

The phototransistors achieve small responsivities due to their small emitter sizes, as already described in section 3. Based on the fact that charges have to travel longer distances to reach the emitter area, the recombination probability is increased, which leads to a small responsivity. However, the presented phototransistors were designed and optimized for high-speed applications. Tab. 2 presents the responsivity values for the $40 \times 40\,\mu m^2$ phototransistors at the three wavelengths and different collector-emitter voltages V_{CE}. The responsivity values for the $100 \times 100\,\mu m^2$ sized phototransistors have only a minor change compared to the big sized ones. As expected the results show the highest responsivity for red light (675 nm). The maximum achieved responsivity is thereby 2.95 A/W for the $40 \times 40\,\mu m^2$ PT$_{QUAD}$S$_B$ phototransistor at $V_{CE} = -10\,V$.

4.2.2 Bandwidth Measurements

The bandwidth of the devices was measured by means of a vector network analyzer (VNA). A depiction of the bandwidth measurement setup is shown in Fig. 7. Phototransistors with a small base (S$_B$) under the emitter area show higher bandwidths than phototransistors with a full base (F$_B$), due to a smaller base-collector capacitance C_{BC}. Furthermore the $40 \times 40\,\mu m^2$ devices show higher bandwidths compared to the $100 \times 100\,\mu m^2$ devices because of a smaller base-collector capacitances C_{BC} as well as e smaller perimeter capacitance. By increasing the collector-emitter voltage V_{CE} both space-charge regions become thicker. This leads to smaller junction capacitances C_{BC} and C_{BE} and as shown in equation

(2) to a higher bandwidth. In Fig. 8 the dependence of the bandwidth on the phototransistor size together with the collector-emitter voltage V_{CE} is depicted for the phototransistor $PT_{QUAD}F_B$ at 675 nm. Tab. 3 shows the bandwidth values for this phototransistor with both mentioned sizes. In Fig. 9 the measured frequency response of the $40 \times 40\,\mu m^2$ $PT_{EDGE}S_B$ phototransistor for the three mentioned wavelengths at a collector-emitter voltage $V_{CE} = -10\,V$ is depicted. This device achieves maximum bandwidths of 60.3 MHz, 92.0 MHz and 50.0 MHz at 410 nm, 675 nm and 850 nm, respectively. Bandwidths for this and the other $40 \times 40\,\mu m^2$ phototransistors at the three wavelengths and different collector-emitter voltages are presented in Tab. 4. The frequency bandwidth at $V_{CE} = -2\,V$ is noticeable, since the quad emitter devices have a higher bandwidth than the edge emitter devices. This is caused by shorter diffusion distances for generated charges. For all devices the bandwidth maximum is achieved at 675 nm since at this wavelength the main part of the charges is generated in the base-collector space-charge region. All of these charges are directly generated in the electrical field zone. For low collector-emitter voltages $V_{CE} = -2\,V$ the base-collector space charge region will not extend over the whole detector area. Therefor even for 675 nm the device is slow compared to the higher collector-emitter voltage ($V_{CE} = -10\,V$). Nevertheless, for 850 nm the thickness of the whole device is more important than the lateral dimension so phototransistors at low collector-emitter voltages have a higher bandwidth for 850 nm.
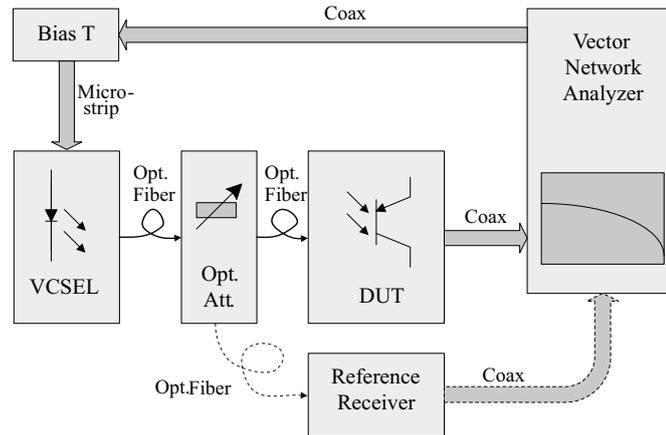
Figure 7: Setup for frequency response measurements.
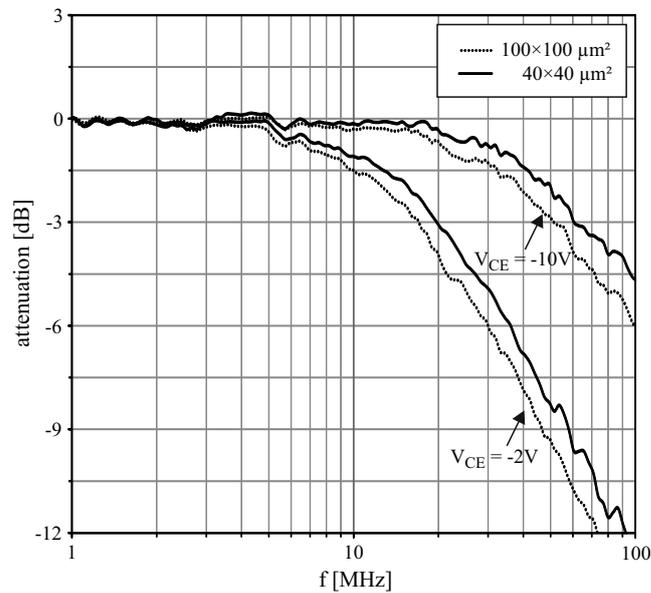
Figure 8: *Frequency response of the $40 \times 40\,\mu m^2$ and $100 \times 100\,\mu m^2$ $PT_{QUAD}F_B$ phototransistor at 675 nm and $V_{CE} = -2\,V$ and $-10\,V$.*
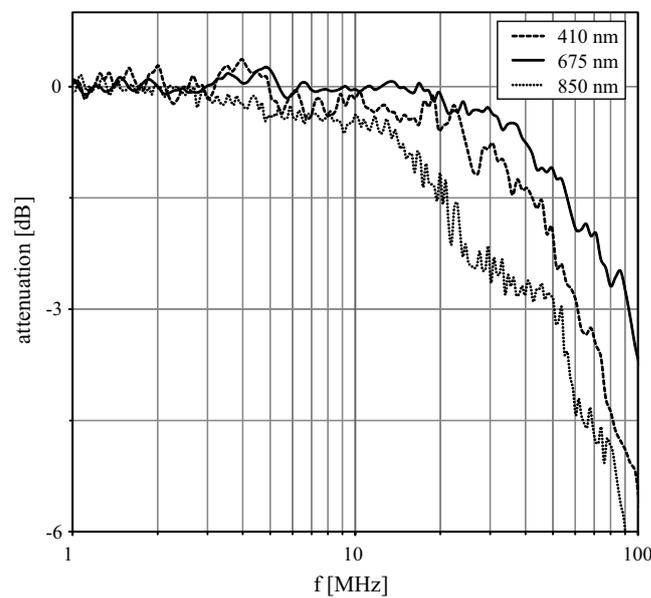
Figure 9: *Frequency response of the $40 \times 40\,\mu m^2$ $PT_{EDGE}S_B$ phototransistor at 410 nm, 675 nm, 850 nm and $V_{CE} = -10\,V$.*

Table 3: *Bandwidth values in MHz for the $40 \times 40\,\mu m^2$ and $100 \times 100\,\mu m^2$ $PT_{QUAD}F_B$ phototransistor for two different collector-emitter voltages.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
$40 \times 40\,\mu m^2$	20.2	54.2	18.8	60.3	18.6	31.6
$100 \times 100\,\mu m^2$	16.6	34.0	16.1	51.6	15.8	21.4

Table 4: *Bandwidth in MHz for the four $40 \times 40\,\mu m^2$ phototransistors for two different collector-emitter voltages at 410 nm, 675 nm and 850 nm.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
$PT_{EDGE}S_B$	13.2	60.3	9.6	92.0	12.0	50.0
$PT_{EDGE}F_B$	12.2	58.6	12.1	77.4	12.8	50.0
$PT_{QUAD}S_B$	20.0	52.0	13.8	72.5	19.1	37.2
$PT_{QUAD}F_B$	20.2	54.2	18.8	60.3	18.6	31.6

4.2.3 Step Response Measurements

Step response measurements were done for the phototransistors at 410 nm, 675 nm and 850 nm. Fig. 10 depicts the step function of the $40 \times 40\,\mu m^2$ $PT_{EDGE}S_B$ at $V_{CE} = -2\,V$ and $V_{CE} = -10\,V$. This measurement was done at 675 nm with an optical light power of $-19\,dBm$. The laser was modulated with 630 kHz. Rise times for this device and the other $40 \times 40\,\mu m^2$ phototransistors at different wavelengths and at different collector-emitter voltages are presented in Tab. 5.

Table 5: *Rise times in ns for the four $40 \times 40\,\mu m^2$ phototransistors for two different collector-emitter voltages at 410 nm, 675 nm and 850 nm.*

	λ=410 nm		λ=675 nm		λ=850 nm	
	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V	V_{CE}=−2 V	V_{CE}=−10 V
$PT_{EDGE}S_B$	27	5	44	12	41	7
$PT_{EDGE}F_B$	20	5	37	15	41	8
$PT_{QUAD}S_B$	16	8	28	13	40	11
$PT_{QUAD}F_B$	17	7	31	19	40	13
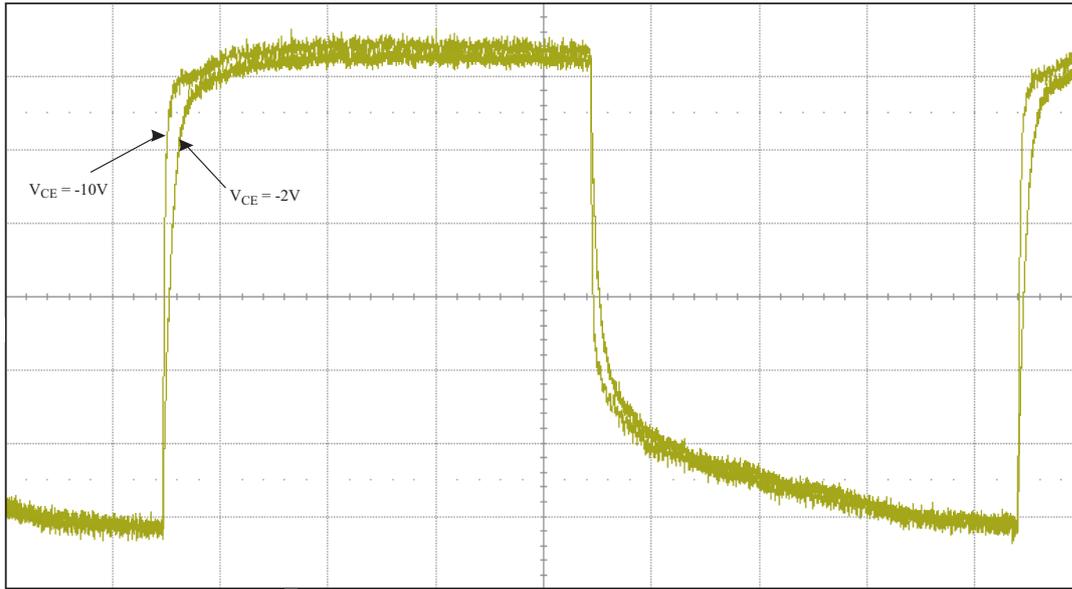
$V_{CE} = -10V$

$V_{CE} = -2V$

Figure 10: *Step response of the $40 \times 40\ \mu m^2\ PT_{EDGE}S_B$ phototransistor. Operating point conditions: $P_{opt} = -19\ dBm$ @ $675\ nm$, $V_{CE} = -2\ V$ and $V_{CE} = -10\ V$. (Axis-properties: x: 200 ns/dev, y: 200 μV/dev).*

5   Conclusion

In this work we present four kinds of speed optimized bipolar pnp phototransistors built in a standard 180 nm CMOS process without any process modifications. The aim of this work was to design fast devices for deep penetrating light. The increase of the devices' bandwidth was done by reducing the emitter size as well as the base size of the device. The phototransistors were implemented in sizes of $40 \times 40\ \mu m^2$ and $100 \times 100\ \mu m^2$. As starting material a wafer was used with a 15 µm thick low doped p$^-$ epi layer grown on top of the p substrate. By means of this low doped epi layer a thick space-charge region is formed between base and collector which leads to a fast separation of deep generated charges caused by deep penetrating light. The thick space-charge region and thus fast separation of the generated charges are important for achieving high bandwidths. For a further speed optimization the phototransistors were implemented with small emitter areas to reduce the base-emitter capacitance. However, due to the small emitter areas the phototransistors achieve relatively small responsivity values. Nevertheless, the

presented phototransistors achieve for 850 nm dynamic responsivities which are by a factor of more than 6 larger than the presented responsivities for the 65 nm pnp phototransistor described in [3]. Furthermore, the presented phototransistors achieve bandwidths up to 60 MHz for 410 nm, up to 92 MHz for 675 nm and up to 50 MHz for 850 nm. When comparing the bandwidth results for 850 nm with the results of the phototransistor presented in [3], the bandwidth increase is more than a factor of 330. Alternatively compared to the fastest own results presented in [14] the bandwidth increase is still a factor of more than 3 at 850 nm. A globally optimized phototransistor cannot be found, since its properties and its realisation depend strongly on the demands on the application field. A trade-off between responsivity and bandwidth exists and thus each phototransistor can only be the best solution for a narrow field of application. Furthermore, the phototransistors are hard to be compared meaningfully with other devices (even other phototransistors) due to their strongly non-linear behaviour. The nonlinearity leads to a strong dependence on different factors like collector-emitter voltage, wavelength, size of the device, optical light power, additional base currents, etc. Unfortunately many publications on phototransistors are lacking one or more of these values, which gives them limited comparability. However, in Tab. 6 we have tried to give a comparison of the fastest presented device together with other (Bi)CMOS phototransistors from literature. Due to the presented results these phototransistors are well suited for cheap high speed optical CMOS applications, where a photosensitive device with an inherent current amplification is needed for weak light detection. Possible applications are fast opto-coupler, optical data receiver, etc.

Acknowledgements

Table 6: *Comparison of CMOS and BiCMOS phototransistors.*

Refs.	Techno -logy	Device type	Dimension (μm^2)	V_{CE} (V)	Wavelength (nm)	P_{opt} (dBm)	Responsivity (A/W)	Rise time (ns)	f_{-3dB} (MHz)	RBW (A/W∗MHz)
[3]	65 nm CMOS	NPN	60×60	1.3	850	×	0.34	×	0.15	0.05
[14]	0.6 µm CMOS	PNP	100×100	−10	850	−10	1.62	25	14[a]	25.2
[15]	0.35 µm CMOS	PNP	35×35	×	×	×	×	×	< 1	×
[16]	×	NPN	700×700	5	420	×	0.25	×	×	×
[18]	0.8 µm BiCMOS	NPN	53×53	×	638	×	×	56	7.8	×
[20]	0.8 µm, 1.2 µm, 2.0 µm CMOS	PNP	60×60	×	660	×	×	3100	×	×
This work	0.18 µm CMOS	PNP	40×40	−10	410 675 850	−12.7 −19.2 −15.8	0.51 2.18 1.28	5 12 7	60.3[a] 92.0[a] 50.0[a]	30.8 200.1 64.0

[a] Fastest device.

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics.* Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] E. Fullin, G. Voirin, M. Chevroulet, A. Lagos, and J.-M. Moret, "CMOS-Based Technology For Integrated Optoelectronics: A Modular Approach," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 527–530, 1994.

[3] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[4] R. Swoboda and H. Zimmermann, "11Gb/s Monolithically Integrated Silicon Optical Receiver for 850 nm Wavelength," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 904–911, 2006.

[5] A. Nemecek, K. Oberhauser, and H. Zimmermann, "Correlating PIN-Photodetector with Novel Difference-Integrator Concept for Range-Finding

Applications," in *IEEE European Solid-State Circuits Conference (ESS-CIRC)*, pp. 491–494, 2005.

[6] M. Davidovic, G. Zach, K. Schneider-Hornstein, and H. Zimmermann, "Range Finding Sensor in 90 nm CMOS with Bridge Correlator Based Background Light Suppression," in *IEEE European Solid-State Circuits Conference (ES-SCIRC)*, pp. 298–301, 2010.

[7] G. Zach and H. Zimmermann, "A 2×32 Range-Finding Sensor Array with Pixel-Inherent Suppression of Ambient Light up to 120 klx," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 352–353,353a, 2009.

[8] G. Zach, M. Davidovic, and H. Zimmermann, "Extraneous-Light Resistant Multipixel Range Sensor Based on a Low-Power Correlating Pixel-Circuit," in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 236–239, 2009.

[9] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, pp. 1956–1976, 1996.

[10] M. Gersbach, J. Richardson, E. Mazaleyrat, S. Hardillier, C. Niclass, R. Henderson, L. Grant, and E. Charbon, "A low-noise single-photon detector implemented in a 130 nm CMOS imaging process," *Solid-State Electronics*, vol. 53, no. 7, pp. 803–808, 2009.

[11] M. Karimi, M. Gersbach, and E. Charbon, "A New Single-Photon Avalanche Diode in 90 nm Standard CMOS Technology," *SPIE - The International Society for Optical Engineering*, vol. 7780, no. 77801F, 2010.

[12] J. Richardson, L. Grant, E. Webster, and R. Henderson, "A 2 µm Diameter, 9 Hz Dark Count, Single Photon Avalanche Diode in 130 nm CMOS Technology," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 257–260, 2010.

[13] L. Pancheri and D. Stoppa, "Low-noise Single Photon Avalanche Diodes in 0.15 µm CMOS Technology," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 179–182, 2011.

[14] P. Kostov, K. Schneider-Hornstein, and H. Zimmermann, "Phototransistors for CMOS Optoelectronic Integrated Circuits," *Sensors and Actuators A: Physical*, vol. 172, no. 1, pp. 140–147, 2011.

[15] A. Hu and V. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[16] A. Tibuzzi, G.-F. D. Betta, C. Piemonte, C. D. Natale, A. D'Amico, and G. Soncini, "High gain bipolar junction phototransistors with finger-shaped emitter for improved optical gas sensing in the blue spectral region," *Sensors and Actuators A: Physical*, vol. 136, no. 2, pp. 588–596, 2007.

[17] A. Tibuzzi, G.-F. Dalla Betta, F. Ficorella, G. Soncini, C. Di Natale, and A. D'Amico, "Finger emitter/base bipolar junction phototransistors for optical gas sensing in the blue spectral region," in *IEEE Sensors Conference*, vol. 3, pp. 1581–1584, 2004.

[18] K. Kieschnick, H. Zimmermann, and P. Seegebrecht, "Silicon-based optical receivers in BiCMOS technology for advanced optoelectronic integrated circuits," *Materials Science in Semiconductor Processing*, vol. 3, no. 5-6, pp. 395–398, 2000.

[19] P. Kostov, W. Gaberl, and H. Zimmermann, "High-Speed PNP PIN Phototransistors in a 0.18 µm CMOS Process," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 187–190, 2011.

[20] P. Kostov, W. Gaberl, A. Polzer, and H. Zimmermann, "CMOS PIN Phototransistors for High-Speed Photosensitive Applications," *Procedia Engineering*, vol. 25, no. 0, pp. 1397–1400, 2011.

[21] R. Sandage and J. Connelly, "A Fingerprint Opto-Detector Using Lateral Bipolar Phototransistors in a Standard CMOS Process," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 171–174, 1995.

[22] W. Zhang, M. Chan, and P. Ko, "A Novel High-Gain CMOS Image Sensor Using Floating N-Well/Gate Tied PMOSFET," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1023–1025, 1998.

[23] G. Winstel and C. Weyrich, *Optoelektronik II.* Berlin/Heidelberg, Germany: Springer-Verlag, 1986.

[24] S. Sze and K. Ng, *Physics of Semiconductor Devices.* New York, USA: John Wiley & Sons, Inc., third ed., 2006.

[25] G. Reider, *Photonik.* Wien, Austria: Springer-Verlag, second ed., 1997.

Publication C

Bandwidth and Gain Enhanced PNP Phototransistors for VIS and NIR Light in 180 nm CMOS

Abstract

Two phototransistor concepts with a size of $40 \times 40\,\mu m^2$ are presented. These devices were implemented in a 850 nm standard CMOS process without process modifications. The use of a special starting material with a low doped p^- epitaxial layer on top of the high doped p^+ substrate opens the possibility for achieving high bandwidths and responsivities even for deep penetrating light. Optical characterization of the devices was done at 410 nm, 675 nm and 850 nm. Bandwidths up to 67 MHz and responsivities up to 12.35 A/W were achieved. These devices are well suited for integrated optoelectronic circuits (OEICs).

Keywords: BJT, CMOS Phototransistors, Light Detector, NIR, Silicon Photode-

tector

1   Introduction

The development of VCSELs at 850 nm has opened the possibility for many applications to use this wavelength for optical sensors with nonvisible light. Due to the used wavelength, silicon is suitable as detector material. In standard silicon processes different kinds of photodetectors can be realized since silicon is sensitive for optical radiation in the range from 300 nm to 1100 nm. Possible photodetectors are photodiodes, phototransistors, avalanche photodiodes and so on. Light in the mentioned wavelength range penetrates in the silicon photodetector and is absorbed in it. The penetration depth and absorption coefficient of the light is wavelength dependent since photons have different energies at different wavelengths. For example, light with a short wavelength (e.g. 430 nm) has a higher energy than light with a long wavelength (e.g. 850 nm). This fact leads to photon absorption closer to the surface of the silicon for short wavelength light and an absorption deep in the substrate for long wavelength light. The $1/e$ penetration depth at 430 nm (blue light) is about 0.2 µm and at 850 nm (near infrared light) about 16.6 µm [1]. A wavelength dependent distribution of the drift and diffusion part of the total photocurrent is caused thereby by the penetrating photons. This fact has a strong impact on the bandwidth and the responsivity of a photodetector.

Photodiodes are the most common photodetectors. A photodiode can be formed by combining a p and an n doped silicon area. The resulting structure leads to a space-charge region (SCR) in the border area between p and n layer. In the SCR generated carriers will be separated and will contribute to the photocurrent of the photodiode if an external bias voltage is applied. For increasing the bandwidth and responsivity (especially for deep penetrating light) a thick low doped intrinsic layer is placed between the anode and the cathode of the photodiode. The resulting device is called a pin photodiode. They have therefore a thicker SCR compared to common pn photodiodes This is advantageous for the collection of deep penetrating light, since the recombination probability of the generated electron-hole pairs outside the SCR is decreased. In [2] lateral and vertical pin photodiodes are

presented. The presented photodiodes achieve responsivities up to 0.15 A/W and bandwidths up to 3.1 GHz while biased at 15.5 V. Phototransistors and avalanche photodiodes have an inherent amplification and therefore a higher responsivity compared to photodiodes. Avalanche photodiodes need for their amplification a high voltage which is not suitable in integrated circuits. Compared to avalanche photodiodes, phototransistors have an acceptable current amplification at a moderate bias voltage. The most common implementation is as vertical or lateral bipolar junction transistor (BJT) [3–6]. Ref. [3] reports on a phototransistor with a bandwidth of a few hundred kHz. Photodiodes and phototransistors in a 65 nm CMOS technology with responsivities up to 0.34 A/W and bandwidths up to 150 kHz are presented in [4]. In [5, 6] pnp phototransistors built in a 0.6 μm CMOS technology with bandwidths up to 8.8 MHz and a corresponding responsivity of 5.2 A/W at 675 nm are presented. This is equivalent to a Responsivity-Bandwidth Product of 45.8 MHz×A/W.

2 Working Principle

A vertical pnp phototransistors is formed by starting with the p-substrate which forms the collector area. Afterwards an n-well (base) and a p-source/drain contact area (emitter) are implemented in the collector and base region, respectively. Since the collector is formed by the substrate the device can be used only in an emitter-follower configuration. The phototransistor can be described as a pn-photodiode which is formed by the base-collector (BC) junction with an inherent pnp BJT for amplification. In this assumption the photodiode sinks the base current for the BJT. The base current corresponds to the photocurrent, which is generated in the BC junction by deep penetrating light. The generated charges are separated by the electric field and attracted by the opposite charged pole. In case of the pnp phototransistor, electrons are attracted towards the base and holes towards the collector, which leads to an accumulation of electrons in the base and to a reduction of the base potential. If the base potential is sufficiently negative so that the forward bias voltage of the base-emitter (BE) diode is reached, a process starts where the emitter injects holes through the base towards the collector. This is the transistor effect and causes the amplification of the base (photo) current.

The current gain β in the phototransistor is [7]:

$$\beta = \frac{I_C}{I_{PH}} = \frac{D_p L_n N_A}{D_n W_B N_D} + 1.$$ (1)

In this equation I_C is the collector current, I_{PH} the photocurrent, D_p and D_n are the diffusion coefficients of holes and electrons in the base, respecttively, W_B is the effective base width, L_n is the diffusion length of electrons in the emitter and N_D and N_A are the donor and acceptor densities in the base and emitter. The effective base width W_B is the area between the boundaries of the BC and the BE SCR. According to (1) a thin W_B together with a low doped base and a high doped emitter is necessary for a high current gain.

Another important parameter of a phototransistor is its $-3\,\text{dB}$ bandwidth ω_B:

$$\frac{1}{\omega_B} = \beta \left(\frac{C_{BE} + C_{BC}}{g_m} + \tau_B + R_L C_{BC} \right).$$ (2)

Here C_{BE} and C_{BC} are the SCR junction capacitances, g_m is the transconductance, τ_B is the base transit time of the minority carriers and R_L is the load resistance [8]. A deeper and more detailed explanation of common CMOS phototransistors can be found in [1, 7, 8].

3   Implemented Devices

We present in this work two $40 \times 40\,\text{µm}^2$ pnp pin phototransistors. The phototransistors were fabricated in a standard $180\,\text{nm}$ CMOS process without process modifications. For achieving high bandwidths, a low doped p^- epitaxial layer was grown on top of the p^+ substrate between base and collector. This layer leads to a thick BC-SCR and thus to a strongly reduced C_{BC}, which increases the $-3\,\text{dB}$ bandwidth according to (2). A further increase of the bandwidth was introduced by implementing the base as $500\,\text{nm}$ wide n-well stripes with $500\,\text{nm}$ gaps between them (see Fig. 1). Due to the thermal budget in the process these stripes will diffuse into each other and will form one more or less homogeneous n-well base area with the half doping concentration compared to a homogeneous n-well implant.
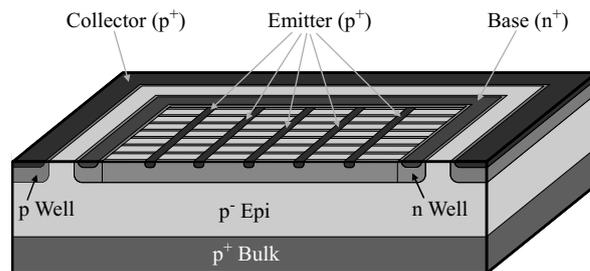
Figure 1: *3D view and cross-section of the $Stripe_E$ phototransistor.*

The reduction of the base doping concentration will cause a spreading of both SCRs into the base and thus to a reduction of the effective base width. A thinner effective base width will cause on one hand an increase of the current gain β (see (1)) and on the other hand a decrease of the base transit time τ_B. The latter will lead to a higher bandwidth (see (2)). For a further increase of the bandwidth the phototransistors were built with small emitter areas. Due to the small emitter area only a small BE-SCR and thus a small C_{BE} are formed, which has a positive effect on the bandwidth. However, a small emitter is a drawback for the responsivity of the phototransistor. Since the emitter is quite small compared to the whole photosensitive area, all photogenerated charges which are not generated directly under the emitter area will have to travel longer distances through the base to reach the BE-SCR. This increases the probability for recombination in the base and leads to a reduced responsivity. One phototransistor ("$Center_E$") was implemented with a small $0.74 \times 0.74 \, \mu m^2$ p^+ emitter area placed in the center of the phototransistor for achieving high bandwidths. A second phototransistor ("$Stripe_E$") was implemented with five emitter stripes for achieving a higher responsivity. Each stripe is $320 \, nm$ wide and has a gap of $7.7 \, \mu m$ to the next one (Fig. 1).

4   Simulation Results

Several electrical field simulations were done to investigate variations between different collector-emitter voltages (V_{CE}). The simulations were done for dark light conditions. In Fig. 2 one electrical field simulation for the $Stripe_E$ phototransistor at $V_{CE} = -10 \, V$ is depicted. In the figure the value of the electrical field in the
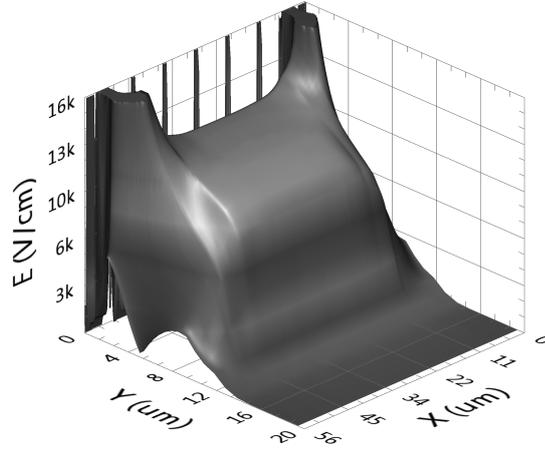
Figure 2: *Simulated electric field strength for the Stripe$_E$ phototransistor at*
$V_{CE} = -10$ V.

BC-SCR as well as the thickness of the BC-SCR are noticeable. Furthermore at
$Y = 0$ the contacts of the collector and the five emitter stripes are visible. The
scale was limited to $16\,\text{kV/cm}$ for a better depiction of the relevant field magnitude
in the BC-SCR.

5   Measurement Results

The phototransistors were characterized by measuring the dynamic responsivities,
$-3\,\text{dB}$ bandwidths and rise times at three different wavelengths: $410\,\text{nm}$, $675\,\text{nm}$
and $850\,\text{nm}$. Thereby, the base was left floating and V_{CE} was set to $-2\,\text{V}$ and
$-10\,\text{V}$. The main measuring equipment consists of a vector network analyzer, an
oscilloscope with $50\,\Omega$ input resistance and three laser sources. The optical light
power was adjusted for each laser source to compensate for the different photon
energy and penetration depth. Otherwise a lack of comparability would arise if all
laser sources would have the same optical light power. Thus, the light power was
set to $-12.7\,\text{dBm}$ at $410\,\text{nm}$, $-19.2\,\text{dBm}$ at $675\,\text{nm}$ and $-15.8\,\text{dBm}$ at $850\,\text{nm}$.

Tab. 1 shows the measured dynamic responsivities for both phototransistors. The
highest value of $12.35\,\text{A/W}$ is achieved by the *Stripe$_E$* phototransistor at $675\,\text{nm}$
and $V_{CE} = -10\,\text{V}$. This is caused by an optimal penetration depth at $675\,\text{nm}$,

where the main part of charges is generated directly inside the BC SCR. Thereby the thickness of the BC-SCR optimally suites the penetration depth. Furthermore, also the probability for recombination in the base is smaller compared to the $Center_E$ phototransistor due to more emitter area. However, the larger emitter area increases C_{BE}, which has together with the presence of the base transit time τ_B an effect on the bandwidth as depicted in Tab. 2 and Fig. 3. Furthermore, these parameters also increase the rise times (Tab. 3). Thus, the small C_{BE} of the $Center_E$ phototransistor leads to a $-3\,\text{dB}$ bandwidth of $67\,\text{MHz}$ at $675\,\text{nm}$ and

Table 1: *Responsivities in A/W for both phototransistors at 410 nm, 675 nm, 850 nm and $V_{CE} = -2$ V and -10 V.*

	$V_{CE} = -2\,\text{V}$		$V_{CE} = -10\,\text{V}$	
	$Center_E$	$Stripe_E$	$Center_E$	$Stripe_E$
410 nm	0.58	3.20	0.61	4.13
675 nm	1.74	10.65	1.81	12.35
850 nm	1.34	6.74	1.36	7.86

Table 2: *Bandwidths in MHz for both phototransistors at 410 nm, 675 nm, 850 nm and $V_{CE} = -2$ V and -10 V.*

	$V_{CE} = -2\,\text{V}$		$V_{CE} = -10\,\text{V}$	
	$Center_E$	$Stripe_E$	$Center_E$	$Stripe_E$
410 nm	10.7	4.1	57.5	13.5
675 nm	9.6	3.7	67.0	19.3
850 nm	12.8	8.9	50.0	16.1

Table 3: *Rise times in ns for both phototransistors at 410 nm, 675 nm, 850 nm and $V_{CE} = -2$ V and -10 V.*

	$V_{CE} = -2\,\text{V}$		$V_{CE} = -10\,\text{V}$	
	$Center_E$	$Stripe_E$	$Center_E$	$Stripe_E$
410 nm	32	85	6	26
675 nm	36	95	5	18
850 nm	27	39	7	22
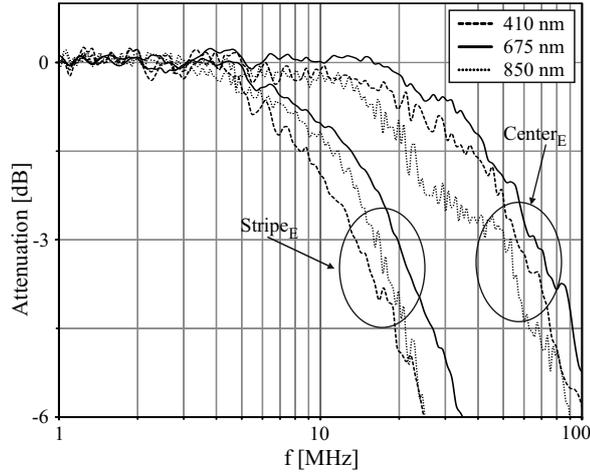
Figure 3: *Frequency response of both phototransistors at 410 nm, 675 nm, 850 nm and $V_{CE} = -10$ V.*

$V_{CE} = -10\,\text{V}$. For higher V_{CE} the bandwidth will be increased due to a reduction of C_{BC}, C_{BE} and τ_B. However, the highest Responsivity-Bandwidth Product of $238.4\,\text{MHz}\times\text{A/W}$ is achieved by the $Stripe_E$ phototransistor.

6   Conclusions

We present two pnp pin phototransistors with a thick low doped p⁻ epitaxial layer between base and p⁺ collector. Together with a lower doped base, the phototransistors achieve high $-3\,\text{dB}$ bandwidths. For a further increase of the bandwidth one phototransistor was implemented with a small emitter. Thus bandwidths up to $67\,\text{MHz}$ were achieved. However, the small emitter causes a small responsivity. For achieving a higher responsivity a second phototransistor was implemented with five emitter stripes. This device achieves responsivities up to $12.35\,\text{A/W}$. Its maximum achieved bandwidth was $19.3\,\text{MHz}$. Both devices achieve responsivities which are at least more than 12 times larger compared to the pin photodiode presented in [2] and more than five times larger compared to the presented pnp phototransistor in [4]. Furthermore also the $-3\,\text{dB}$ bandwidth is several hundred times larger than the results presented in [4]. Compared to our own results presented in [5, 6] we could increase the Responsivity-Bandwidth Product at $675\,\text{nm}$

with a factor of more than five. Due to the results we can say that each presented phototransistor fits in applications where photosensitive devices with on one hand high bandwidth or on the other hand a higher responsivity compared to a common pn or pin photodiode are required. Since the devices are based on a standard CMOS process, they are well suited for integration together with a readout circuitry to an optoelectronic circuit (OEIC). Possible applications could be optical sensors, fast opto-couplers and so on.

Acknowledgements

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics*. Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] B. Ciftcioglu, L. Zhang, J. Zhang, J. Marciante, J. Zuegel, R. Sobolewski, and H. Wu, "Integrated Silicon PIN Photodiodes Using Deep N-Well in a Standard 0.18 μm CMOS Technology," *Journal of Lightwave Technology*, vol. 27, no. 15, pp. 3303–3313, 2009.

[3] A. Hu and V. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[4] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[5] P. Kostov, W. Gaberl, and H. Zimmermann, "Visible and NIR integrated Phototransistors in CMOS technology," *Solid-State Electronics*, vol. 65-66, pp. 211–218, 2011.

[6] P. Kostov, K. Schneider-Hornstein, and H. Zimmermann, "Phototransistors for CMOS Optoelectronic Integrated Circuits," *Sensors and Actuators A: Physical*, vol. 172, no. 1, pp. 140–147, 2011.

[7] G. Winstel and C. Weyrich, *Optoelektronik II.* Berlin/Heidelberg, Germany: Springer-Verlag, 1986.

[8] D. Decoster and J. Harari, *Optoelectronic Sensors.* Hoboken, London: Wiley-ISTE, 2009.

Publication D

Integrated 180 nm CMOS Phototransistors with an Optimized Responivity-Bandwidth-Product

Authored by P. Kostov, W.Gaberl, M. Hofbauer and H. Zimmermann

Abstract

A phototransistor with an optimized responsivity-bandwidth-product is presented in this paper. The device has a size of $40 \times 40\,\mu\text{m}^2$ and is implemented in a standard 180 nm CMOS process. By means of a thick low doped p-epitaxial layer starting material (collector), a base formed as striped n-wells and an optimized design of the emitter high responsivity-bandwidth-product values up to $171.1\,\text{A/W}*\text{MHz}$ are achieved.

Keywords–Phototransistor, CMOS, Light Detector

1 Introduction

The most used photodetectors are implemented as PN or PIN photodiodes (PDs), avalanche photodiodes (APDs) or as phototransistors (PTs). Fabricated in silicon, these devices can detect light in the range from 300 to 1100 nm. This range is limited by the physical characteristics of silicon. Due to varying photon energies at different wavelengths a wavelength dependent $1/e$ penetration depth occurs: e.g. 0.2 µm at 430 nm or 16.6 µm at 850 nm [1]. However, each device type is different and has certain advantages and disadvantages. PIN PDs can be used for detection of light modulated with high frequencies up to several GHz as shown in [2]. This is possible due to a thick low doped epitaxial layer between anode and cathode, which results in a thick space-charge region (SCR) and thus to a larger drift current portion of the resulting photogenerated current. The drawback of a PD is the relatively small responsivity. Ref. [2] reports on PIN PD achieving 3.1 GHz with 0.15 A/W @ 15.5 V. However, there are applications which require a high responsivity and a smaller bandwidth. In this case APDs and PTs are more appropriate as they have an inherent current amplification mechanism. The drawback of APDs is their need of a quite high bias voltage compared to PTs. A common bipolar PT can be described as a PD (formed by the base-collector (BC) junction) and an inherent BJT for the current amplification. The PT's responsivity and bandwidth is strongly dependent on the design of the PT. The possibility to vary the design of emitter, base and collector opens up many optimization options for different characteristics of the device. By modification of the design it is possible to control several important parameters: the base-emitter (BE) capacitance C_{BE}, the base-collector capacitance C_{BC}, the base doping concentration N_B, the effective base-width W_B (width between the borders of BE- and BC-SCR inside the base) and the base transit time τ_B. These parameters are primarily responsible for the current gain β and the -3 dB bandwidth ω_{-3dB} [3]:

$$\beta \propto \frac{N_E}{W_B N_B}, \tag{1}$$

$$\frac{1}{\omega_{-3dB}} \propto \beta \left(\tau_B + \frac{C_{BE} + C_{BC}}{g_m} \right). \tag{2}$$

In (1) N_E represents the emitter doping concentration and g_m the transconductance.

The implementation of a vertical pnp PT starts with the p substrate, which forms the collector. An n-well implant in the collector and another p$^+$ drain/source implant in the n-well form the base and emitter, respectively. When irradiated, a high amount of photogenerated electrons will reach the base and cause a reduction of the base potential. If the base-emitter voltage is sufficiently high the emitter will start injecting holes through the base towards the collector (transistor effect).

In [4] a PT with $\omega_{-3dB} < 1\,\text{MHz}$ is reported. Ref. [5] reports on a PT with a responsivity-bandwidth-product (RBP) of $0.051\,\text{A/W}*\text{MHz}$ ($0.34\,\text{A/W}$, $150\,\text{kHz}$). PTs with RBPs up to $45.8\,\text{A/W}*\text{MHz}$ ($5.2\,\text{A/W}$, $8.8\,\text{MHz}$) are presented in [6].

2 Device Structure

A 3D view of the presented PT is depicted in Fig. 1. The PT has a size of $40 \times 40\,\mu\text{m}^2$ and is built in a standard $180\,\text{nm}$ CMOS process using a special starting wafer. The wafer consists of a high doped p$^+$ substrate with a $\sim 15\,\mu\text{m}$ thick low doped p-epitaxial layer on top of it. By means of this epi layer a thick BC-SCR is formed. This has a positive effect on ω_{-3dB} since C_{BC} is reduced. A further increase of ω_{-3dB} was achieved by reducing the base transit time τ_B. This was done by implementing the base as $1\,\mu\text{m}$ wide n-well stripes with $0.5\,\mu\text{m}$ wide gaps between them. Due to the thermal budget these stripes diffuse into each other and lead to a reduction of the effective N_B, which results in a smaller W_B. At first sight a tiny emitter seems prosperous. By implementing a small emitter C_{BE} would also get small, leading to an increase of ω_{-3dB}. However, in this case the responsivity will be strongly decreased due to strong recombination in the base. If, on the other hand, the emitter is large, C_{BE} will also be large too, leading to a small ω_{-3dB} and a high responsivity. An optimized RBP was found by forming the emitter with five stripes. Each stripe has a width of $0.32\,\mu\text{m}$ and a gap of $7.7\,\mu\text{m}$ to the next one.
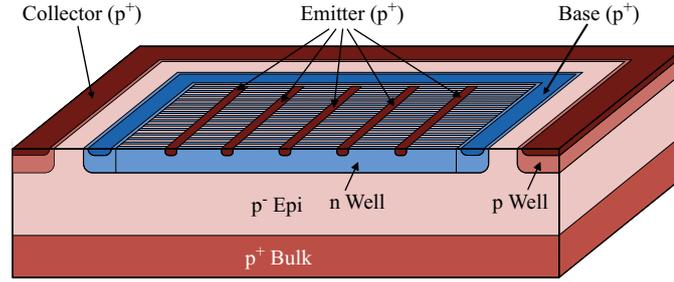
Figure 1: *3D view and cross-section of the phototransistor.*

3 Results

Electrical field simulations were done to characterize the device at different V_{CE}s (collector-emitter voltages). Fig. 2 depicts the electric field at $V_{CE} = -10\,\text{V}$. For a better readability the field strength was limited to $17\,\text{kV cm}^{-1}$. The thickness of the BC-SCR is clearly visible.

Device characterizations were done by optical measurements at 410, 675 and 850 nm, respectively. Responsivities and ω_{-3dB} were measured at floating base conditions and at sinking a constant base current of $10\,\mu\text{A}$. Due to different photon energies the optical power was regulated to get the same collector current for the three investigated wavelengths. The optical power was set to: $-12.7\,\text{dBm}$ @ 410 nm, $-19.2\,\text{dBm}$ @ 675 nm and $-15.8\,\text{dBm}$ @ 850 nm. In Tab. I the PT's characteristics together with the RBP are presented. By means of a small τ_B and a small C_{BC} (resulting from the striped base and the low doped epi layer in the collector) and an optimal design of the emitter high RBPs were achieved. The maximum achieved RBP is $171.1\,\text{A/W}*\text{MHz}$ (9.4 A/W, 18.2 MHz). Fig. 3 presents the frequency response of the PT.

4 Conclusion

A vertical pnp PT with an optimized RBP is presented. The device was fabricated in an 180 nm standard CMOS process. A starting wafer with a low doped p-epitaxial layer on top of the p$^+$ substrate was used. This structure leads to a thick
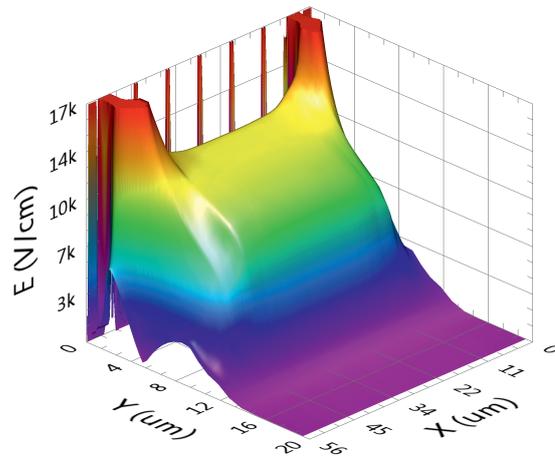
Figure 2: *Simulated electric field strength at $V_{CE} = -10\ V$.*
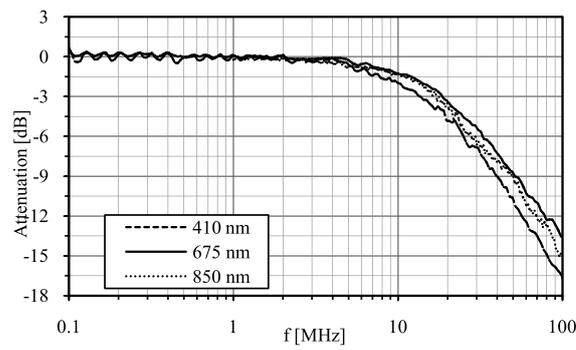
Figure 3: *Frequency response at $V_{CE} = -10\ V$.*

Table I: *Characteristics of the phototransistor at $V_{CE} = -10\ V$.*
Upper Table: $I_B = 0\ A$; Lower Table: $I_B = -10\ \mu A$.

	Rise Time [ns]	Responsivity [A/W]	Bandwidth [MHz]	R*BW [A/W*MHz]
410 nm	26	2.2	13.8	30.4
675 nm	20	9.4	18.2	171.1
850 nm	23	6.3	15.1	95.1
410 nm	17	1.7	21.4	36.4
675 nm	16	6.8	21.4	145.5
850 nm	18	5.6	20.4	114.2

BC-SCR and furthermore to a small C_{BC}, which increases the $-3\,\mathrm{dB}$ bandwidth of the device. A further bandwidth increase was introduced by forming the base as n-well stripes to reduce the effective base doping concentration. Together with an optimized design of the emitter (implemented as stripes) high RBPs were achieved. The maximum achieved RBP of $171.1\,\mathrm{A/W}*\mathrm{MHz}$ ($9.4\,\mathrm{A/W}$, $18.2\,\mathrm{MHz}$) is several hundred times larger than that for the PTs presented in [5] and more than a factor of 3 better than the PTs presented in [6]. The presented PT is well suited for integration into an optoelectronic integrated circuit (OEIC). Possible applications could be opto-couplers, optical detectors, light barriers and so on.

Acknowledgements

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics.* Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] B. Ciftcioglu, L. Zhang, J. Zhang, J. Marciante, J. Zuegel, R. Sobolewski, and H. Wu, "Integrated Silicon PIN Photodiodes Using Deep N-Well in a Standard $0.18\,\mu\mathrm{m}$ CMOS Technology," *Journal of Lightwave Technology*, vol. 27, no. 15, pp. 3303–3313, 2009.

[3] S. Sze and K. Ng, *Physics of Semiconductor Devices.* New York, USA: John Wiley & Sons, Inc., third ed., 2006.

[4] A. Hu and V. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[5] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[6] P. Kostov, K. Schneider-Hornstein, and H. Zimmermann, "Phototransistors for CMOS Optoelectronic Integrated Circuits," *Sensors and Actuators A: Physical*, vol. 172, no. 1, pp. 140–147, 2011.

Publication E

Low Frequency Noise in CMOS PNP PIN Phototransistors

Authored by P. Kostov, W.Gaberl, M. Hofbauer and H. Zimmermann

Abstract

Low frequency noise on six different types of CMOS PNP PIN phototransistors was investigated and is presented in this paper. The output noise spectral density is evaluated by a noise model for the investigated phototransistors. The current gain β and the most dominant shot noise terms including their values of each phototransistor are extracted. The presented phototransistors show a good noise performance.

Keywords–integrated; phototransistor; CMOS; bipolar; shot noise; base resistor; low frequency noise; optoelectronic.

1   Introduction

Photodetectors are used for the detection of optical irradiation. The fact that this irradiation is quite weak in most applications leads to the importance of the investigation and characterization of the noise behavior of such sensors. The noise of the sensor is the limiting factor for the possibility to detect the signal. A low noise floor of the sensor leads to a smaller detectable signal power. Typical noise sources in optoelectronic devices are 1/f noise, thermal noise and shot noise. Generation-recombination noise as well as burst noise are negligible in nowadays CMOS technologies due to a clean production with almost no contaminations.

2   Theory

Typical photodetectors are PIN photodiodes, avalanche photodiodes (APD) and phototransistors. Each detector has a specific noise behavior. In a photodiode the output current noise spectral density is caused by shot noise parts of the dark current I_D and the photocurrent I_{PH} together with the thermal noise of the load resistor R_L:

$$\frac{\overline{i^2_{oPD}}}{\Delta f} = 2q(I_D + I_{PH}) + \frac{4kT}{R_L} \tag{1}$$

In (1) q is the elementary charge, k the Boltzmann constant and T the temperature.

The shot noise density in an avalanche photodiode is multiplied by the squared multiplication factor of the avalanche photodiode [1]. For an avalanche photodiode there is an additional multiplication factor which is called "excess noise factor" to describe the total output noise of the device. In contrary to the avalanche photodiode, the noise in a phototransistor consists of three terms as shown in (2): $\beta^2 S_{I_B}$, S_{I_C}, $S_{I_{BC}}$. The first term represents the noise sources at the base of the phototransistor which are mainly the shot noise caused by the photocurrent and the base-emitter current together with $1/f^\gamma$ noise from both junctions and the base resistor's thermal noise. The factor γ in the $1/f^\gamma$ noise is a model parameter and has typically values between 0.8 and 1.3. These noise sources are multiplied by

the squared current gain. The second term represents the shot and the $1/\mathrm{f}^\gamma$ noise caused by the collector current. The third term is introduced by the correlation of the base and collector current noise terms. All terms are added up to form the output current noise spectral density of a phototransistor [2, 3]:

$$
\frac{\overline{i_{o_{PT}}^2}}{\Delta f} = \overline{\left(\beta\frac{i_b}{\sqrt{\Delta f}} + \frac{i_c}{\sqrt{\Delta f}}\right)^2} = \underbrace{\beta^2\frac{\overline{i_b^2}}{\Delta f}}_{\beta^2 S_{I_B}} + \underbrace{\frac{\overline{i_c^2}}{\Delta f}}_{S_{I_C}} + \underbrace{2\Re\left\{C\sqrt{\beta^2\frac{\overline{i_b^2}}{\Delta f}\frac{\overline{i_c^2}}{\Delta f}}\right\}}_{S_{I_{BC}}},
\qquad (2)
$$

with

$$
S_{I_B} = \frac{\overline{i_b^2}}{\Delta f} = S_{I_{PH}} + S_{I_{EB}} + S_{I_{r_b}}, \qquad (3)
$$

$$
S_{I_{PH}} = 2qI_{PH} + k_1\frac{I_{PH}}{f^\gamma}, \qquad (4)
$$

$$
S_{I_{EB}} = 2qI_{EB} + k_2\frac{I_{EB}}{f^\gamma}, \qquad (5)
$$

$$
S_{I_{r_b}} = \frac{4kT}{r_b}, \qquad (6)
$$

$$
S_{I_C} = \frac{\overline{i_c^2}}{\Delta f} = 2qI_{CE} + k_3\frac{I_{CE}}{f^\gamma}. \qquad (7)
$$

In (2) the noise of the following load resistor was neglected. Furthermore, this equation is only valid for frequencies lower than the $-3\,\mathrm{dB}$ cutoff frequency of the device. The factor C describes the correlation between the base and the collector noise current. Its value can vary between -1 and $+1$.

The base current noise shown in (3) consists of the current noise parts of the base-collector diode (4) and of the base-emitter diode (5) and the thermal noise of the base resistor r_b (6). Both current noise parts in (4) and (5) consist of the shot noise due to the photocurrent I_{PH} and emitter-base current I_{EB} together with a corresponding junction $1/\mathrm{f}^\gamma$ noise. The shot noise of the collector current I_{CE} and its $1/\mathrm{f}^\gamma$ noise is described in (7). k_1, k_2, and k_3 in (4), (5), and (7) are dimensional

constants.

The $1/f^\gamma$ noise sources are caused by recombination of carriers due to trapping centers at the surface of the space-charge regions [4, 5].

3   Phototransistor Structures, Common Noise Model and Noise Analysis

A. Phototransistor Structures

The noise behavior of six pnp PIN phototransistor layouts has been investigated. These devices were built in a $180\,\mathrm{nm}$ CMOS process and have a thick low doped p-epitaxial layer for achieving a high bandwidth and for increasing the responsivity for deep penetrating light, i.e. near infrared light. Each device differs from the others in the design of layout:

- $50_B\mathrm{Center}_E$: 50% doped base; small center emitter

- $100_B\mathrm{Quad}_E$: full base; four emitters in each quadrant

- $100_B\mathrm{Edge}_E$: full base; small edge emitter

- $S_B\mathrm{Quad}_E$: small base under each emitter; four emitters

- $S_B\mathrm{Edge}_E$: small base under the emitter; edge emitter

- $66_B\mathrm{Stripe}_E$: 66% doped base; emitter stripes

A 3D depiction of the $100_B\mathrm{Quad}_E$ phototransistor is shown in Fig. 1. A more detailed description on the characteristics, especially a detailed layout, of the investigated phototransistors can be found in [6–8].

B. Common Noise Model and Noise Analysis

In Fig. 2 the small signal noise model for the pnp phototransistor is shown. The presented model is valid for an open-base circuit as used in the following setup.
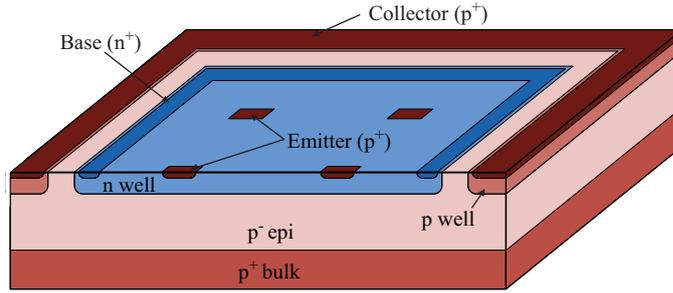
Figure 1: *3D View of the $100_B Quad_E$ phototransistor.*

The representation of the base resistance r_b thermal noise source is done by $S_{I_{r_b}}$, while $S_{I_{PH}}$, $S_{I_{EB}}$, and S_{I_C} stand for the noise current sources. The other resistors r_μ, r_π, and r_{CE} are noiseless model resistors and do not contribute to the output noise. Each of these four noise sources adds a noise part to the output noise current. As shown in (2) and (3) the amplified base noise current S_{I_B} contributes three noise sources: $S_{I_{PH}}$, $S_{I_{EB}}$, and $S_{I_{r_b}}$. The contribution of each noise source to the base noise current source is:

$$S_{I_{B,I_{PH}}} = S_{I_{PH}} \left(\frac{Z_\mu}{Z_\mu + Z_\pi + r_b} \right)^2, \tag{8}$$

$$S_{I_{B,I_{EB}}} = S_{I_{EB}} \left(\frac{Z_\mu + r_b}{Z_\mu + Z_\pi + r_b} \right)^2, \tag{9}$$

$$S_{I_{B,I_{r_b}}} = S_{I_{r_b}} \left(\frac{r_b}{Z_\mu + Z_\pi + r_b} \right)^2, \tag{10}$$

with,

$$Z_\mu = Z_{C_\mu} // r_\mu, \tag{11}$$

$$Z_\pi = Z_{C_\pi} // r_\pi, \tag{12}$$

The low doped p-epitaxial layer between the n-base and the p$^+$ collector leads to a thick base-collector space-charge region and thus to a high GΩ value for r_μ and to value for C_μ in the pF range, respectively. The parallel connection of both elements
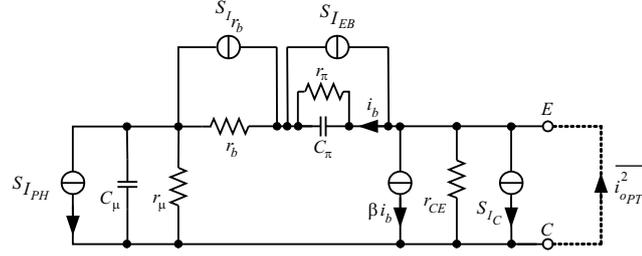
Figure 2: *Small-signal equivalent circuit for the PNP phototransistor including noise sources.*

causes a high value for Z_μ at lower frequencies. Considering the high value for Z_μ in the equations (8)-(10) will lead to a full noise contribution of the shot noise currents $S_{I_{PH}}$ and $S_{I_{EB}}$ and to a negligible thermal noise current contribution $S_{I_{r_b}}$ of the base resistance r_b. However, the photogenerated current I_{PH} leads to disturbance of the charge neutrality in the phototransistor. To maintain the charge neutrality the fluctuations of the photocurrent have to be compensated. For this purpose charges basically are injected from the emitter and carry out the compensation since the base is open. This leads to the conclusion that I_{PH} and I_{EB} and thus also $S_{I_{PH}}$ and $S_{I_{EB}}$ in (4) and (5) have to be equal causing an effective doubling of the base shot noise current:

$$S_{I_B} = S_{I_{PH}} + S_{I_{EB}} = 2S_{I_{PH}}, \tag{13}$$

Furthermore a full correlation between the base and the collector noise current is caused due to the fact that the base-collector junction acts as a current source with a high source resistance Z_μ at the base [9]. This leads to the correlation factor $C = 1$ in (2) for the investigated case.

4   Measurement Setup

The noise measurement setup consists of the phototransistor as device under test, a transimpedance amplifier (TIA) and a spectrum analyzer (SA). The conversion of the photocurrent noise into a voltage noise is done with a low noise LT1124 operational amplifier (OPA) together with a $300\,\mathrm{k\Omega}$ feedback resistor. They act

together as a transimpedance amplifier. A depiction of the measurement setup together with the noise sources is shown in Fig. 3. To guarantee that the power supply noise does not influence the measurement results in the low-frequency range the whole circuit was powered by batteries. The output voltage spectral density $\overline{v_o^2}$ was detected by a HP 4395A spectrum analyzer. $\overline{v_o^2}$ consists of the equivalent input noise sources of the OPA, $\overline{e_n^2}$ and $\overline{i_n^2}$, together with the thermal noise of the feedback resistor and the emitter short circuit noise $\overline{i_{o_{PT}}^2}$ of the investigated phototransistor:

$$\overline{v_o^2} = \left[\overline{i_{o_{PT}}^2} + \overline{i_n^2} + \frac{4kT}{R_f}\right] R_f^2 + \overline{e_n^2}. \tag{14}$$

Fig. 4 shows the simulated equivalent input noise spectral densities of the OPA. The OPA is characterized by a minimum value of $7.29 \times 10^{-18}\,\mathrm{V^2/Hz}$ for $\overline{e_n^2}$ and $9.07 \times 10^{-26}\,\mathrm{A^2/Hz}$ for $\overline{i_n^2}$. In Fig. 5 the measured frequency response of the transimpedance amplifier is shown. A bandwidth of 600 kHz is achieved.

For the measurements the collector potential of each phototransistor was set to $-5\,\mathrm{V}$ and the base was left open. A DC powered light bulb was used as light source. The light intensity was adjusted to meet a defined collector current level in each phototransistor. Measurements were performed at four different collector currents: 100 nA, 500 nA, 1 µA, and 2 µA.
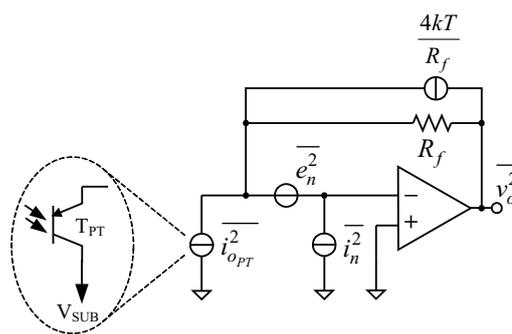

Figure 3: *Noise measurement setup.*
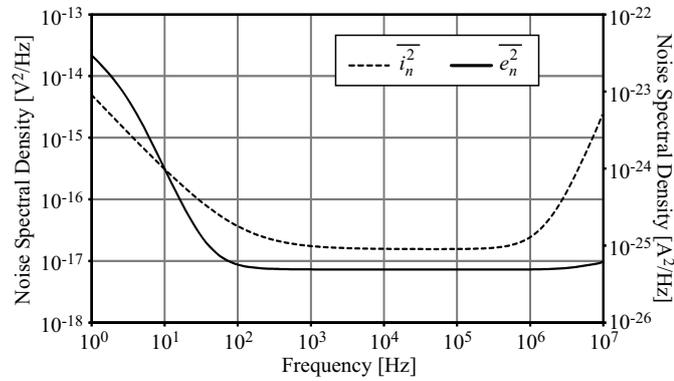
Figure 4: *Simulated input noise current and voltage spectral density of the used operational amplifier.*
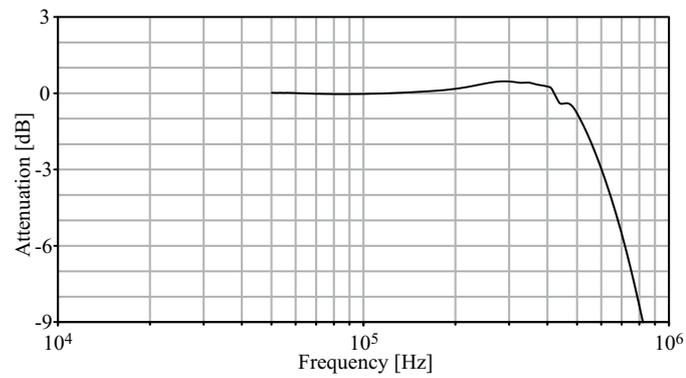
Figure 5: *Measured frequency response of the transimpedance amplifier (low noise OPA with 300 kΩ feedback resistor).*

5 Results

For each presented phototransistor the output current noise spectral density $\overline{i_{o_{PT}}^2}$ was calculated from the measured output voltage noise spectral density $\overline{v_o^2}$ after (14). Fig. 6 shows the output current noise spectral density of the 100_BQuad_E phototransistor for the four different collector currents for frequencies from $10\,\text{Hz}$ to $\sim 700\,\text{kHz}$. The dashed line represents the noise floor of the measurement system. For higher frequencies the measured noise current rolls off due to the bandwidth limitation of the transimpedance amplifier. A low $1/f$ noise corner frequency is noticeable. It increases from $\sim 700\,\text{Hz}$ for $I_C = 100\,\text{nA}$ to $\sim 6\,\text{kHz}$ for $I_C = 2\,\mu\text{A}$.

In Fig. 7 the shot noise part of the output current noise spectral density of each phototransistor extracted from Fig. 5 is presented for different collector currents. Fitting the model presented in (2) to the presented curves leads to the extraction of the current gain β and the current noise densities $\beta^2 S_{I_B}$, S_{I_C}, and $S_{I_{BC}}$ for each phototransistor. Table I presents the extracted results for each phototransistor for $I_C = 2\,\mu\text{A}$. The presented noise figure F_{dB} describes the ratio of the equivalent input noise of each phototransistor compared to the shot noise of a photodiode:

$$F_{dB} = \frac{\overline{i_{o_{PT}}^2}}{\beta^2 \,\overline{i_{o_{PD}}^2}}. \tag{15}$$

Noise figures up to $3.63\,\text{dB}$ were achieved. The best (lowest) noise figure was achieved by the phototransistor with the highest current gain (66_BStripe_E). It is noticeable that the noise figure is almost indirect proportional to the current gain β. Fig. 8 depicts the F_{dB} over the current gain β at $I_C = 2\,\mu\text{A}$.

6 Conclusion

The noise behavior of six $180\,\text{nm}$ CMOS pnp PIN phototransistors was measured and analyzed. Due to the open-base operation a full correlation occurs between the base and collector noise currents which lead to an additional output noise term. On the other side, the open-base operation leads to a negligible thermal noise contribution caused by the base resistor. The current gain together with
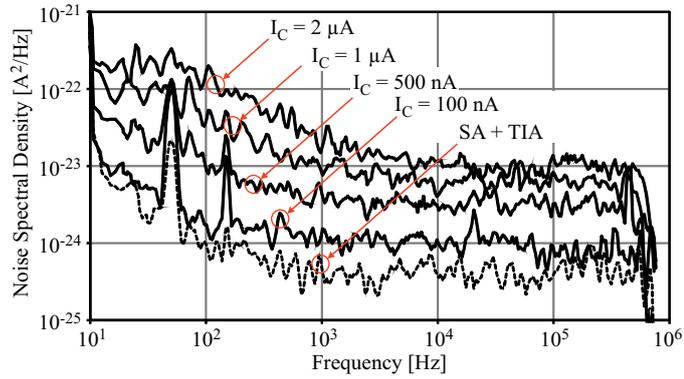
Figure 6: *Output noise current spectral density of the $100_B Quad_E$ phototransistor for different light intensities.*
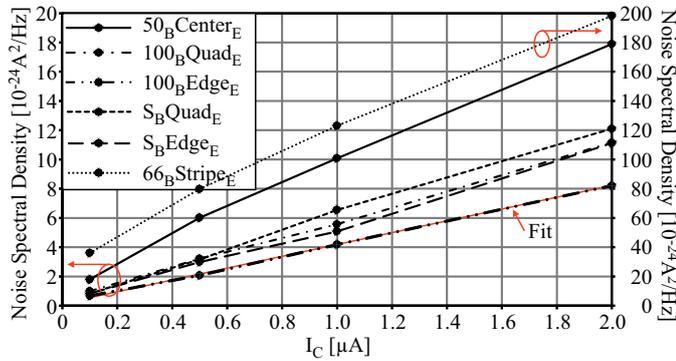
Figure 7: *Shot noise part of the output noise spectral density of the phototransistors for different light intensities i.e. for different output photocurrents.*
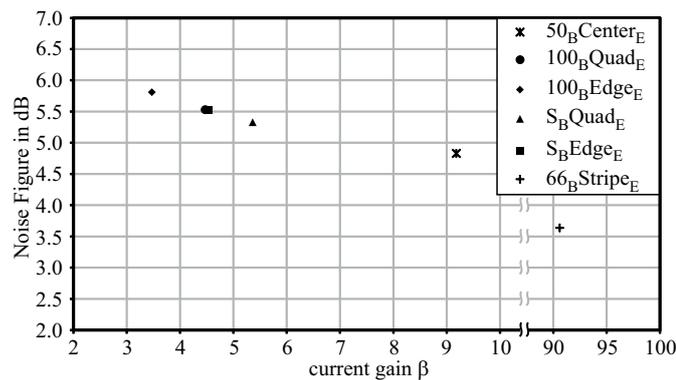
Figure 8: *Noise figure in dB over the extracted current gain β at $I_C = 2\,\mu A$.*

Table I: *Current gain β,*
amplified base current noise density $\beta^2 S_{I_B}$ in $[10^{-24} A^2/Hz]$,
collector current noise density S_{I_C} in $[10^{-24} A^2/Hz]$,
correlation current noise desnity part $S_{I_{BC}}$ in $[10^{-24} A^2/Hz]$,
and noise figure in [dB],
extracted from the output noise for $I_C = 2\,\mu A$.

	β	$\beta^2 S_{I_B}$	S_{I_C}	$S_{I_{BC}}$	F_{dB}
$50_B Center_E$	9.18	11.80	0.64	5.49	4.83
$100_B Quad_E$	4.47	5.73	0.64	3.83	5.53
$100_B Edge_E$	3.47	4.45	0.64	3.38	5.81
$S_B Quad_E$	5.36	6.87	0.64	4.20	5.33
$S_B Edge_E$	4.53	5.81	0.64	3.86	5.52
$66_B Stripe_E$	90.60	116.11	0.64	17.25	3.63

the shot noise densities were extracted from the measured output noise density spectrum for each phototransistor. Furthermore a noise figure for the relationship between the equivalent phototransistor input noise and the photodiode's shot noise is presented. All of the presented devices achieve noise figures better than 5.81 dB. The best one achieves a noise figure of 3.63 dB.

Acknowledgements

References

[1] S. Ouarets, B. Orsal, M. Lahrichi, and M. Achouche, "Optoelectronic 1/f noise of Avalanche Photodiodes (AlInAs/GaInAs/InP) dedicated to Photonic Instrumentation and Telecommunication," in *IEEE International Conference on Noise and Fluctuations (ICNF)*, pp. 313–316, 2011.

[2] F. De La Moneda, E. Chenette, and A. Van Der Ziel, "Noise in Phototransistors," *IEEE Transactions on Electron Devices*, vol. 18, no. 6, pp. 340–346,

1971.

[3] D. Decoster and J. Harari, *Optoelectronic Sensors.* Hoboken, London: Wiley-ISTE, 2009.

[4] A. van der Ziel, X. Zhang, and A. Pawlikiewicz, "Location of 1/f Noise Sources in BJT's and HBJT's-I. Theory," *IEEE Transactions on Electron Devices*, vol. 33, no. 9, pp. 1371–1376, 1986.

[5] T. G. M. Kleinpenning, "Location of Low-Frequency Noise Sources in Submicrometer Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 39, no. 6, pp. 1501–1506, 1992.

[6] P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Integrated 180 nm CMOS Phototransistors with an optimized Responsivity-Bandwidth-Product," in *IEEE Photonics Conference (IPC)*, pp. 314–315, 2012.

[7] P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "PNP PIN bipolar phototransistors for high-speed applications built in a 180 nm CMOS process," *Solid-State Electronics*, vol. 74, no. 0, pp. 49–57, 2012.

[8] P. Kostov, W. Gaberl, and H. Zimmermann, "High-speed bipolar phototransistors in a 180 nm CMOS process," *Optics & Laser Technology*, vol. 46, no. 0, pp. 6–13, 2013.

[9] S. Bruce, L. K. J. Vandamme, and A. Rydberg, "Measurement of Low-Frequency Base and Collector Current Noise and Coherence in SiGe Heterojunction Bipolar Transistors Using Transimpedance Amplifiers," *IEEE Transactions on Electron Devices*, vol. 46, no. 5, pp. 993–1000, 1999.

Publication F

High-Speed Low-Noise PNP PIN Phototransistor Integrated in a 0.35 μm CMOS Process

Authored by P. Kostov, W.Gaberl, M. Hofbauer, and H. Zimmermann

Abstract

A low noise $50 \times 100 \, \mu m^2$ pnp pin phototransistor is presented in this paper. The phototransistor is fabricated in a 0.35 μm CMOS process. An optimized layout leads to responsivities up to 1.99 A/W and bandwidths up to 151.4 A/W. Noise measurements show a low total output current noise spectral density of only $6.67 \times 10^{-24} \, A^2/Hz$ for a collector current of 2 μA.

Keywords–phototransistor; PNP; PIN; light detection; noise; responsivity; bandwidth; CMOS;

1   Introduction

Next to p(i)n photodiodes and avalanche photodiodes, phototransistors (PTs) offer an additional possibility for light detection. Their integration in silicon paves the way for light detection in the visible and near-infrared range up to wave-lengths of 1.1 µm. The properties of silicon lead to a wave-length dependent penetration depth of the photons (e.g. the penetration depth at 850 nm is $\sim 16\,\mu m$, while at 410 nm it is only $\sim 0.2\,\mu m$) [1]. The wavelength dependent penetration depth causes a different ratio of drift and diffusion parts of the photogenerated current. Thus, common CMOS integrated PTs, like the one in [2], achieve small bandwidths for photons with longer wavelengths. E.g. the pnp PT presented in [2] achieves a bandwidth of only 33.9 kHz and a responsivity of 0.83 A/W which results in a responsivity-bandwidth product (RBP) of $28.1 \times 10^{-3}\,\text{A/W} \cdot \text{MHz}$ for red light. A bandwidth reduction for longer wavelengths can be avoided by placing a thick low doped p-epi layer between the base and the collector of the PT, leading to a wider base-collector space-charge region (BC-SCR). A thicker BC-SCR causes an increase of the drift current portion of the photogenerated current. Such a PT with a RBP of $171.1\,\text{A/W} \cdot \text{MHz}$ at 675 nm is presented in [3]. The increased RBP, especially the higher bandwidth, opens the possibility to use these PTs as photodetectors in additional application fields, e.g. fast opto-coupler, shear sensors, time-of-flight sensors, etc. However, depending on the application it can be useful to optimize the trade-off between bandwidth and responsivity of the photodetector. In such cases PTs have an advantage over photodiodes since their behavior can be optimizing by changing the layout of the base and the emitter.

2   Phototransistor Layout and Theory

Fig. 1 shows a 3D depiction of the presented pnp PT. The PT was built in a standard 0.35 µm CMOS technology. A low doped epi-layer with a thickness of $\sim 15\,\mu m$ was placed on top of the high doped p^+ substrate, leading in a thicker BC-SCR and thus in a reduced BC capacitance C_{BC}. The PT has a size of $50 \times 100\,\mu m^2$ and consists of 18 base-emitter (BE) pairs. Each emitter is $0.7 \times 0.7\,\mu m^2$ large. A $3.1 \times 3.1\,\mu m^2$ n-well under each emitter forms the base. Between the BE-pairs a
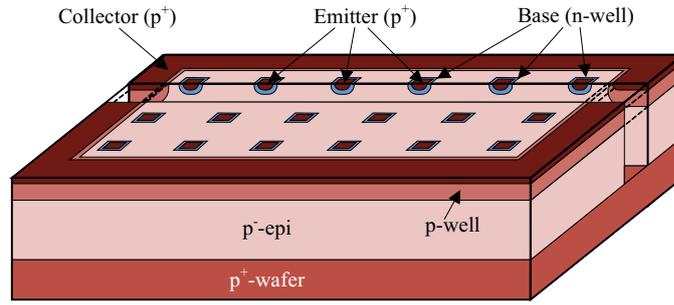
Figure 1: *3D depiction of the presented phototransistor.*

gap of 17.6 µm and 16.1 µm, respectively, is present in both directions.

In the presented pnp PT the BC-SCR works as a photodiode. The generated photocurrent equals a base current and is amplified by the inherent transistor. Each photogenerated electron-hole pair is split in the BC-SCR. The electron drifts into the base making its potential more negative. When the base potential approaches the forward voltage of the BE-diode the emitter starts injecting holes through the base towards the collector. The relationship between the injected holes and the electrons in the base is expressed by the current gain β which is mainly dependent on the doping concentrations of the base and emitter (N_B and N_E) and on the effective base width W_B [4]:

$$\beta = \frac{I_C}{I_{PH}} \propto \frac{N_E}{W_B N_B} \tag{1}$$

The small BE pairs lead to an inhomogeneous electrical field in the BC-SCR between the pairs and thus to a higher probability for electron recombination in the field free region of the p epi layer. This causes a reduction of the responsivity. However, a larger BE area would cause an increase of the corresponding capacity C_{BE}. This will lead to a reduced $-3\,\mathrm{dB}$ bandwidth of the PT. Furthermore, the $-3\,\mathrm{dB}$ bandwidth of the PT depends on the BC-SCR capacity C_{BC}, the transconductance g_m, the base transit time τ_B and the current gain β:

$$f_{-3dB} \propto \frac{1}{\beta \left(\tau_B + \frac{C_{BE} + C_{BC}}{g_m} \right)} \tag{2}$$

A third important equation is necessary for describing the output noise current density of the PT [5]:

$$\frac{\overline{i_{o_{PT}}^2}}{\Delta f} = \overline{\left(\beta \frac{i_b}{\sqrt{\Delta f}} + \frac{i_c}{\sqrt{\Delta f}}\right)^2} = \beta^2 \frac{\overline{i_b^2}}{\Delta f} + \frac{\overline{i_c^2}}{\Delta f} + 2\Re\left\{C\sqrt{\beta^2 \frac{\overline{i_b^2}}{\Delta f} \frac{\overline{i_c^2}}{\Delta f}}\right\} \qquad (3)$$

As can be seen from (3) the total output current noise density consists of three terms; the base noise current multiplied with the squared current gain, the noise current caused by the collector current and the correlation between both noise sources. The correlation factor C describes the correlation strength. It equals 1 for an open-base configured PT [6].

3   Measurements & Results

The PT's responsivity and bandwidth were characterized at 410 nm, 675 nm, and 850 nm with optical powers of -13.0 dBm, -19.2 dBm, and -15.8 dBm, respectively. These light power values have been chosen to get the same collector current for each wavelength. The collector-emitter voltage V_{CE} was set to three different values: -2 V, -5 V, and -10 V. Fig. 2 depicts the frequency response of the PT at $V_{CE} = -10$ V. Bandwidths > 100 MHz for the three wavelengths were achieved. Bandwidths and responsivities at different V_{CE} are shown in Fig. 3. A maximum responsivity of 1.99 A/W was measured. Furthermore at 675 nm and $V_{CE} = -10$ V the highest RBP with 245.5 A/W $\cdot$ MHz is achieved. Table I summarizes the measured responsivity and bandwidth values together with the corresponding RBPs at $V_{CE} = -10$ V.

In addition to responsivity and bandwidth measurements the output noise current density $\overline{i_{o_{PT}}^2}$ of the PT was measured. The measurements were performed by means of a light bulb as light source. For the characterization the intensity of the light was adjusted to meet four different collector currents: 100 nA, 500 nA, 1 µA, and 2 µA. $\overline{i_{o_{PT}}^2}$ was measured with a low noise transimpedance amplifier (TIA) with 300 kΩ feedback resistor together with a spectrum analyzer (SA) [6]. The noise spectral density is depicted in Fig. 4. A low mean output noise current level of

$6.67 \times 10^{-24} \, \text{A}^2/\text{Hz}$ was measured for $I_C = 2 \, \mu\text{A}$.
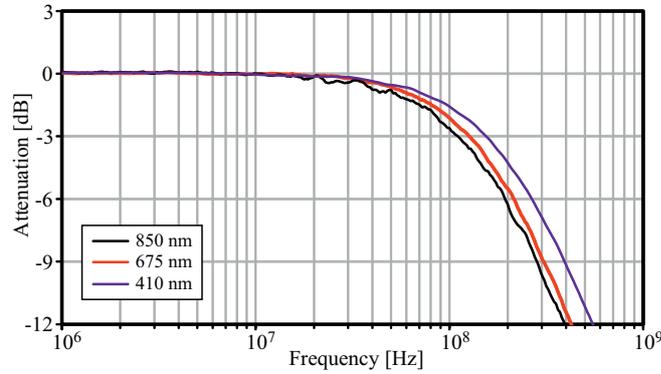
Figure 2: *Measured frequency response at $V_{CE} = -10 \, V$.*
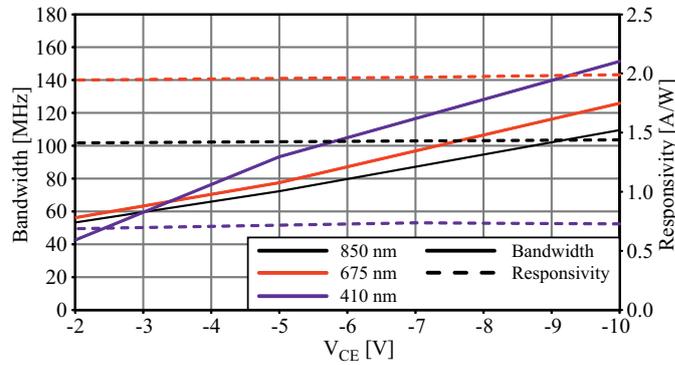
Figure 3: *Responsivity and bandwidth dependence on V_{CE}.*

4   Conclusion

In this paper a low-noise, high-speed pnp pin phototransistor is presented. The device is built in a $0.35 \, \mu\text{m}$ CMOS process and consists of a low doped p-epi layer together with 18 small base-emitter pairs. Bandwidths up to $151.4 \, \text{MHz}$ and responsivities up to $1.99 \, \text{A/W}$ are achieved. Compared to common pnp phototransistors built in the same technology [2] the introduced phototransistor exceeds the presented values: For red light the achieved responsivity-bandwidth product of $152.8 \, \text{A/W} \cdot \text{MHz}$ for $V_{CE} = -5 \, \text{V}$ exceeds that of [2] under the same conditions by more than 5400 times. The highest responsivity-bandwidth product of
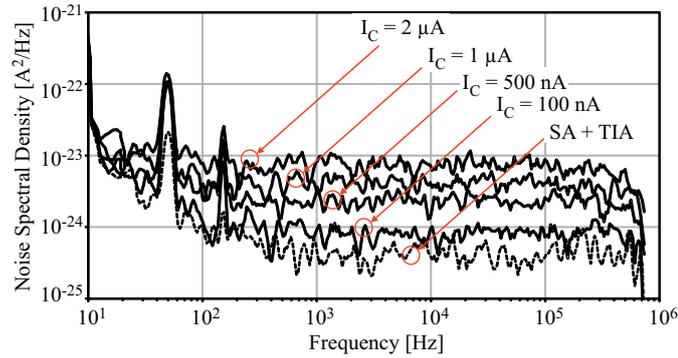
Figure 4: *Measured output noise current spectral density of the phototransistor for different light intensities.*

Table I: *Responsivities, bandwidths and responsivity-bandwidth product at the three different wavelengths for $V_{CE} = -10$ V.*

	BW [MHz]	R[A/W]	RBP[A/W · MHz]
410 nm	151.4	0.69	104.5
675 nm	125.9	1.95	245.5
850 nm	109.6	1.41	154.5

245.5 A/W · MHz was achieved for $V_{CE} = -10$ V. Compared to the results presented in [3], the introduced phototransistor has a 1.43 times better responsivity-bandwidth product under the same conditions. Furthermore, very low output noise current densities down to 0.78×10^{-24} A^2/Hz at $I_C = 100$ nA were measured.

Acknowledgements

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics.* Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] Y. Matsumoto, T. Hara, and Y. Kimura, "CMOS photo-transistor array detection system for visual light identification (ID)," in *IEEE International Conference on Networked Sensing Systems (INSS)*, pp. 99–102, 2008.

[3] P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Integrated 180 nm CMOS Phototransistors with an optimized Responsivity-Bandwidth-Product," in *IEEE Photonics Conference (IPC)*, pp. 314–315, 2012.

[4] S. Sze and K. Ng, *Physics of Semiconductor Devices.* New York, USA: John Wiley & Sons, Inc., third ed., 2006.

[5] D. Decoster and J. Harari, *Optoelectronic Sensors.* Hoboken, London: Wiley-ISTE, 2009.

[6] P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Low Frequency Noise in CMOS PNP PIN Phototranisistors," in *IEEE International Conference on Noise and Fluctuations (ICNF)*, p. accepted, 2013.

Publication G

Visible and NIR Integrated Phototransistors in CMOS Technology

Abstract

In this paper we present several different types of fully integrated pnp phototransistors realized in a $0.6\,\mu m$ OPTO ASIC CMOS process using low doped epitaxial starting wafers. Different types of phototransistors were realized by varying base doping profile and emitter area. This variations lead to different characteristics of the phototransistors. Devices with high responsivities or high bandwidths are achieved. Responsivities up to $98\,A/W$ and $37.2\,A/W$ for modulated light at $330\,kHz$ were achieved at $675\,nm$ and $850\,nm$ wavelengths, respectively. On the other hand bandwidths up to $9.7\,MHz$ and $14\,MHz$ for $675\,nm$ and $850\,nm$ wavelength, respectively, were achieved at the expense of a reduced responsivity. Due to the fact that the used process is a standard silicon CMOS technology, low-cost

integration to an integrated optoelectronic circuit is possible. This could lead to possible applications like low-cost, highly sensitive optical receivers, optical sensors, systems-on-a-chip for optical distance measurement or combined to an array even in a 3D camera.

Keywords: Phototransistor; CMOS; Light Detector; SoC; OEIC

1   Introduction

Photodetectors are used to convert optical into electrical signals. Most used photodetectors are PN-photodiodes, PIN-photodiodes, avalanche photodiodes (APD) and phototransistors (PT). The goal of the PTs as well as APDs is to increase the responsivity compared to conventional photodiodes. For integrated circuits, different types of photodetectors can be built in a standard CMOS process.

Photodiodes can be realized for high speed or high responsivity applications. The characteristics of detectors depend strongly on the used wavelength. Near infrared (IR) light, e.g. 850 nm, has a $1/e$ penetration depth of around 16 µm whereas red light, e.g. 675 nm, has a penetration depth of 4.1 µm in silicon [1]. The PN-photodiode consists of a basic p-n junction, which can be realized by two different layouts in a standard CMOS process. Each structure has advantages in either high speed or high responsivity.

First, a PN diode can be realized by an n-well/p-substrate diode. This structure can receive photons of the complete visible and near infrared spectrum. The large penetration depth of the near infrared light leads to long travel distances for charges in the field free diffusion region. Therefore this structure has a large diffusion and a small drift current portion for near-infrared light. This leads to a slow detector.

Second, a PN diode can be built by a p^+/n-well structure, which is inherently isolated in a common p-substrate. The photosensitive structure will be only around 1 µm thick and every electron-hole-pair generated by photons in the substrate will be lost for the photodiode. By losing all generated charges deep in the substrate, a

main portion of the diffusion current is omitted. Because of this mechanism such structures show a high bandwidth together with a rather low responsivity.

To achieve high bandwidths without losing the deep-generated charges, an additional low doped intrinsic layer is placed in the p-n junction. PN diodes with an additional intrinsic layer are called PIN diodes. For the integration of PIN diodes in a CMOS process, a special starting material is used. This starting material has a 10 to 15 µm low doped epitaxially grown layer on top of the high doped substrate. The intrinsic zone of the PIN diode is formed by this low doped epitaxial layer. Due to the low doping concentration of the intrinsic layer the extension of the space-charge region (SCR) inside the diode is increased. Therefore charges generated deep in the substrate are now accelerated by the electric field in the thick drift zone. The photodetector becomes faster and shows a rather high responsivity for a photodiode. These characteristics are also the reason why PIN diodes are mostly used as photodetectors for high speed applications, e.g. [2]. Furthermore PIN photodiodes are also used in distance measurement applications as single pixel [3], as line sensor [4] or as 3D camera [5]. Nevertheless, the responsivity of this photodetector is limited under best circumstances to 0.65 A/W and 0.55 A/W for 850 nm and 675 nm, respectively [1].

Photodiodes do not have an internal amplification. Their maximum possible quantum efficiency is 1. Maximum quantum efficiency will occur when all charges generated by photons contribute to the photocurrent. Phototransistors and avalanche photodiodes exceed this limitation with an internal amplification of the primary photocurrent. This amplification is desirable and important for detecting weak optical signals. APDs achieve their amplification by the avalanche multiplication process. This takes place at high electric field strengths and needs voltages of at least several tens of volts [6]. Such high voltages are hard to handle in integrated circuits. Furthermore APDs show a very narrow bias voltage range for linear operation and therefore nonlinear behaviour is expected for any changes of the bias voltage. Background light is also amplified in APDs, which can lead to saturation of pixel circuits. This is also the reason why APDs are not practicable for the use in image sensors or distance measurement setups, especially in bright

sunlight. Nevertheless there are many other application fields for APDs. Complex bias voltage control circuits are necessary to handle the above mentioned problems in APDs. In reference [7] a shallow APD for 430 nm light with a responsivity of 4.6 A/W at a reverse bias of 19.5 V is reported in CMOS. For red and infrared light, the detection probability decreases and much lower responsivities result.

Opposed to APDs PTs do not need such high voltages for their internal amplification. This is the most important advantage of PTs. In a phototransistor a large photodiode is formed by the base-collector diode. Also the base-emitter diode forms a photodiode but usually the area is small and the contribution is negligible. The internal bipolar transistor amplifies the primary photocurrent. Charges generated in the base-collector diode are separated and swept into base and collector. For pnp phototransistors, as shown in Fig. 1, electrons are swept into the base and holes into the collector area. The electron accumulation in the base area makes the potential of the base more negative. This effect leads furthermore to the injection of holes from the p^+ emitter into the base. This mechanism amplifies the generated primary photocurrent from the base-collector photodiode. A typical value for the responsivity of a PT in standard-burried-collector (SBC) bipolar or BiCMOS technology at 850 nm presented in [8] is 2.7 A/W. The SiGe PT in [8] has a thin thickness of the base-collector space-charge region of only about 1 μm, which leads to the low responsivity.

In this work we present silicon integrated PTs in a CMOS process with different layouts of the base and emitter area. The presented PTs achieve much higher responsivities than published bipolar SBC PTs. The higher responsivity is achieved
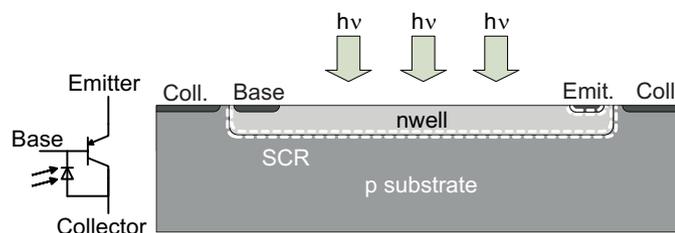
Figure 1: *Schematic and cross section of a phototransistor integrated in a standard CMOS process.*

due to implementing a deep intrinsic layer for a thick base-collector SCR. Different designs of the base and emitter area can be used to optimize the devices for different goals such as high responsivity or high speed. Cheap CMOS integration of PTs paves the way for optoelectronic integrated circuits (OEICs) and system-on-chip (SoC) with several advantages. Such advantages are e.g. smaller area due to only one die instead of two (one for the photodetector and one for the circuit), no bond wires, handling, packaging and many more advantages. The fact that PTs need only low voltages compared to APDs and show a high responsivity due to the current amplification makes them well suited for different SoC applications like active pixels, light barriers or optocouplers.

2 Device Structure Options

Several versions of pnp-type PTs with a photosensitive area of $100 \times 100 \, \mu m^2$ were implemented in a $0.6 \, \mu m$ OPTO ASIC CMOS process. The only difference to a standard CMOS ASIC process is the use of a special starting wafer for the implementation of the PTs. This special wafer has a thick ($\sim 15 \, \mu m$), low-doped ($2 \times 10^{13} \, cm^{-3}$) p-epitaxial layer and on top a shallow ($\sim 1 \, \mu m$), low-doped ($10^{14} \, cm^{-3}$) n-epitaxial layer. Below is the highly doped p-substrate material. The p-epitaxial layer leads to a PIN structure for the base-collector junction. Thus the device gets a thick SCR even for low voltages. A thick SCR is well suited for light with a high penetration depth, e.g. light with a wavelength of $850 \, nm$. Nevertheless, the bandwidth of PTs is lower than the bandwidth of PIN photodiodes. The reason for this limitation is the fact that PTs have two p-n junctions and thus two capacitances (base-collector capacitance C_{BC} and base-emitter capacitance C_{BE}). An additional bandwidth limiting factor is the base transit time τ_B which is not present in a PD. The definition of the $-3 \, dB$ bandwidth of a PT is shown in equation (1) [9]:

$$f_{-3dB} = \frac{1}{2\pi\beta(\tau_B + \frac{k_B T}{q I_E}(C_{BE} + C_{BC}))},\tag{1}$$

In (1) β is the current gain, τ_B is the base transit time, k_B is the Boltzmann constant, T is absolute temperature, q is the elementary charge and I_E is the

emitter current of the transistor. All PTs have different layout structures. The different structures lead to different characteristics of each device. The following subsections describe the collector (p-substrate), base (n-region) and emitter (p-region) areas.

2.1   Collector Area

The collector is formed by the p-type substrate. It is connected via a large-area ring of substrate contacts on the border of the PT and tied to substrate potential. Due to this fact the PT can only be used in emitter follower setup.

2.2   Base Area

A shallow low-doped n-epitaxial layer forms the base. Inspired by [10], the doping concentration of the base can be varied by additional n-well implantations inside the n-epi layer. In this work three different base layouts (Fig. 2) are used.
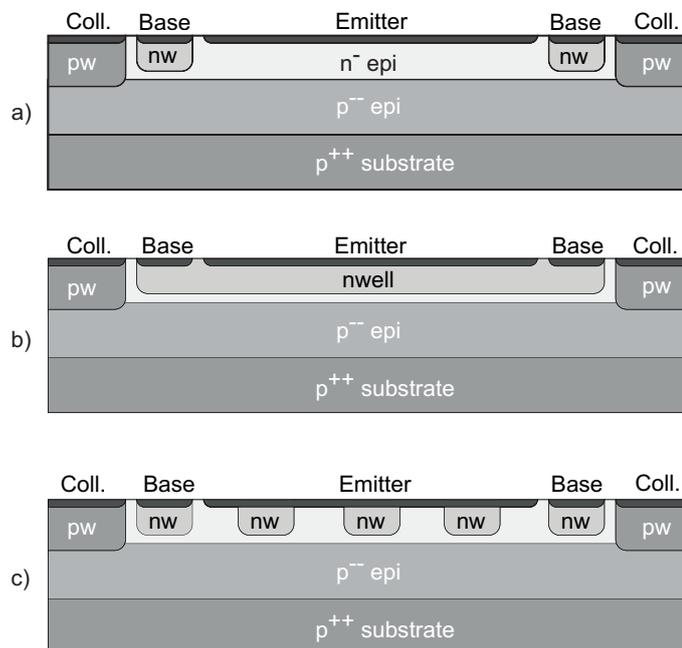
Figure 2: *Different base designs (cross section): (a) base without additional n-doping, (b) base with highest doping concentration, (c) base with varied doping concentration.*

Fig. 2a shows the layout with the lowest doped base. In this structure no additional n-wells, except for contacting the area, are implanted which leads to an increased thickness of the SCRs for base-collector diode and for the base-emitter diode. The increase of SCRs thickness leads to a decrease of the capacitances C_{BC} and C_{BE} and to a reduced effective base width W_B. These facts cause a faster transport of the minority carriers through the thinner effective base region, resulting in an increase of the PT's bandwidth. Depending on the collector-emitter voltage, the effective base thickness can become zero and the SCRs can touch each other with the effect of a reachthrough current between emitter and collector.

Fig. 2b depicts the second version of the base layout with the highest doped base. The base is implemented as a full n-well. The higher doped base leads to thinner SCRs (compared to Fig. 2a) which leads to larger capacitances C_{BC} and C_{BE} and a thicker effective base width. Therefore the device speed is slower and the current gain β decreases [11]:

$$\beta = \frac{1}{\frac{W_B^2}{2\tau_B D_p} + \frac{D_n W_B N_D}{D_p L_n N_A}}.$$ (2)

In (2) τ_B is the minority lifetime in the base, D_p is the carrier diffusion coefficient of holes in the n-type base, D_n is the diffusion coefficient of electrons in the p-type emitter, L_n is the electron diffusion length in the emitter, and N_D and N_A are the donor and acceptor densities in the base and emitter [11].

Fig. 2c shows a method to vary the doping concentration of the base with the technology available in a standard CMOS process. Therefore the bandwidth and gain properties can be adjusted by the width-to-spacing ratio of the n-well stripes. Three different width-to-spacing ratios were designed:

- NW_{33}: 1 µm stripe with 2 µm space,

- NW_{50}: 1 µm stripe with 1 µm space,

- NW_{66}: 2 µm stripe with 1 µm space.

During the CMOS processing, the designed stripes diffuse into an inhomogeneously

doped base layer. Due to this effect it is possible to adjust the effective base doping even in a standard ASIC process.

2.3   Emitter Area

The properties of the PT can be varied by the base doping concentration as well as the different emitter area layouts. In this work we implement three different versions of the emitter layout. Fig. 3 shows the top view of the three different emitter layouts with a full n-well base.

In Fig. 3a a full plane emitter with an area of $97 \times 97\,\mu m^2$ is shown. This layout type leads to a low current density resulting in a reduced cut-off frequency. Due to the large emitter area, the generated charges move only vertically and therefore have to travel over the shortest distances. A disadvantage of the large emitter area is the low current density in the emitter as well as a high base-emitter capacitance C_{BE}. This disadvantage results according (1) in a low $-3\,dB$ cut-off frequency.

Fig. 3b and 3c shows the PT-layout with the smaller sized emitter-area. The stripes of the emitter in Fig. 3b are $1.4\,\mu m$ wide and have an $8.4\,\mu m$ wide gap between them. The small emitter of Fig. 3c is placed in the centre of the PT and has a size of $1.4 \times 1.4\,\mu m^2$. Both structures have in common, that the current density is higher and the base-emitter capacitances are lower because of the smaller emitter area. Due to these effects, the $-3\,dB$ bandwidth of the PT is increased. As a disadvantage can be mentioned, that the electric field in the PTs is not homogenous
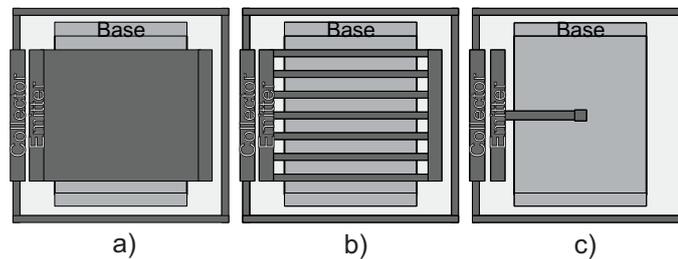
Figure 3: *Top view of different emitter layouts with full n-well base: (a) full plane, (b) stripes, (c) point.*

anymore and therefore the charge carriers have to travel over longer distances. During traveling over longer distances recombination can occur which leads to a reduced gain of the PT.

A second version of a small-emitter-PT was also produced, where the small-emitter has a size of $7.0 \times 1.4\,\mu m^2$ and was placed at the corner of the PT outside the photosensitive area. The placement of the emitter outside of the photosensitive area enables the possibility to use an additional opto-window, i.e. an anti-reflection coating, which will increase the responsivity by about 2 to 3 dB depending on the wavelength. For a better comparison with the other PTs this version was also built without an opto-window.

3   Measurements and Results

The PTs' properties were characterized by three different measurements. First, the electrical current amplification was verified through Gummel measurements. Second, the DC responsivity was measured by sweeps of the light power at 675 nm and 850 nm wavelength. Third, the AC responsivity respectively bandwidth was measured at an average optical power of $-10\,\text{dBm}$ and $-21.2\,\text{dBm}$ for 850 nm wavelength as well as $-13.4\,\text{dBm}$ and $-24.6\,\text{dBm}$ for 675 nm wavelength. Due to different responsivities of the PIN base-collector diode at 675 nm and 850 nm light, the optical power for each wavelength was adapted to meet the same collector current. Laser diodes were used for the DC and AC light measurements. For AC light measurements the extinction ratio was set at 2:1.

3.1   Gummel measurements

PTs without additional doping in the base (Fig. 2a) show a reach-through effect for a collector emitter voltage of 4 V and beyond. This fact is due to a direct contact of both SCRs as described above. The photodetectors with the higher doped base show the expected current amplification β between 57 and 176. Thereby the highest amplification was achieved by the PT with the 33% doped n-well base and the small centre emitter (Fig. 4) and the lowest one by the PT with the full

n-well base and the corner emitter. PTs with lower doping concentration of the base (striped n-well base PTs) have a higher current gain β than PTs with higher doping concentration of the base (full n-well base PTs). This results from equation 2 with a smaller effective base width W_B for the striped n-well base PTs. The dark currents for these PTs were below 60 pA, so no reach-through occurred.

In contrast to the phototransistors of Fig. 2a without additional n-well doping, only PTs with 33% doped n-well base and full plane emitter shows reachthrough. In case of low currents their β reaches values up to 10^5. Fig. 5 depicts the Gummel plot of such a transistor. The dark current for this special PT was only about 4.56 µA for a collector-emitter voltage of 4 V. The current was limited to 10 mA to protect the device from damage during measurement.

3.2   DC measurements

The DC measurements were done on PTs at 675 nm and at 850 nm by varying the optical power with an optical attenuator. The optical power was varied for the measurements with 675 nm from -62.6 dBm to -11 dBm, respectively, for 850 nm from -55 dBm to -11 dBm. The optical power of -62.6 dBm is much smaller than that used in [12] and therefore a higher responsivity is observed here at 675 nm. An optical 50/50 beam splitter was used to monitor the optical power via an optical power meter. The collector emitter voltage was varied from 1 V to 8 V. DC responsivities at a collector-emitter voltage of 4 V for three PTs are shown in Fig. 6. A light power increase shows a decrease of the responsivity due to the operating point variation. This fact is due to an increase of the induced base current in the range of several µA which leads to a reduced current gain β due to the Kirk effect [13].

As visible in Tab. 1, the responsivity shows only a minor dependence on the collector-emitter voltage. An even better responsivity (98 A/W) than listed in Tab. 1 for -30 dBm optical input power was achieved for -62.6 dBm optical power. The maximum achieved responsivity at a collector-emitter voltage of 4 V was 98 A/W and 36 A/W for 675 nm and 850 nm, respectively. These values were
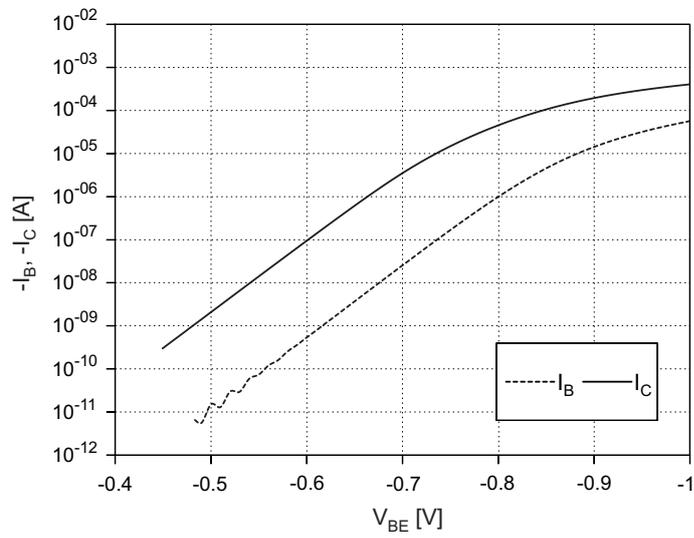
Figure 4: *Gummel plot of the 33% doped n-well base and center emitter phototransistor.*
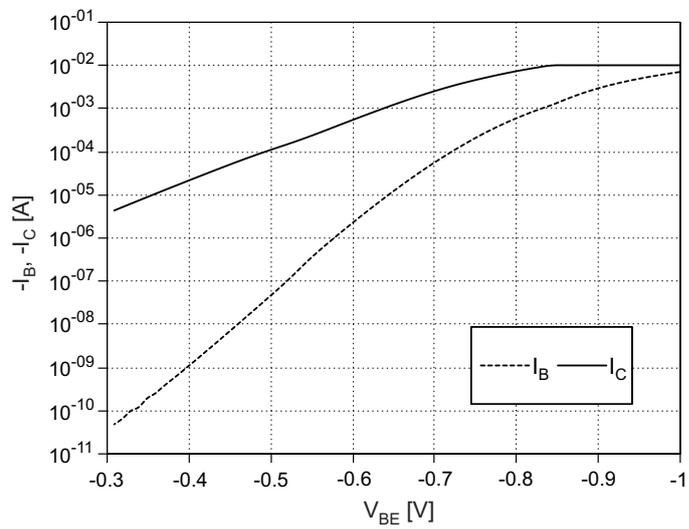
Figure 5: *Gummel plot of the 33% doped n-well base and full plane emitter phototransistor operating near to the reach-through scenario.*

Table 1: *Responsivity in A/W for two phototransistors at an optical power of*
−30 dBm, different collector-emitter voltages and 675 nm respectively 850 nm
wavelength.

	λ=675 nm			λ=850 nm		
	V_{CE}=−1 V	V_{CE}=−4 V	V_{CE}=−8 V	V_{CE}=−1 V	V_{CE}=−4 V	V_{CE}=−8 V
$NW_{50}E_{full}$	61.2	64.7	68.4	30.8	32.0	33.8
$NW_{50}E_{ctr}$	23.9	25.4	27.0	14.6	15.5	16.3

achieved for the PT with the 50% doped n-well base (NW_{50}) and the full plane
emitter. By means of the full plane emitter the photogenerated carriers have
the shortest travel distance to the emitter which minimises carrier diffusion and
recombination in the base and furthermore improves the responsivity of the device.

Due to a larger penetration depth of 850 nm light, the effect of the SCRs is larger.
At this wavelength, the responsivity values varied from 36 A/W to about 10 A/W
for the three different types of PTs shown in Fig. 6. These values were achieved
for a low optical power of −55 dBm at a collector-emitter voltage of −4 V. For
an optical power of −11 dBm, the responsivity values were about 2 A/W. The
smallest responsivity change was measured at the full and striped emitter devices.
For these devices the responsivity change is below 20% over the whole light power
range.

The PTs which operate near reach-through scenario (33% doped n-well base NW_{33}
with full plane emitter) show a dark current corrected DC responsivity of 23 000 A/W
at a low optical light power of −55 dBm and 80 A/W at a high optical power of
−11 dBm both at 850 nm.

3.3 AC measurements

The dynamic responsivity and bandwidth of the photodetectors was measured by
means of modulated light. These measurements were done at a low optical power
of −21.2 dBm and at a high optical power of −10 dBm at 850 nm, respectively,
−24.6 dBm and −13.4 dBm at 675 nm. The optical power was adjusted to dif-
ferent values for 675 nm and 850 nm to meet the same collector current for each
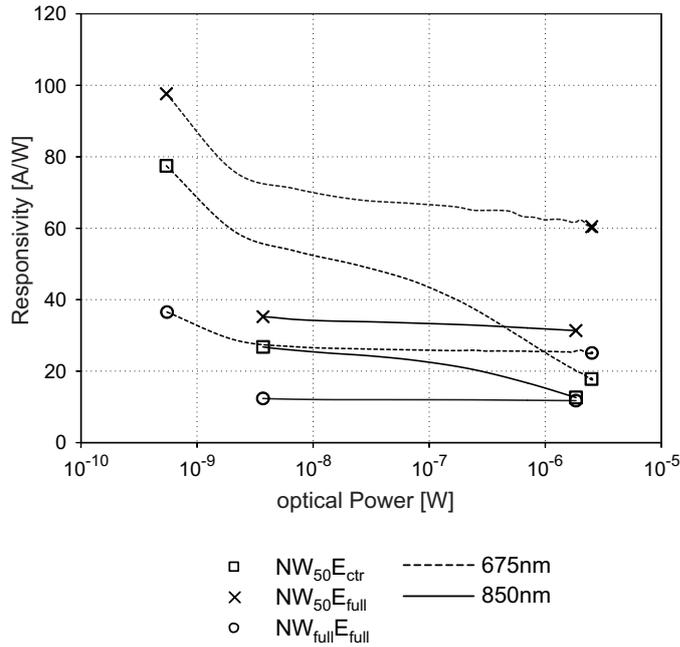
Figure 6: DC responsivity vs. optical power for three different types of PTs.

wavelength. The devices were characterized at three different collector-emitter voltages: $-2\,\mathrm{V}$, $-5\,\mathrm{V}$ and $-10\,\mathrm{V}$. For operating point adjustment on the PTs, a current sink was applied to the base (via an on-chip $1\,\mathrm{M\Omega}$ resistor). Eight PTs were characterized at five different operating points at $675\,\mathrm{nm}$ (Fig. 7) as well as at $850\,\mathrm{nm}$ (Fig. 8) light.

For both wavelengths the measurements at the high optical power show a decrease of the responsivity for larger base currents. This is due to increased base currents and therefore decreased current amplifications [13]. PTs with a small emitter have a small but rather constant responsivity. This fact is due to an increased recombination of charges in the base, since some generated charges have to travel longer distances to reach the emitter. Large emitter devices show larger voltage dependent responsivities. Furthermore their responsivity is larger compared to PTs with small emitter, since the generated charges have to travel only short distances to reach the emitter. The PT with 50% n-well and full emitter showed the largest responsivity of $98\,\mathrm{A/W}$ at $675\,\mathrm{nm}$ and $37.2\,\mathrm{A/W}$ at $850\,\mathrm{nm}$ both for $V_{CE} = -10\,\mathrm{V}$. The responsivity decreases for low optical power for all

PTs at higher base currents. The responsivity of small emitter PTs does not depend much on the collector-emitter voltage. However, the dependence is stronger for 675 nm than for 850 nm wavelength. This is due to the fact, that 850 nm light has a larger penetration depth in silicon and therefore a smaller part of the generated charges contribute to the amplified photocurrent compared to 675 nm light. Furthermore, the PTs with larger emitter sizes show a strong increase of the responsivity for higher collector-emitter voltages. Also in this case the PTs show at 675 nm a stronger increase of the responsivity than at 850 nm wavelength.

The bandwidth is nearly constant for all PTs for all operating points in both wavelength cases at high optical power conditions. This fact is due to a certain operating condition ensured by the incident optical power. A variation of the collector-emitter voltage leads to a change in the SCR thickness in the PTs. This change leads furthermore to a change of the capacitances and the effective base width and according (1) to a change of the bandwidth. At low optical power conditions the bandwidth is also strongly dependent on the collector-emitter voltage. For 850 nm the bandwidth increases by increasing the base current. In the case of 675 nm wavelength the bandwidth stays independent of the operating point. Small-emitter PTs show higher bandwidths than large-emitter ones due to a smaller base-emitter capacitance.

In addition to responsivity and bandwidth measurements, transient measurements of eight transistors were done. For the transient behaviour measurements the PTs were set up in emitter follower configuration, where the output signal was capacitively coupled to the $50\,\Omega$ input of an oscilloscope by an additional bias tee. Fig. 9 shows the step function of the PT with 50% doped n-well base (NW_{50}) and full emitter at a collector-emitter voltage of $-10\,\text{V}$ and floating base. The measurement was done at 675 nm wavelength and an optical power of $-13.4\,\text{dBm}$. The rise time of this PT is 140 ns and its fall time is 156 ns. Further rise times for this, as well as for the other PTs at different operating point conditions and wavelengths are listed in Tab. 2.1 and Tab. 2.2. The PT with the full n-well and the corner emitter has the fastest rise-times. Also for all PTs the rise time results correspond to the bandwidth results.
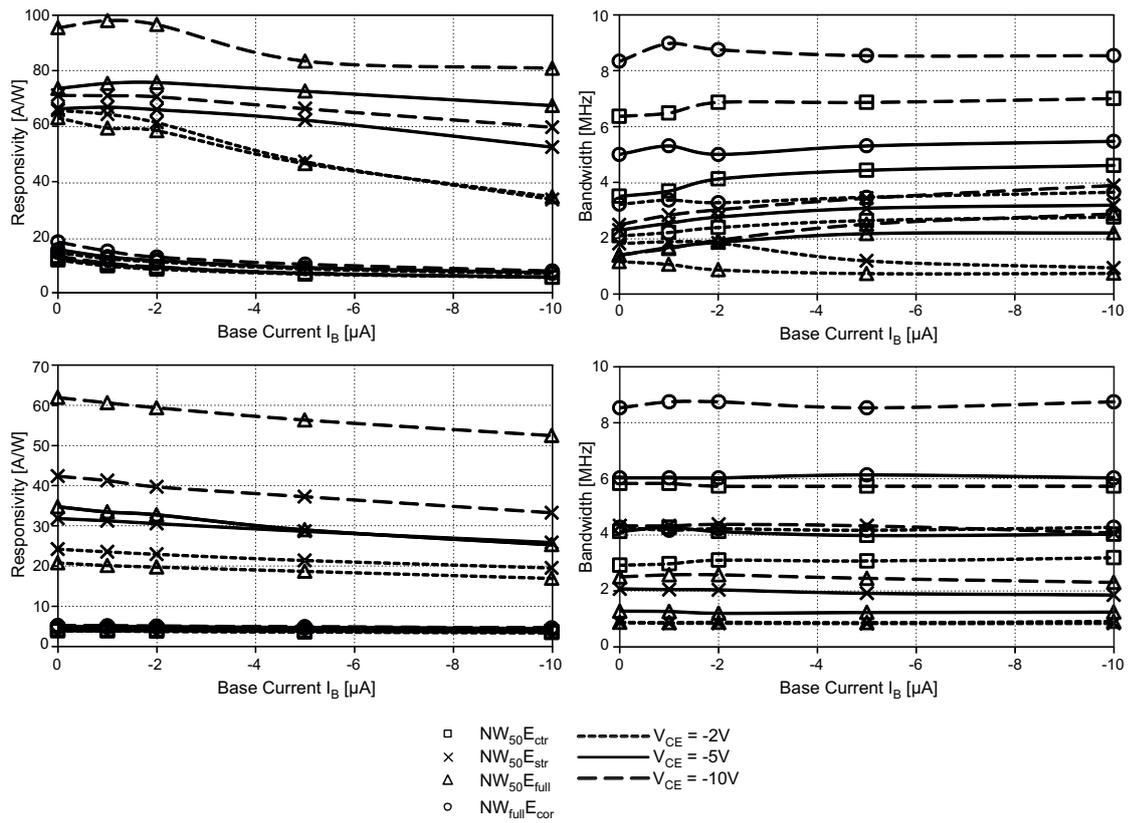
Figure 7: *Responsivity and bandwidth measurements at 675 nm for four phototransistors (upper diagrams - low optical power, bottom diagrams - high optical power).*
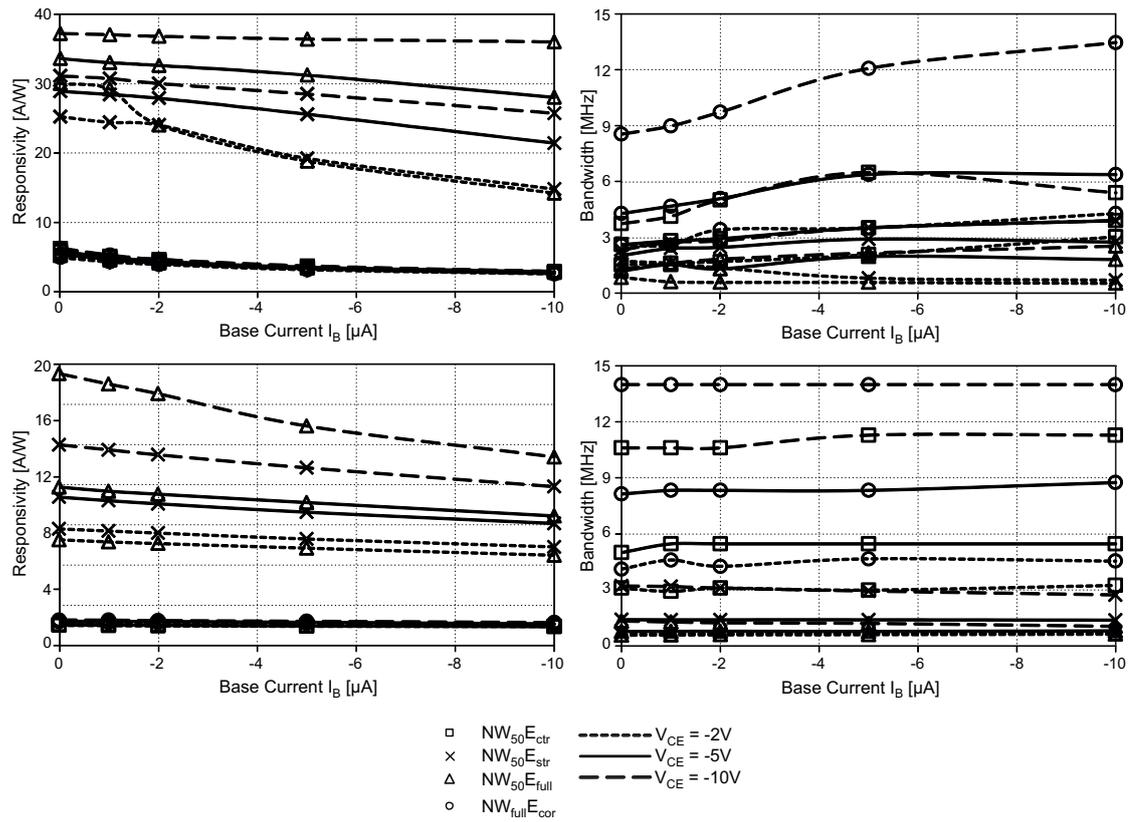
Figure 8: *Responsivity and bandwidth measurements at 850 nm for four phototransistors (upper diagrams - low optical power, bottom diagrams - high optical power).*

Table 2.1: *PT rise times at 675 nm in nanoseconds.*

V_{CE}		−2 V					−5 V					−10 V			
I_B	0 A	1 µA	2 µA	5 µA	10 µA	0 A	1 µA	2 µA	5 µA	10 µA	0 A	1 µA	2 µA	5 µA	10 µA
Low optical power (−24.6 dBm)															
$NW_{50}E_{ctr}$	168	159	147	133	127	100	95	85	79	76	55	54	51	51	50
$NW_{50}E_{str}$	194	187	192	295	374	153	138	127	114	110	141	124	116	102	90
$NW_{50}E_{full}$	302	330	406	479	476	253	210	189	162	160	250	215	182	140	122
$NW_{full}E_{cor}$	109	104	107	101	96	70	66	70	66	64	42	39	40	41	41
High optical power (−13.4 dBm)															
$NW_{50}E_{ctr}$	120	118	113	114	110	85	82	85	88	87	60	60	61	61	61
$NW_{50}E_{str}$	404	413	415	419	417	169	171	172	183	189	81	81	80	81	86
$NW_{50}E_{full}$	399	406	398	405	386	274	277	292	285	282	140	136	136	143	152
$NW_{full}E_{cor}$	82	84	83	84	82	58	58	58	57	58	41	40	40	41	40

Table 2.2: *PT rise times at 850 nm in nanoseconds.*

V_{CE}		−2 V					−5 V					−10 V			
I_B	0 A	1 µA	2 µA	5 µA	10 µA	0 A	1 µA	2 µA	5 µA	10 µA	0 A	1 µA	2 µA	5 µA	10 µA
Low optical power (−21.2 dBm)															
$NW_{50}E_{ctr}$	230	220	208	170	116	135	125	120	100	90	94	85	70	54	65
$NW_{50}E_{str}$	205	220	260	440	510	174	146	143	121	128	152	128	125	100	90
$NW_{50}E_{full}$	420	590	618	620	680	296	230	270	179	195	272	220	193	163	139
$NW_{full}E_{cor}$	136	136	103	100	82	82	76	69	55	55	41	39	36	29	26
High optical power (−10 dBm)															
$NW_{50}E_{ctr}$	113	120	113	117	108	70	64	64	64	64	33	33	33	31	31
$NW_{50}E_{str}$	553	544	534	518	510	249	250	250	250	253	109	110	113	119	128
$NW_{50}E_{full}$	607	597	588	577	555	452	448	445	450	433	262	272	282	290	333
$NW_{full}E_{cor}$	85	76	82	75	77	43	42	42	42	40	25	25	25	25	25

4   Conclusion

We present fully integrated silicon phototransistors in a CMOS OPTO ASIC process. The process uses a special starting material with an epitaxial layer on top of the p-substrate material. Several photodetectors with different layouts of the base and emitter area have been produced and characterized. The phototransistors were characterized by electrical Gummel plot as well as optical DC and AC measurements. The optical measurements were done at 675 nm and 850 nm light. For optical AC measurements two different incident optical light powers
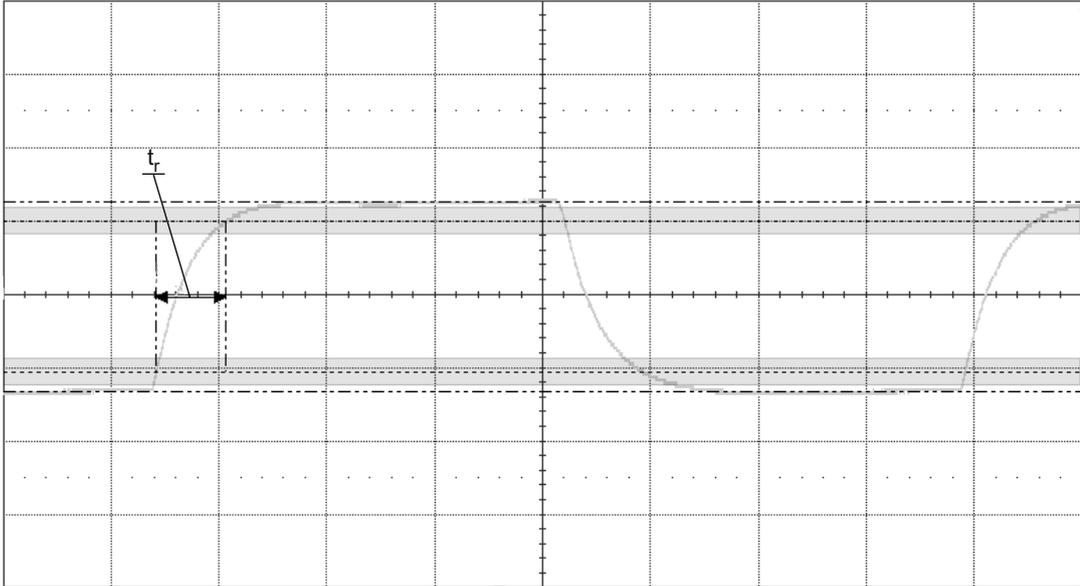
Figure 9: *Step function of the 50% doped n-well base PT with the full emitter at 850 nm, $V_{CE} = -10$ V, $P_{opt} = -13.4$ dBm, floating base. (Axis-properties: x: 200 ns/div, y: 50 mV/div).*

where applied. Furthermore measurements at different collector-emitter voltages were done. A maximal electrical current gain β of 176 was achieved for the 33% doped n-well base with small centre emitter phototransistor due to a small effective base width. The phototransistors achieve higher responsivities for 675 nm than for 850 nm, because of a shorter light penetration depth. In case of a 50% doped n-well base and full plane emitter phototransistor the highest responsivity of 98 A/W at 675 nm is reached. This value is about 37 times better compared to SBC npn phototransistors in SiGe BiCMOS technology. However, its bandwidth was in consequence limited to 1.6 MHz. A maximal bandwidth of 14 MHz was measured for the full n-well base and corner emitter phototransistor at 850 nm. In this operating condition the device has a responsivity of 1.8 A/W. It achieves at the same operating conditions a maximal bandwidth of 8.8 MHz and a responsivity of 5.2 A/W for 675 nm. If we introduce the bandwidth multiplied by the responsivity as figure of merit, the phototransistor with the 50% doped n-well base and striped emitter would have the best results over the most operating points. It achieves in the best case a bandwidth of 3.9 MHz and a responsivity of 60 A/W at 675 nm. In

addition to responsivity and bandwidth measurement also rise times of the phototransistors were measured and presented. The fastest phototransistor achieves a rise time of 25 ns. A phototransistor near to a reach-through scenario shows for a low optical input power a current amplification of up to 50.000. The properties of the phototransistors depend mainly on the base and emitter layout. This fact opens the opportunity to design optimal phototransistors for several optical sensing applications, imaging systems and optoelectronic SoCs.

Acknowledgements

References

[1] H. Zimmermann, *Integrated Silicon Optoelectronics.* Springer Series in Optical Sciences, Vol. 148, Berlin/Heidelberg, Germany: Springer-Verlag, second ed., 2010.

[2] R. Swoboda and H. Zimmermann, "11Gb/s Monolithically Integrated Silicon Optical Receiver for 850 nm Wavelength," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 904–911, 2006.

[3] A. Nemecek, K. Oberhauser, and H. Zimmermann, "Correlating PIN-Photodetector with Novel Difference-Integrator Concept for Range-Finding Applications," in *IEEE European Solid-State Circuits Conference (ESS-CIRC)*, pp. 491–494, 2005.

[4] G. Zach and H. Zimmermann, "A 2×32 Range-Finding Sensor Array with Pixel-Inherent Suppression of Ambient Light up to 120 klx," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 352–353,353a, 2009.

[5] G. Zach, M. Davidovic, and H. Zimmermann, "Extraneous-Light Resistant Multipixel Range Sensor Based on a Low-Power Correlating Pixel-Circuit,"

in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 236–239, 2009.

[6] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, pp. 1956–1976, 1996.

[7] A. Pauchard, A. Rochas, Z. Randjelovic, P. Besse, and R. Popovic, "Ultraviolet avalanche photodiode in cmos technology," in *International Electron Devices Meeting (IEDM)*, pp. 709–712, 2000.

[8] T. Yin, A. Pappu, and A. Apsel, "Low-Cost, High-Efficiency, and High-Speed SiGe Phototransistors in Commercial BiCMOS," *IEEE Photonics Technology Letters*, vol. 18, no. 1, pp. 55–57, 2006.

[9] G. Winstel and C. Weyrich, *Optoelektronik II*. Berlin/Heidelberg, Germany: Springer-Verlag, 1986.

[10] A. Marchlewski, H. Zimmermann, G. Meinhardt, I. Jonak-Auer, and E. Wachmann, "Pnp pin phototransistor with modulation-doped base," *Electronics Letters*, vol. 46, no. 16, pp. 1154–1155, 2010.

[11] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*. Wiley, 5th ed., 2008.

[12] P. Kostov, W. Gaberl, and H. Zimmermann, "Integrated Phototransistors in a CMOS Process for Optoelectronic Integrated Circuits," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 250–253, 2010.

[13] R. Whittier and D. Tremere, "Current Gain and Cutoff Frequency Falloff at High Currents," *IEEE Transactions on Electron Devices*, vol. 16, no. 1, pp. 39–57, 1969.

Publication H

Development and Verification of a CMOS Phototransistor Noise Model

Authored by P. Kostov, W.Gaberl, M. Hofbauer, and H. Zimmermann

Abstract

In this paper a noise model for phototransistors is presented. Noise measurements and Gummel measurements on four different phototransistors were performed to verify the noise model. In addition, the output noise current density was modeled and compared with the measurements. A maximum difference of less than 12% is noticed.

Keywords–phototransistor; noise; noise model; shot noise; gummel; current gain; pnp; pin;

1   Introduction

Phototransistors (PTs) are promising devices for detection of light. Compared to p(i)n photodiodes they have an inherent gain. Together with a suitable readout circuitry they offer possibilities for different applications, e.g. shear sensors, image sensors [1], opto-couplers, etc. In such applications typically bandwidths below 100 MHz are sufficient. This allows the use of PTs. However, it is important to analyze the photodetectors' noise, since the noise determines the sensitivity. Thus, it is advantageous and important to have a noise model of the PT for further circuit analysis.

2   Phototransistors, Noise Model and Theory

Four pnp pin PTs were used for the development and analysis of the noise model. Each PT was fabricated in a 0.6 μm CMOS technology and has a thick, low doped p-epi collector layer, ensuring a thick space-charge region (SCR). This leads to an increased bandwidth and responsivity of the PT. Furthermore, the layout of the base and the emitter of each PT is unique, leading to different characteristics:

- $NW_{50}E_{ctr}$: half doped base, small center emitter.

- $NW_{50}E_{str}$: half doped base, stripped emitter.

- $NW_{50}E_{full}$: half doped base, full emitter.

- $NW_{full}E_{cor}$: full n-well base, small corner emitter.

Fig. 1 shows a 3D view of the $NW_{50}E_{ctr}$ PT. Further details on layout and characteristics of these PTs can be found in [2]. Fig. 2 depicts the developed noise model of a pnp pin PT in an open-base configuration, as used in the measurement setup. According to this model, the total output noise is composed of the base noise current and the collector noise current. Furthermore, since these currents are correlated a third additional noise term arises in the total output noise current formula [3]:

$$\frac{\overline{i_{oPT}^2}}{\Delta f} = \overline{\left(\beta\frac{i_b}{\sqrt{\Delta f}} + \frac{i_c}{\sqrt{\Delta f}}\right)^2} = \beta^2\frac{\overline{i_b^2}}{\Delta f} + \frac{\overline{i_c^2}}{\Delta f} + 2\Re\left\{C\sqrt{\beta^2\frac{\overline{i_b^2}}{\Delta f}\frac{\overline{i_c^2}}{\Delta f}}\right\} \quad (1)$$

As shown in (1) the base noise current is amplified by the squared current gain β of the PT. β is mainly dependent on the minority charge carrier density inside the base. This leads to a decrease of β at higher collector currents (Kirk effect). The base noise current consists of a doubled shot noise part of the photocurrent, an $1/f^\gamma$ noise part in the low-frequency range and the thermal noise part of the base resistance. The doubling of the shot noise part is caused by the open-base setup of the PT [4]. In this case the base-emitter current equals the photocurrent and their shot noise terms are quadratically summed, since they are uncorrelated. The collector noise current part is caused by the shot noise of the collector current at the output of the PT. In the third term of (1) C describes the correlation between the first and the second term. It can take any value between -1 and $+1$
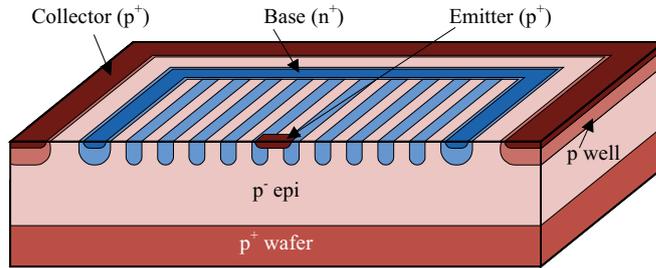

**Figure 1:** *3D depiction of the $NW_{50}E_{ctr}$ phototransistor.*
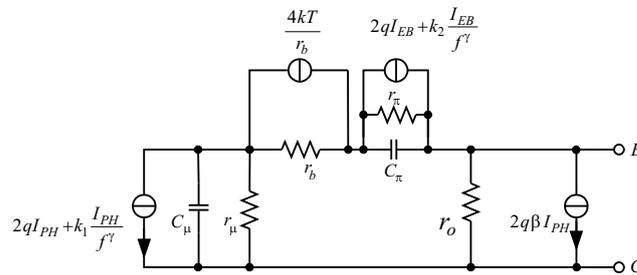
Figure 2: *PNP phototransistor noise model.*

as stated in [3]. In the case of the presented open-base PTs C has a value of 1. This value is caused by the base-collector model resistor r_μ, which acts like a source resistor with a high resistance in the GΩ range. The high source resistor leads to a full correlation between the base noise current part and the collector noise current part [5]. Consequently, the high GΩ value of r_μ prevents the thermal noise current contribution of the base resistance r_b. Thus, nearly the whole noise power of r_b is negligible in the total output current noise $\overline{i_{o_{PT}}^2}$. Furthermore, r_μ, r_π and r_o are model resistors and do not have any noise contribution.

3   Measurements and Results

The noise measurements were performed with the low noise operational amplifier (OPA) LT1124 together with a $300\,\text{k}\Omega$ feedback resistor, a light bulb and a spectrum analyzer (SA). The OPA and the feedback resistor act together as a transimpedance amplifier and convert the output noise current of the PT into a noise voltage, which is captured by the SA. The measured output noise density was corrected by the noise contribution of the SA and the TIA.

Noise current density measurements of the $\text{NW}_{50}\text{E}_{\text{ctr}}$ PT at different collector currents are presented in Fig. 3. The light power was adjusted to meet a defined collector current ($0.1\,\mu\text{A}$, $0.5\,\mu\text{A}$, $1\,\mu\text{A}$, and $2\,\mu\text{A}$). The roll-off at higher frequencies is caused by the bandwidth limitation of the setup. Based on the model, the current gain β of each PT was extracted after (1) from the average noise current density. To verify the correctness of the model, β was measured by electrical Gummel measurements. Both β, the extracted one from the noise model and the measured one were compared and are depicted in Fig. 4. The comparison shows a good agreement of both. The deviation is below 9%. This is a good value if considering the challenge of doing noise measurements and the typically limited precision. Furthermore, the total output white noise current density was modeled according to (1) using the β from the Gummel measurements. A comparison of both noise densities is depicted in Fig. 5. The measured points represent the mean white noise current densities of the results presented in Fig. 3. All points except one are within a range of 12%. Table I summarizes the presented values of the
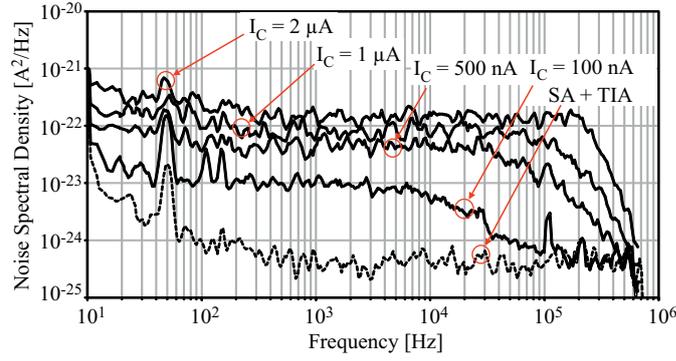
Figure 3: *Output current noise spectral density of the $NW_{50}E_{ctr}$ phototransistor for different light intensities.*
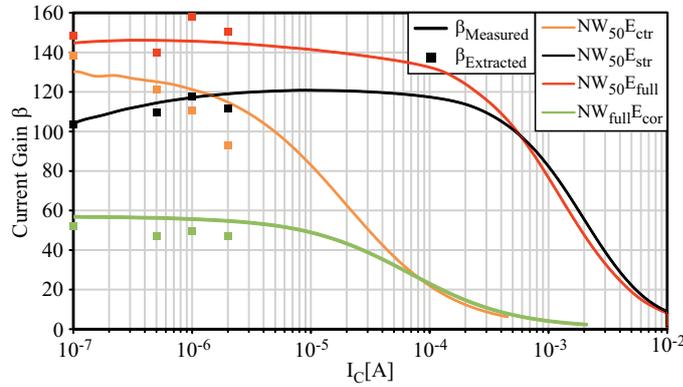
Figure 4: *Measured and extracted current gain β.*
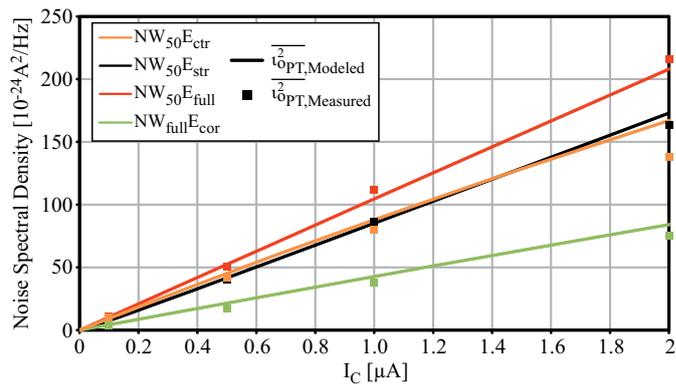
Figure 5: *Measured and modeled output noise current at different I_C.*

Table I: *Measured and modeled values for the output noise current in* $[10^{-24}\ A^2/Hz]$ *and current gain* β *at* $I_C = 1\ \mu A$.

	$\overline{i^2_{o_{PT,Measured}}}$	$\overline{i^2_{o_{PT,Modeled}}}$	$\beta_{Measured}$	$\beta_{Extracted}$
NW$_{50}$E$_{ctr}$	80.2	87.6	121	111
NW$_{50}$E$_{str}$	86.5	86.1	117	118
NW$_{50}$E$_{full}$	112.0	104.5	146	158
NW$_{full}$E$_{cor}$	38.3	42.8	55	50

current gain β and the output noise current of each PT at a collector current of $1\,\mu A$.

4   Conclusion

A noise model for open-base configured phototransistors was developed and verified. The model and the verification are based on measurements done on four pnp pin phototransistors. Each device was processed in a $0.6\,\mu m$ CMOS process and has different characteristics. Phototransistor noise measurements were performed at four different collector currents. Furthermore, electrical Gummel measurements were performed to determine the current gain β of each phototransistor. The model was verified by modeling the current gain β and the output noise current from the noise current density and the Gummel measurements, respectively. Both, the modeled and the measured values were compared at the same collector currents. The comparison shows a difference of less than 12% between the modeled and the measured values of the current gain and the output noise current density.

Acknowledgements

References

[1] J. Hurwitz, M. Panaghiston, K. Findlater, R. Henderson, T. Bailey, A. Holmes, and B. Paisley, "A 35 mm Film Format CMOS Image Sensor for Camera-Back Applications," in *IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 1, pp. 48–443, 2002.

[2] P. Kostov, W. Gaberl, and H. Zimmermann, "Visible and NIR integrated Phototransistors in CMOS technology," *Solid-State Electronics*, vol. 65-66, pp. 211–218, 2011.

[3] D. Decoster and J. Harari, *Optoelectronic Sensors*. Hoboken, London: Wiley-ISTE, 2009.

[4] F. De La Moneda, E. Chenette, and A. Van Der Ziel, "Noise in Phototransistors," *IEEE Transactions on Electron Devices*, vol. 18, no. 6, pp. 340–346, 1971.

[5] S. Bruce, L. K. J. Vandamme, and A. Rydberg, "Measurement of Low-Frequency Base and Collector Current Noise and Coherence in SiGe Heterojunction Bipolar Transistors Using Transimpedance Amplifiers," *IEEE Transactions on Electron Devices*, vol. 46, no. 5, pp. 993–1000, 1999.

Comparison and Conclusion

Within this thesis new kinds of bipolar phototransistors have been built and investigated. These devices were built in three different standard CMOS technologies: $0.18\,\mu m$, $0.35\,\mu m$, and $0.6\,\mu m$. All phototransistors were fabricated on a p-substrate wafer. Due to the availability of PIN photodiodes on a p-substrate, a conclusion can be drawn that only PNP PIN phototransistors were technically feasible.

The first phototransistors were developed and built in a $0.6\,\mu m$ process. The next realisation of phototransistors was exploiting smaller structure sizes of a $0.18\,\mu m$ CMOS process. Even though the results gained in this technology were promising, due to bankruptcy of the fab, I had to switch to another process. As mentioned in the introduction, as well as in the publications, the phototransistors designed within the scope of this dissertation benefit from a low-doped epitaxial layer. Therefore, the most advanced commercially available process that exploits an intrinsic-like layer for the photodetection was a $0.35\,\mu m$ CMOS process. For saving production costs, it was necessary to produce the phototransistors together with further integrated circuits from the workgroup in cumulative tape outs. This mainly influenced the chronology of the used technologies.

For different technology nodes the characteristics of a PIN photodiode changes only lightly. However, this was not the case for the investigated phototransistors, which is mainly caused by different well dopings in the different technologies. This does not influence the PIN photodiodes since in their structure no well is present. Thus the effective base doping will change for the implementations in different technologies leading into different sizes of the base-emitter and base-collector space-charge regions. These parameters are process dependent and their influence has to be

investigated for each technology.

Due to the possible monolithically integration of the photodetector together with a read out circuitry it is benefitial to use smaller technologies. If the phototransistor is used as a sensor element in a pixel array of a camera then the following readout circuitry will need a smaller area in a smaller technology. Thus the fill factor will be increased compared to the same implementation in a larger technology.

The major outcome of this thesis is that the characteristics of each phototransistor can be adjusted by varying the layout of the base and the emitter. This variation leads to different properties of the transit time of charge carriers as well as to different recombination probabilities within the phototransistor. As a consequence the bandwidth and the responsivity of the phototransistor can be adjusted and optimized for a variaty of different applications during the design phase.

The phototransistors can be designed for a high bandwidth, a high responsivity or for an optimum combination of both leading to a high responsivity-bandwidth product (RBP). As a guide for the design of high-bandwidth phototransistors it is important to reduce the base transit time and to reduce the parasitic capacitances caused by the base-emitter and base-collector space-charge regions. These reductions are fulfilled by (I) including an intrinsic layer between base and collector, (II) changing the emitter area as discussed in the following, and (III) lowering the base doping concentration, by implementing the base as n-well stripes. Reducing the emitter area leads to a smaller base-emitter capacitance and has therefore a positive effect on the bandwidth of the device. However, at the same time the probability for charge recombination in the base is increased since minority charges have to travel longer distances within the base to reach the base-emitter space-charge region. This limits the phototransistor's gain β and in turn its responsivity. Furthermore, these longer distances lead to increased transit times of minority charges through the base, causing a reduction of the bandwidth. However, the positive effect of reduction of the base-emitter capacitance surpasses the negative effect of the increased transit time. As for an ordinary bipolar junction transistor, the bandwidth of the phototransistor is indirectly proportional to the gain of the de-

vice. The higher the gain is, the lower is the bandwidth of the phototransistor. Thus a reduced gain will further improve the bandwidth. An additional increase of the bandwidth can be achieved by reducing the base-collector capacitance. In addition to the implementation of the low doped epitaxial layer a reduction of the phototransistor size helps to reduce the capacitance.

For designing a phototransistor with a high responsivity it is necessary to increase the area of the emitter. Correspondingly, the size of the emitter area is a trade-off between high responsivity and high bandwidth.

As figure of merit for the comparison of the different phototransistors the RBP is used. From the investigations on the presented phototransistors in the first used technologies ($0.6\,\mu$m and $0.18\,\mu$m) the optimum RBP was found for phototransistors with a 50% doped base and a striped emitter. These investigations and results from the phototransistors implemented in these first two CMOS processes lead to the new idea of developing a phototransistor with 18 base-emitter pairs, which was implemented in the $0.35\,\mu$m CMOS process. As already mentioned above, a small emitter will lead to a faster device. However, if the base is implemented as an n-well over the entire photosensitive area, then the minority charges in the base will have to travel longer distances in the field free region through the base. This is a slow diffusion process. Thus, to further increase the bandwidth, the dimension of the base under the emitter was reduced to the minimum possible area regarding to the design rules of the process. The resulting base-emitter islands are placed close enough to each other so that the epitaxial region between them is fully depleted for a large enough applied voltage. This leads to a fast device. Furthermore, the strongly reduced base area causes a decreased probability for recombination in the base.

During the dissertation a large variety of phototransistor with different doping concentrations of the base, varying area sizes, and locations of the emitter were investigated. The presented publications in this thesis are ordered by technologies, ascending:

In **Publications A** to **E** phototransistors implemented in a $0.18\,\mu$m CMOS process are presented. The phototransistors reported in **Publication A** and **B** have

the same sizes and locations of the emitter. But they differ in the size, doping concentration, and location of the base. In both publications one phototransistor was presented with an emitter at the edge of the photosensitive area. The intention of placing the emitter at the edge was to have the possibility for applying an optical window together with an anti-reflection coating on top of the remaining photosensitive area. This is not possible for a centered emitter since the etch for the optical window would destroy the metals for connecting the emitter. In **Publication C** and **D** phototransistors with striped emitters and different doping concentration of the base are presented. **Publication E** deals with the noise behaviour of the phototransistors presented in **Publications A** to **D**.

The phototransistor with the 18 emitter-base pairs built in the 0.35 µm CMOS process is presented in **Publication F**. It should be again mentioned that this device is the most promising phototransistor for high speed due to its emitter-base islands and the fully depleted space-charge region between them for a large enough reverse voltage. The reduction of the base area and the thus the reduction of the diffusion through the base speeds up the device.

In **Publication G** phototransistors built in the 0.6 µm CMOS process with different layouts of the base and emitter are presented. In **Publication H** the development and investigation of a phototransistor noise model based on noise measurements and results from the phototransistor presented in **Publication G** is reported. Several of the presented structures were simulated and the phototransistors were characterized by measuring their most important characteristics, i.e. responsivity, bandwidth, rise and fall time, noise, etc., at different wavelengths.

A comparison of the phototransistors is given for the responsivity, bandwidth, and RBP for the three investigated wavelengths (410 nm, 675 nm, and 850 nm) in an open base configuration for the three different technologies. The best achieved results of this comparison are summarized in Tab. 1. The bold values show the highest achieved results for each category. Phototransistors built in 0.18 µm and 0.35 µm CMOS have smaller responsivities compared to the phototransistors built in 0.6 µm CMOS. Due to the lower base doping concentration in the 0.6 µm CMOS process a higher gain β could be achieved, resulting in a higher responsivity compared to the smaller technologies. As mentioned before, the frequency response of

Table 1: *Comparison of the best achieved phototransistor results for responsivity, bandwidth, and responsivity-bandwidth product (RBP) for the three technologies 0.18 μm, 0.35 μm, and 0.6 μm at 410 nm (top), 675 nm (middle), and 850 nm (bottom) in open base configuration.*

Techno-logy	Publi-cation	Phototransistor Type	Responsivity [A/W]	Bandwidth [MHz]	RBP [A/W·MHz]
0.18 μm	C	Striped E; 50% doped B	**4.1**	13.5	**55.4**
	A	Small edge E; fully doped B	0.5	**60.5**	30.3
0.35 μm	F	18 point E; small B under E	**0.7**	**151.4**	**106.0**
0.6 μm	G	Striped E; 50% doped B	**20.5**	5.0	**102.5**
	G	Small edge E; fully doped B	1.6	**11.7**	18.7

@ λ = 410 nm, (E...Emitter, B...Base)

Techno-logy	Publi-cation	Phototransistor Type	Responsivity [A/W]	Bandwidth [MHz]	RBP [A/W·MHz]
0.18 μm	C	Striped E; 50% doped B	**12.4**	19.3	**238.4**
	B	Small B and E at the edge	2.2	**92.0**	202.4
0.35 μm	F	18 point E; small B under E	**2.0**	**125.9**	**251.8**
0.6 μm	G	Full E; 50% doped B	**95.4**	1.4	133.6
	G	Small B and E at the edge	18.3	**8.3**	151.9
	G	Striped E; 50% doped B	71.1	2.5	**177.8**

@ λ = 675 nm, (E...Emitter, B...Base)

Techno-logy	Publi-cation	Phototransistor Type	Responsivity [A/W]	Bandwidth [MHz]	RBP [A/W·MHz]
0.18 μm	C	Striped E; 50% doped B	**7.9**	16.1	**127.2**
	B	Small edge E; fully doped B	1.5	**50.7**	76.1
0.35 μm	F	18 point E; small B under E	**1.4**	**109.6**	**153.4**
0.6 μm	G	Full E; 50% doped B	**37.2**	1.3	48.4
	G	Small edge E; fully doped B	6.3	**8.5**	53.6
	G	Striped E; 50% doped B	31.1	2.3	**71.5**

@ λ = 850 nm, (E...Emitter, B...Base)

a phototransistor is indirect proportional to its gain (or responsivity). This fact leads to the smaller achieved bandwidths of the phototransistors built in 0.6 μm CMOS compared to the others built in 0.18 μm and 0.35 μm CMOS. It is remarkable that the highest values for the RBPs in the three processes are all of the same order of magnitude. As noticeable, the phototransistor with the 18 emitter-base pairs (**Publication F**) achieves the highest values for the RBP. They are 106.0 A/W·MHz, 251.8 A/W·MHz, and 153.4 A/W·MHz at 410 nm, 675 nm, and 850 nm, respectively. Furthermore the same device achieves also the highest bandwidths: 151.4 MHz, 125.9 MHz, and 109.6 MHz at 410 nm, 675 nm, and 850 nm, respectively. The highest bandwidth could be achieved for the wavelength with the shortest penetration depth (410 nm). This is caused since most of the charge carriers are generated in the base-collector space-charge region that reaches up to the surface between the base islands. Therefore the photogenerated current consists mostly of a fast drift current and only a negligible amount of slower diffusion current. The photogenerated charges will drift laterally to the base. The bandwidth of this phototransistor decreases for longer wavelengths with deeper penetration depths due to the larger amount of diffusion current and longer drift distances.

For the phototransistors, which have a base over the entire photosensitive area the bandwidth is highest for 675 nm due to its optimum penetration depth within the base-collector space-charge region. For light with 410 nm wavelength the penetration into silicon will be close to the surface and thus the generation of charge carriers will be outside the depletion region. In such phototransistors the photogenerated charges will cause a high part of diffusion current and only a small part of drift current. A similar effect has deep penetrating light of e.g. 850 nm. In this case a part of the charges will be generated in the field free region of the base or emitter (depending on the phototransistor structure) as well as in the field free region of the collector (substrate) and thus causing also a slow diffusion current. This leads to a reduced bandwidth compared to irradiation with light with 675 nm wavelength.

In addition to the responsivity, bandwidth, and RBP of a phototransistor also the lowest possible detectable signal is highly interesting. This characteristic is

determind by the noise behaviour of the phototransistor. The investigation of the noise behaviour together with the development of a noise model is presented in the publications **Publication E**, **F**, and **H**. Bipolar junction transistors typically suffer from thermal noise of the base resistor, $1/f$ noise, and shot noise. As presented in the publications, thermal noise caused by the base resistor is no issue in phototransistors in open base configuration. However, their output current noise is higher than that of a photodiode. This is caused by (I) the amplification of the photocurrent and by (II) an additional excess noise caused by the correlation of the base shot noise current and the collector shot noise current. The phototransistor presented in **Publication D** shows the lowest noise when comparing the equivalent input current noise of this device with the current noise of the other phototransistors as reported in **Publication E**. The equivalent input current noise for this phototransistor for an collector current of $2\,\mu A$ is $3.63\,dB$ larger than the current noise of a photodiode with a corresponding photocurrent.

Tab. 2 shows a comparison of the phototransistors with the best achieved RBP from each process (presented in **Publication C**, **F**, and **G**) and devices from the literature. A comparison is difficult since for most of the phototransistors from literature the bandwidth is not investigated. Almost each device from the literature has only information on the responsivity of the corresponding phototransistor. However, comparing the RBPs of the presented phototransistors with those from the literature, where bandwidth informations is available, it can be seen that the performance of the presented phototransistors surpasses that of the state-of-the-art CMOS phototransistors by several orders of magnitude.

The cheap and easy fabrication of the presented PNP PIN phototransistors in standard CMOS processes together with the needlessness of a following amplification chain offers new possibilities for commercial high-gain photodetecting devices. Together with an appropriate readout circuitry these phototransistors can be used as photodetectors in range finding sensors as presented in [1–3]. In such applications a high fill factor is desired. This can be achieved by implementing the monolithic circuitry into a smaller CMOS technology. However, the results show that for this application a photodiode is more appropriate than a phototransistor due to a

higher dynamic range and better linearity and controllability in background light conditions [4]. These phototransistors are very promising devices for applications with well defined irradiation conditions as in closed systems (e.g. sheer force sensors as presented in [5]). There the bad linearity is not an issue and the application can take full advantage of the inherent gain and bandwidth of the phototransistor. Further possible applications are be light barriers, opto-coupler, etc.

Table 2: Comparison of the best presented phototransistors from each technology with devices from the literature.

Refs.	Publi-cation	Techno-logy	Device type	Dimension (μm^2)	Wavelength (nm)	Responsivity (A/W)	f_{-3dB} (MHz)	RBP (A/W·MHz)
[6]		65 nm CMOS	NPN	60×60	850	0.34	0.15	0.05
[7]		0.35 µm CMOS	PNP	35×35	×	×	< 1	×
[8]		0.35 µm CMOS	PNP	×	Red	0.83	0.034	0.03
[9]		0.8 µm BiCMOS	NPN	53×53	638	×	7.8	×
[10]		1.2 µm CMOS	PNP	×	730	75	×	×
[11]		2.0 µm CMOS	PNP	60×60	633	27	×	×
	C	0.18 µm CMOS	PNP	100×100	410	4.1	13.5	55.4
					675	12.4	19.3	238.4
					850	7.9	16.1	127.1
This work*	F	0.35 µm CMOS	PNP	50×100	410	0.7	151.4	106.0
					675	2.0	125.9	251.8
					850	1.4	109.6	153.4
	G	0.6 µm CMOS	PNP	100×100	410	20.5	5.0	102.5
					675	71.1	2.5	177.8
					850	31.1	2.3	71.5

* Best results for RBP in open-base configuration presented.

References

[1] P. Kostov, M. Davidovic, M. Hofbauer, W. Gaberl, and H. Zimmermann, "Phototransistor Based Time-of-Flight Range Finding Sensor in an 180 nm CMOS Process," in *IEEE Photonics Conference (IPC)*, pp. 28–29, 2012.

[2] P. Kostov, M. Davidovic, M. Hofbauer, J. Seiter, W. Gaberl, and H. Zimmermann, "Time-of-Flight Range Finding Sensor Using a PNP Bipolar Phototransistor in a 0.35 µm CMOS Process With High Immunity Against Background Light," in *IEEE Photonics Conference (IPC)*, p. submitted, 2013.

[3] M. Davidovic, P. Kostov, M. Hofbauer, W. Gaberl, and H. Zimmermann, "Time-Of-Flight Range Finding Sensor Using an Integrated PNP PIN Phototransistor in 180 nm CMOS," in *IEEE International Conference on Group IV Photonics (GFP)*, pp. 258–260, 2012.

[4] M. Davidovic, *Enhanced Dynamic Range Distance Measurement Sensor with Low Noise*. PhD thesis, Vienna University of Technology, 2012.

[5] J. Missinne, P. Kostov, B. Van Hoe, E. Bosman, W. Gaberl, H. Zimmermann, and G. Van Steenberge, "Ultra-Thin Multi-Axial Shear Stress Sensor Based on a Segmented Photodiode," in *IEEE Photonics Conference (IPC)*, p. submitted, 2013.

[6] A. Carusone, H. Yasotharan, and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, 2011.

[7] A. Hu and V. P. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274–280, 2010.

[8] Y. Matsumoto, T. Hara, and Y. Kimura, "CMOS photo-transistor array detection system for visual light identification (ID)," in *IEEE International Conference on Networked Sensing Systems (INSS)*, pp. 99–102, 2008.

[9] K. Kieschnick, H. Zimmermann, and P. Seegebrecht, "Silicon-based optical receivers in BiCMOS technology for advanced optoelectronic integrated circuits," *Materials Science in Semiconductor Processing*, vol. 3, no. 5-6, pp. 395–398, 2000.

[10] R. Sandage and J. A. Connelly, "A 128×128 Imaging Array Using Lateral Bipolar Phototransistors in a Standard CMOS Process," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 6, pp. 641–644, 1998.

[11] R. Sandage and J. A. Connelly, "Producing Phototransistors in a Standard Digital CMOS Technology," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp. 369–372, 1996.

List of Own Publications

Journal Papers

1. P. Kostov, K. Schneider-Hornstein, and H. Zimmermann, "Phototransistors for CMOS Optoelectronic Integrated Circuits," *Sensors and Actuators A: Physical*, vol. 172, no. 1, pp. 140 – 147, 2011.

2. P. Kostov, W. Gaberl, and H. Zimmermann, "Visible and NIR Integrated Phototransistors in CMOS Technology," *Solid-State Electronics*, vol. 65 – 66, pp. 211 – 218, 2011.

3. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "PNP PIN Bipolar Phototransistors for High-Speed Applications Built in a 180 nm CMOS Process," *Solid-State Electronics*, vol. 74, pp. 49 – 57, 2012.

4. P. Kostov, W. Gaberl, and H. Zimmermann, "High-Speed Bipolar Phototransistors in a 180 nm CMOS Process," *Optics & Laser Technology*, vol. 46, pp. 6 – 13, 2013.

Conference Papers

1. P. Kostov, W. Gaberl, and H. Zimmermann, "Integrated Phototransistors in a CMOS Process for Optoelectronic Integrated Circuits," *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pp. 250 – 253, 2010.

2. P. Kostov, W. Gaberl, and H. Zimmermann, "CMOS Phototranisistors for

Deep Penetrating Light," *IMEKO TC2 Symposium on Photonics in Measurement*, pp. 46 – 49, 2011.

3. P. Kostov, W. Gaberl, A. Polzer, and H. Zimmermann, "CMOS PIN Phototransistors for High-Speed Photosensitive Applications," *Procedia Engineering (Eurosensors Conference)*, vol. 25, pp. 1397 – 1400, 2011.

4. P. Kostov, W. Gaberl, and H. Zimmermann, "High-Speed PNP PIN Phototransistors in a 0.18 μm CMOS Process," *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pp. 187 – 190, 2011.

5. P. Kostov and H. Zimmermann, "Integrierte CMOS PIN-Fototransistoren für kurzwelliges infrarotes Licht," *Messtechnisches Symposium des Arbeitskreises der Hochschullehrer für Messtechnik (AHMT)*, pp. 139 – 150, 2011.

6. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Integrated 180 nm CMOS Phototransistors with an Optimized Responsivity-Bandwidth-Product," *IEEE Photonics Conference (IPC)*, pp. 314 – 315, 2012.

7. P. Kostov, M. Davidovic, M. Hofbauer, W. Gaberl, and H. Zimmermann, "Phototransistor Based Time-of-Flight Range Finding Sensor in an 180 nm CMOS Process," *IEEE Photonics Conference (IPC)*, pp. 28 – 29, 2012.

8. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Bandwidth and Gain Enhanced PNP Phototransistors for VIS and NIR Light in 180 nm CMOS," *IEEE International Semiconductor Conference (CAS)*, pp. 475 – 478, 2012, Best Paper Award.

9. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Low Frequency Noise in CMOS PNP PIN Phototranisistors," *IEEE International Conference on Noise and Fluctuations (ICNF)*, 2013, accepted.

10. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "Development and Verification of a CMOS Phototransistor Noise Model," *IEEE International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, 2013, accepted.

11. P. Kostov, M. Davidovic, M. Hofbauer, J. Seiter, W. Gaberl, and H. Zimmermann, "Time-of-Flight Range Finding Sensor Using a PNP Bipolar Phototransistor in a 0.35 µm CMOS Process With High Immunity Against Background Light," *IEEE Photonics Conference (IPC)*, 2013, submitted.

12. P. Kostov, W. Gaberl, M. Hofbauer, and H. Zimmermann, "High-Speed Low-Noise PNP PIN Phototransistor integrated in an 0.35 µm CMOS Process," *IEEE Photonics Conference (IPC)*, 2013, submitted.

13. M. Davidovic, P. Kostov, M. Hofbauer, W. Gaberl, and H. Zimmermann, "Time-Of-Flight Range Finding Sensor Using an Integrated PNP PIN Phototransistor in 180 nm CMOS," *IEEE 9th International Conference on Group IV Photonics (GFP)*, pp. 258 – 260, 2012.

14. A. Polzer, K. Schneider-Hornstein, J. Dong, P. Kostov, and H. Zimmermann, "Investigation of triple-junction photodetector in 90 nm CMOS technology," *Procedia Engineering (Eurosensors Conference)*, vol. 25, pp. 864 – 867, 2012.

15. J. Missinne, P. Kostov, B. Van Hoe, E. Bosman, W. Gaberl, H. Zimmermann, and G. Van Steenberge, "Ultra-Thin Multi-Axial Shear Stress Sensor Based on a Segmented Photodiode," *IEEE Photonics Conference (IPC)*, 2013, submitted.

Book Chapters

1. M. Perenzoni, P. Kostov, M. Davidovic, G. Zach, and H. Zimmermann, *TOF Range-Imaging Cameras*, ch. Electronics-Based 3D Sensors. Berlin/Heidelberg, Germany: Springer-Verlag, first ed., ISBN: 3642275222, pp. 39 – 68, 2013.

Curriculum Vitae

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